AC-Dynamic

You can start AC-Dynamic with different parameters. A help screen will display with

ac_dynmaic –h

The chain length is fixed with the parameter *–c* followed by a number (blank). All possible chain lengths will be simulated if this parameter is not set. The parameter *–a* chooses an asymmetric clock signal, while it is not set a symmetric clock signal is used. All clean buffer chains will be transformed in a single TSPC-gate with the parameter *–bufchains*. This parameter can only set in combination with a fixed chain length. If the parameter *–debug* is set, a debug modus starts after every optimization. In this modus you can get information about every gate and the structure of the circuit. The parameter *–l* followed by a number (blank) set the quantity of information, which is displayed as the program runs. The smallest value is 0. The parameters *–no, -nbo* and *–uni* affect the optimization. No optimization will proceed if the parameter *–no* (no optimization) is set. The parameter *–uni* has to set if the tool should insert Uni-Logics. If the parameter *–nbo* (new buffer optimization) is set, buffers will be insert to delay some signals. Sometimes it is needful to get all information of the gates, which the tool uses internally. You get an according netlist with the parameter *–pipe*.

You start the tool with:

ac_dynamic [parameter] XNF-file

You can choose several parameters.
You get two netlists if the tool is ready. The name of these netlists depends on the symmetry of the clock signal:

Timing_best_sym_clk.xnf and *Timing_best_latenz_sym_clk.xnf*
or
Timing_best_unsym_clk.xnf and *Timing_best_latenz_unsym_clk.xnf*

These netlists include the solutions fort he highest clock frequency and the shortest latency time.

If the debug modus is active, you get a selected menu after the evaluation for every chain length. You can choose the options by the according numbers. If you select the number 2, you get the rules. These rules specify which input signals are necessary to start an evaluation. Over the numbers 2 to 8 and 12 to 18 you can display the times for every gate, whereas *e* means the evaluation, *p* means precharge and *i* means input signal. You get the properties of every gate with number 10 (specify the coordinates in the array) and number 20 (specify the name of the gate). You have to choose number 21 if you want check this netlist work with a special clock frequency. Then at first you have to input the length of the low phase of the clock signal in ns, then the length of the high phase, and then the debug level. To exit choose number 0.

Format of the Timing-Information

The timing parameter has to integrate for every gate into the XNF-netlist file. If there are no parameters, the tool uses standard values (AMS 0.6µm). The syntax of the timing parameter is:

SYM, …
TIM,*pre_min,pre_max,eva_min,eva_max,ru_min,ru_max,rd_min,rd_max,clk_fall_min,clk_fall_max,clk_rise_min,clk_rise_max*
RULES, (port;port;…)(port;port…)(..)
…

pre means precharge phase, *eva* means evaluation phase, *ru* means ready up (evaluation time for self timed signal after gate is ready with precharge phase), *rd* means ready down (evaluation time for self timed signal after gate is ready with evaluation), *clk_fall* and *clk_rise* means the delay of the clock signal if the gate is the last gate in a chain. RULES means which input signal are necessary to start an evaluation.

The file *timing.cfg* includes the timing values for the self timed logic, the ports of the circuit, and for additional buffers. *uni* means the parameter of the universal logic. *vb* is the prefix for the parameter of the buffer, which have to input to complete the last chains.

If all gates should have the same parameter, use the tool new_timing:

new_timing <eva> <eva_master> <eva_diff> <ru> <ru_diff> <pre> <pre_master> <pre_diff> <rd> <rd_diff> <or> <or_diff> <filename>

You can set special parameters for the last 3 gates in a chain (called master gates) with the *_master_* parameter. *or* means the parameter for an 2-input-or. These values will extrapolate for or-gates with more inputs. *diff* means the positive and negative difference from the set time.