SBCCI2008
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Encountering Gate Oxide Breakdown with Shadow Transistors to Increase Reliability

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Focus / Main ideas

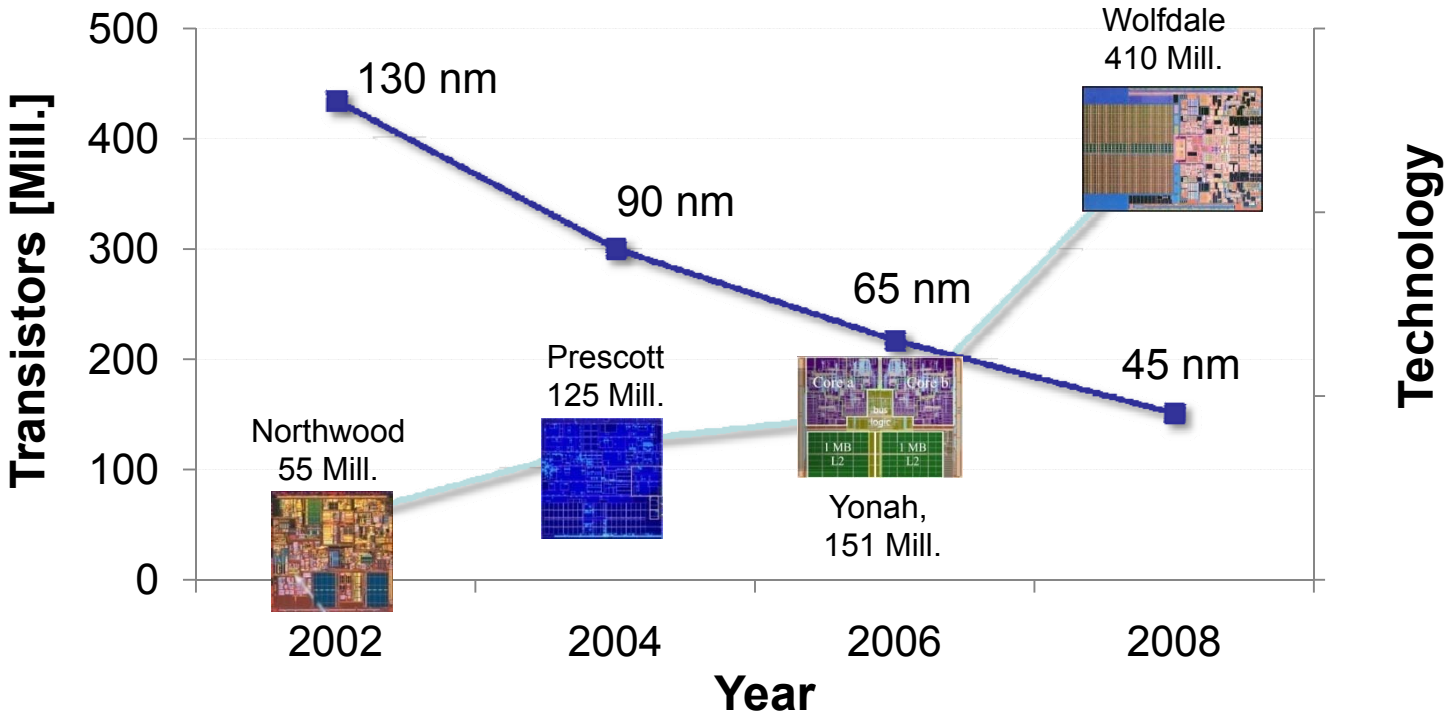
1. **Reliability regarding oxide breakdown**
2. **Transistor / Gate level approach**
3. **Selective insertion / thick oxide devices**

Outline

- Motivation
  - Technology development
  - Error classification
  - Time-Dependent Dielectric Breakdown (TDDB)
- Shadow Transistors
  - Used model
  - Main Ideas
  - Algorithm
- Results
- Conclusion

Motivation

Technology development

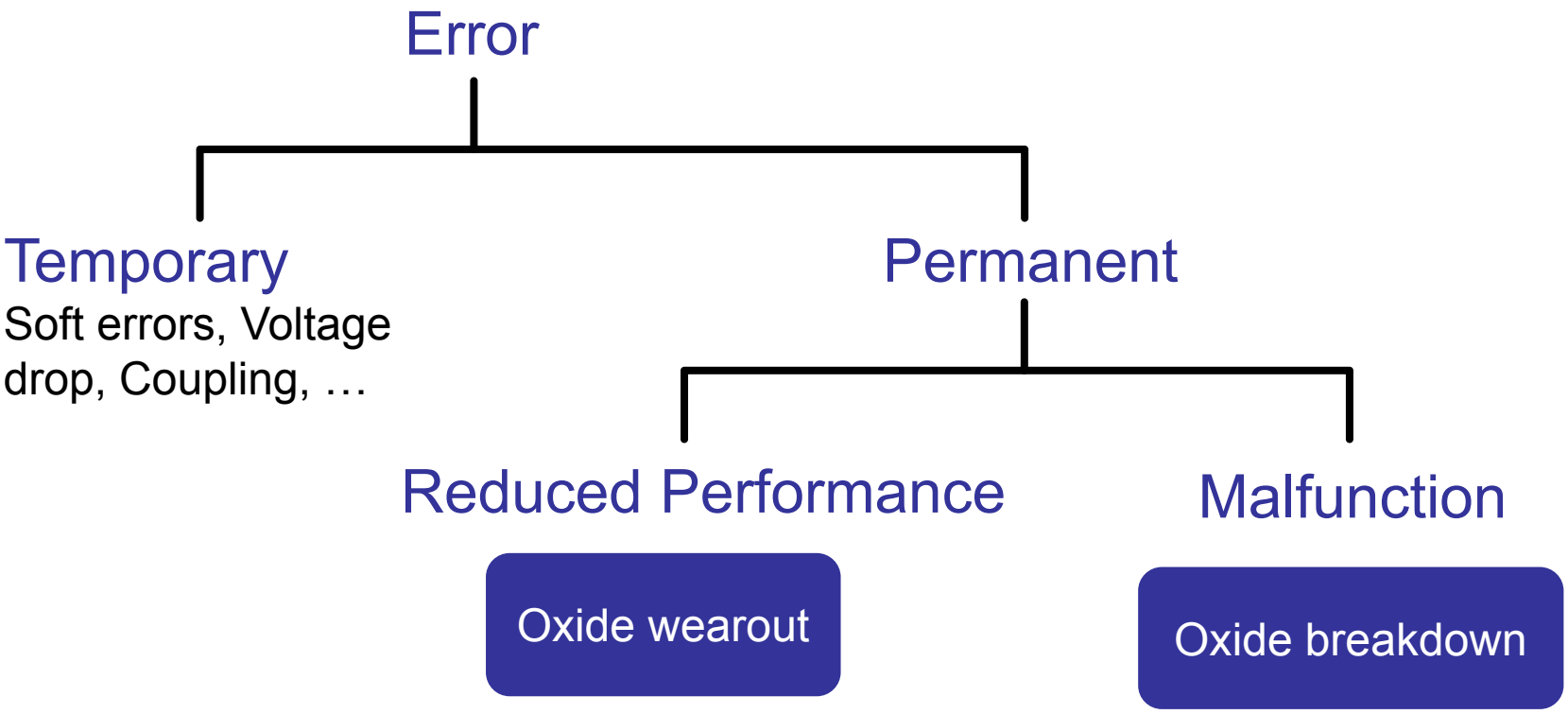


Probability for failures increases due to:

- Increasing transistor count
- Shrinking technology

Motivation

Error classification



Motivation

Time-Dependent Dielectric Breakdown (TDDB)

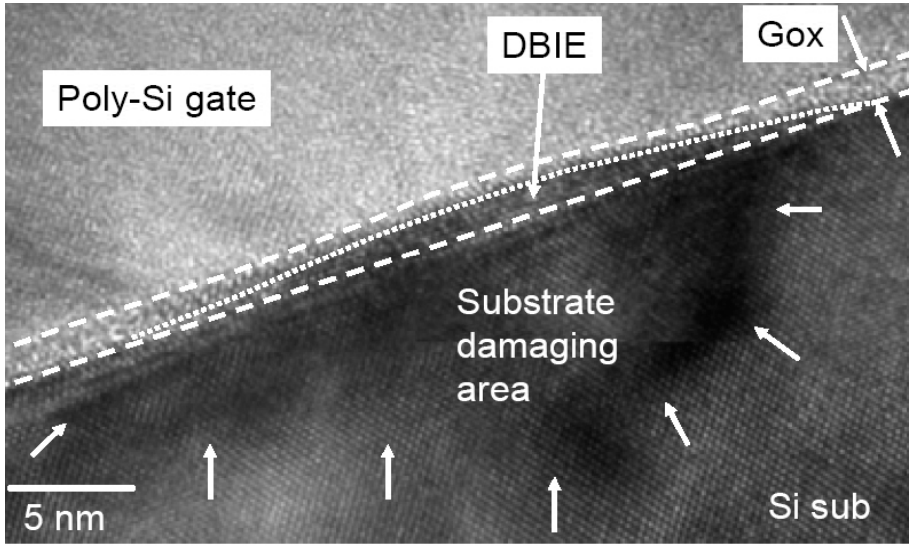
- Tunneling currents

  ↷ Wear out of gate oxide

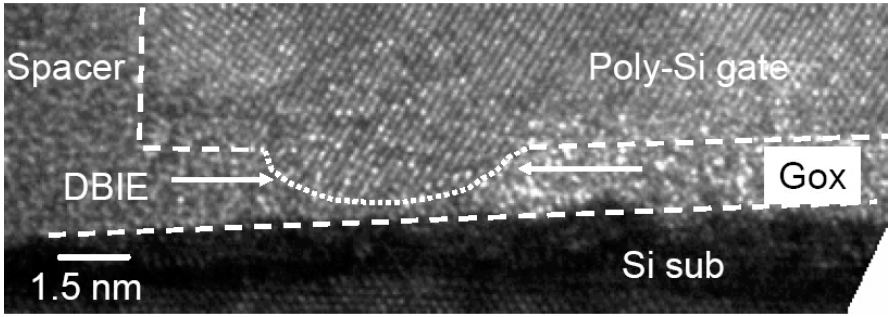
- Creation of conducting path between Gate and Substrate, Drain, Source

- Depending on electrical field over gate oxide, temperature (exp.), and gate oxide thickness (exp.)

- Also: abrupt damage due to extreme overvoltage (e.g. Electro-Static Discharge)



Source: Pey&Tung

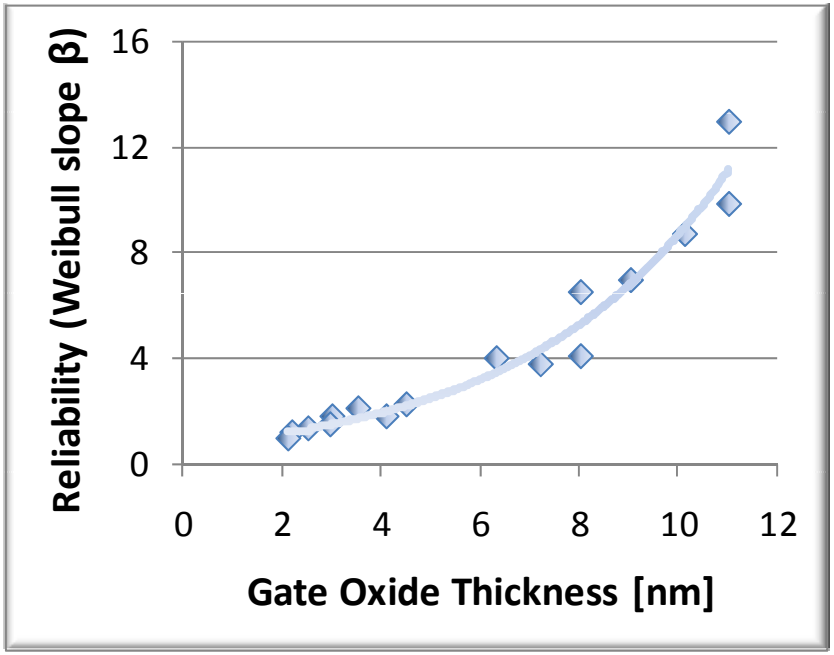


Source: Pey&Tung

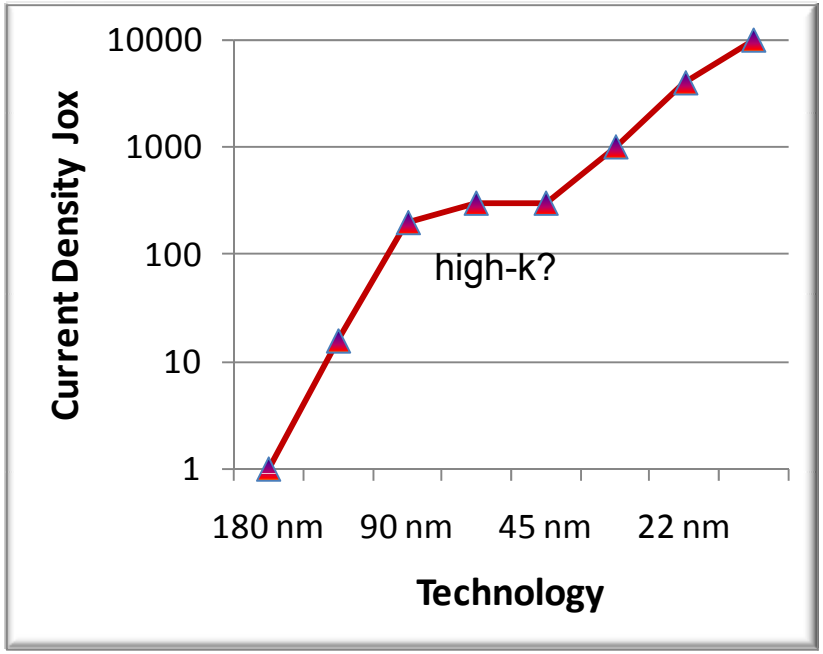
Motivation

TDDB — Trends

Increasing probability for Gate-Oxide-Breakdown



Source: Kauerauf, EDL, 2002

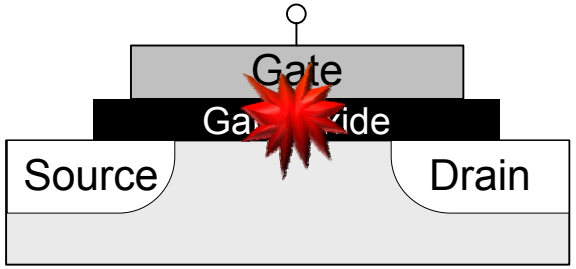


Source: Borkar, Intel

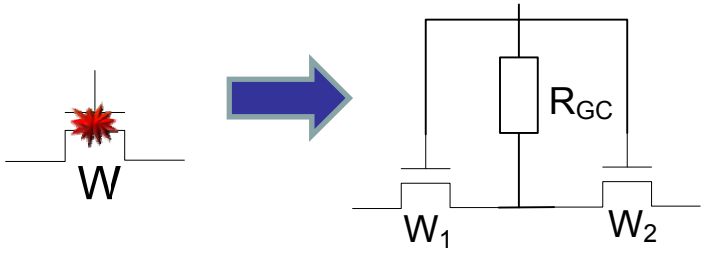
Shadow Transistors

Applied model

TDDB between gate and channel

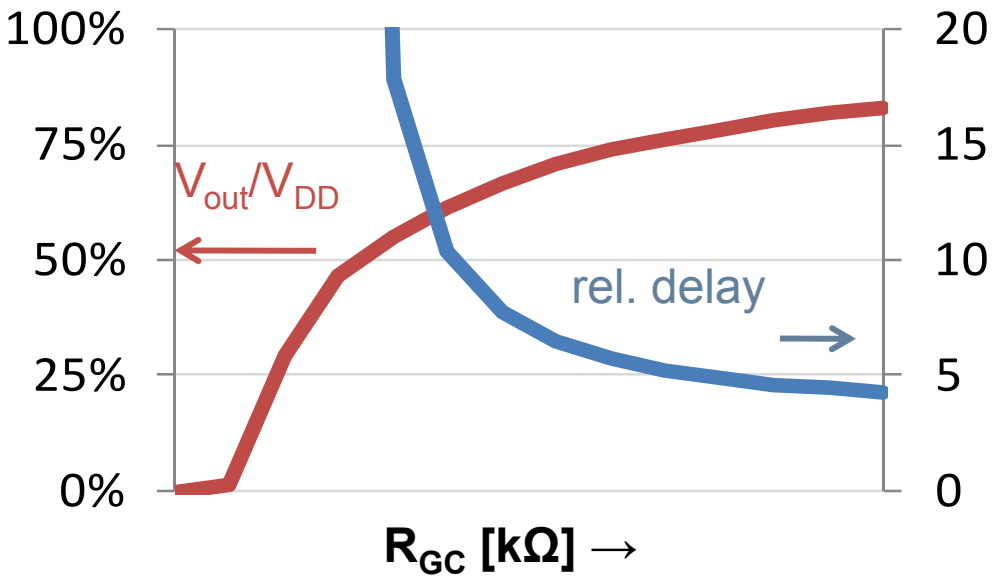


Model:



W= W_1+W_2

For an Inverter, 65nm-BPTM:

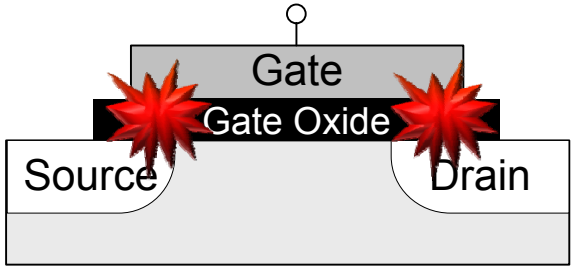


Based on: Segura et. al., "A Detailed Analysis of GOS Defects in MOS Transistors: Testing Implications at Circuit Level" 1995.

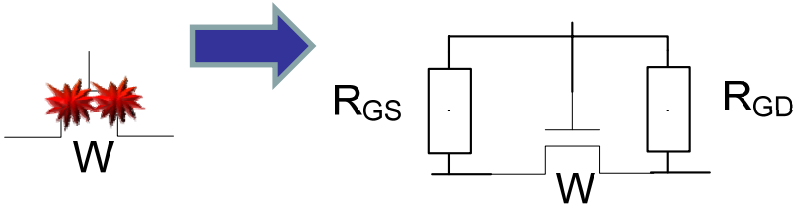
Shadow Transistors

Applied model

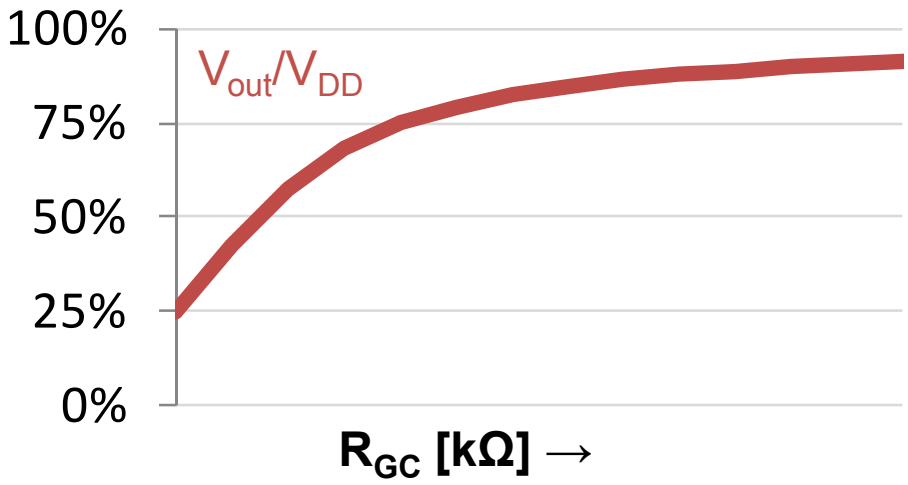
TDDB between gate and source/drain



Model:



For an Inverter, 65nm-BPTM:



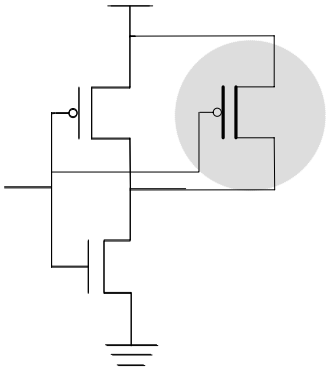
Based on: Segura et. al., “A Detailed Analysis of GOS Defects in MOS Transistors: Testing Implications at Circuit Level” 1995.

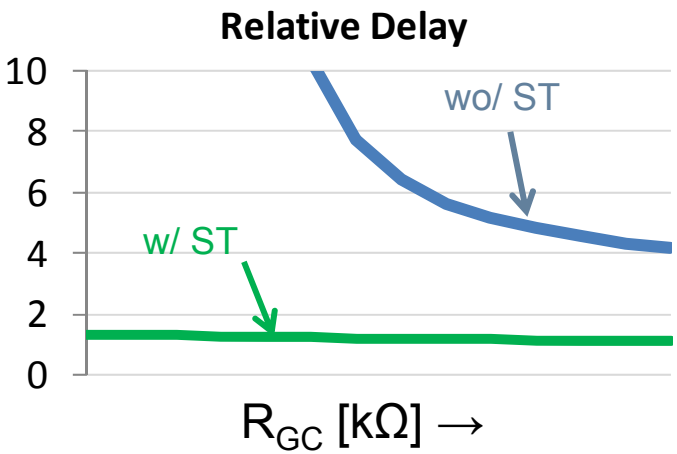
Shadow Transistors

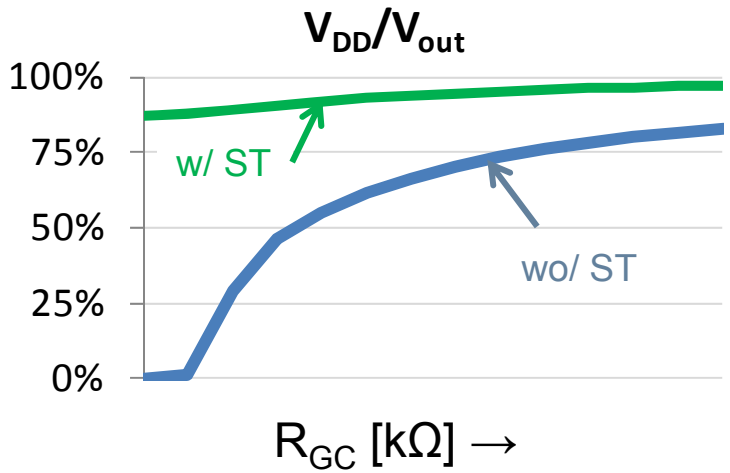
Main idea (1) – Parallel transistors

1. Insertion of additional transistors in parallel to vulnerable transistors

   → **Shadow transistors** (ST)



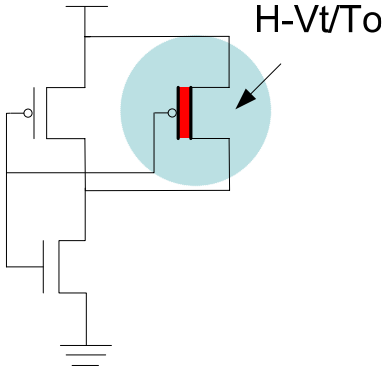




For an Inverter, 65nm-BPTM

Shadow Transistors

Main idea (2) – Thick gate oxides



2. Application of H-Vt/To transistors with:

- Higher threshold voltage
- Thicker gate oxide

↷ **Less vulnerable to TDDB**

$$10^{\frac{\Delta t_{ox}}{0.22}} \quad \curvearrowright \quad \frac{MTTF_{H-Vt/To}}{MTTF_{L-Vt/To}} = 10^{\frac{0.15}{0.22}} = 4.81$$

MTTF – Mean Time To Failure

Source: Srinivasan, "RAMP: A Model for Reliability Aware Microprocessor Design"
Stathis, J., "Reliability Limits for the Gate Insulator in CMOS Technology"

Shadow Transistors

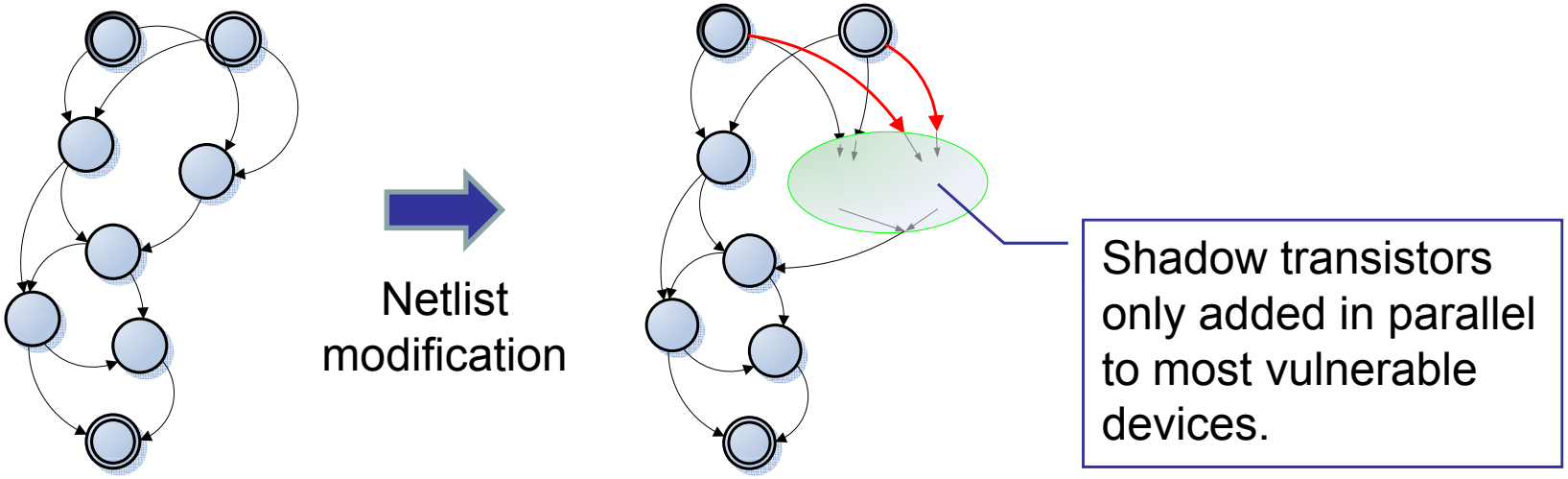
Main idea (3) – Selective insertion

3. Selective insertion of shadow transistors in parallel to vulnerable transistors:

– Component reliability depends on

Activity, state, temperature, size, fabrication …

Most vulnerable can be identified



Shadow Transistors

Main idea (3) – Selective insertion

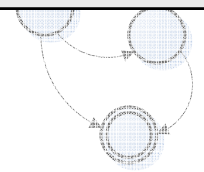
3. Selective insertion of shadow transistors in parallel to vulnerable transistors:

Our Approach

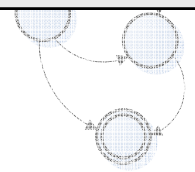
- Estimation of stress factors
- Determination of components reliability
- Adding redundancy only at most vulnerable components

➔ Advantage: **Lower area, power and delay** penalty compared to complete redundancy or random insertion [Sri04]

Source: [Sri04] Sirisantana, D&T, 2004



modification



to most vulnerable devices.

Shadow Transistors

Main ideas – Discussion

Advantages

- Increased reliability in respect to TDDB
- H-Vt/To: Reliability increases by ~5x (for Δt_{ox} = 0.15 nm)

➔ Remarkable increase of system life time

Drawbacks

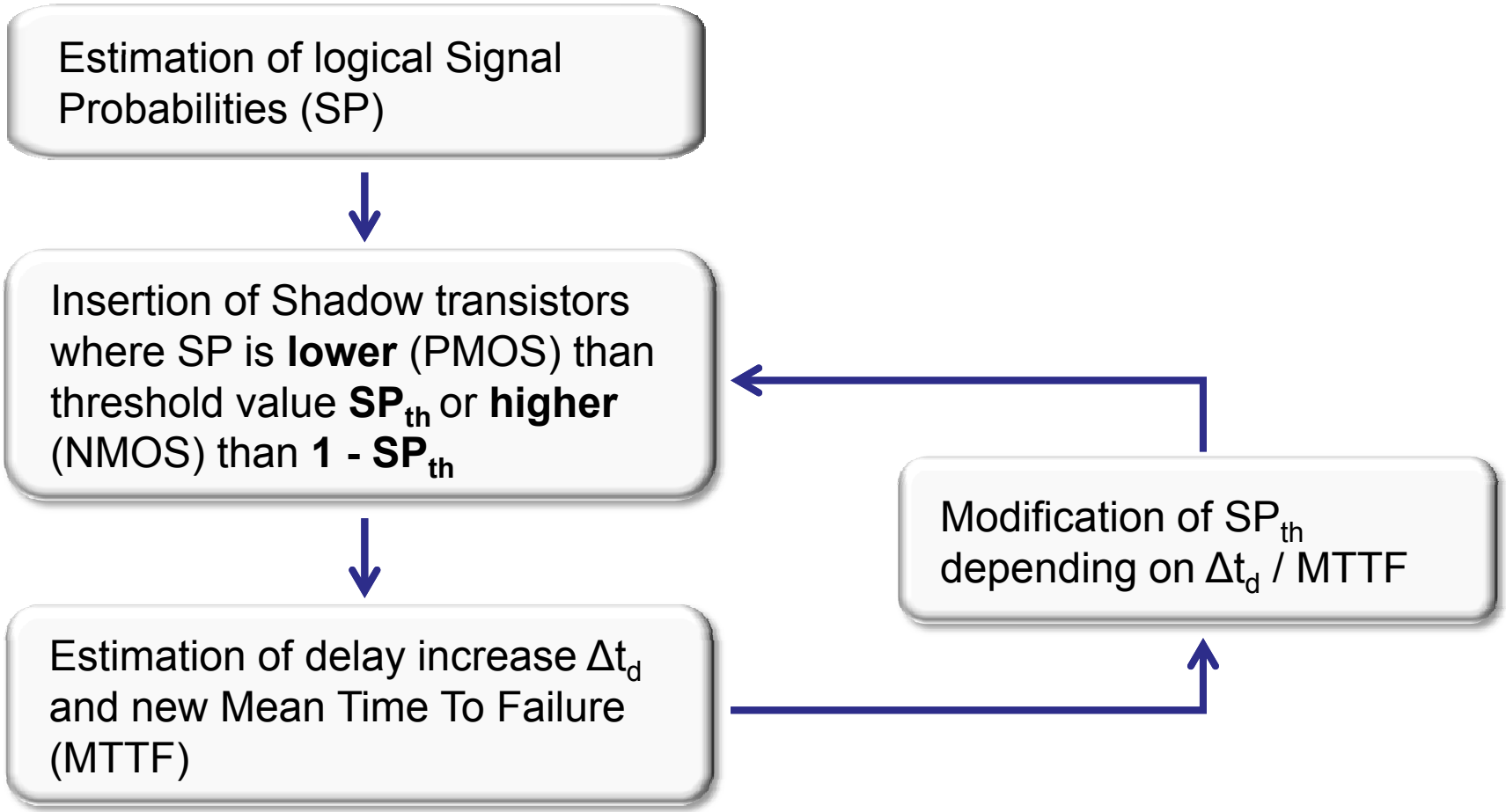
- Higher input capacity → higher delay and dynamic power dissipation
- Area increase

Remarks

- Only slight improvements for Gate-Drain/Source breakdown
- H-Vt/To has to be supported by technology

Shadow Transistors

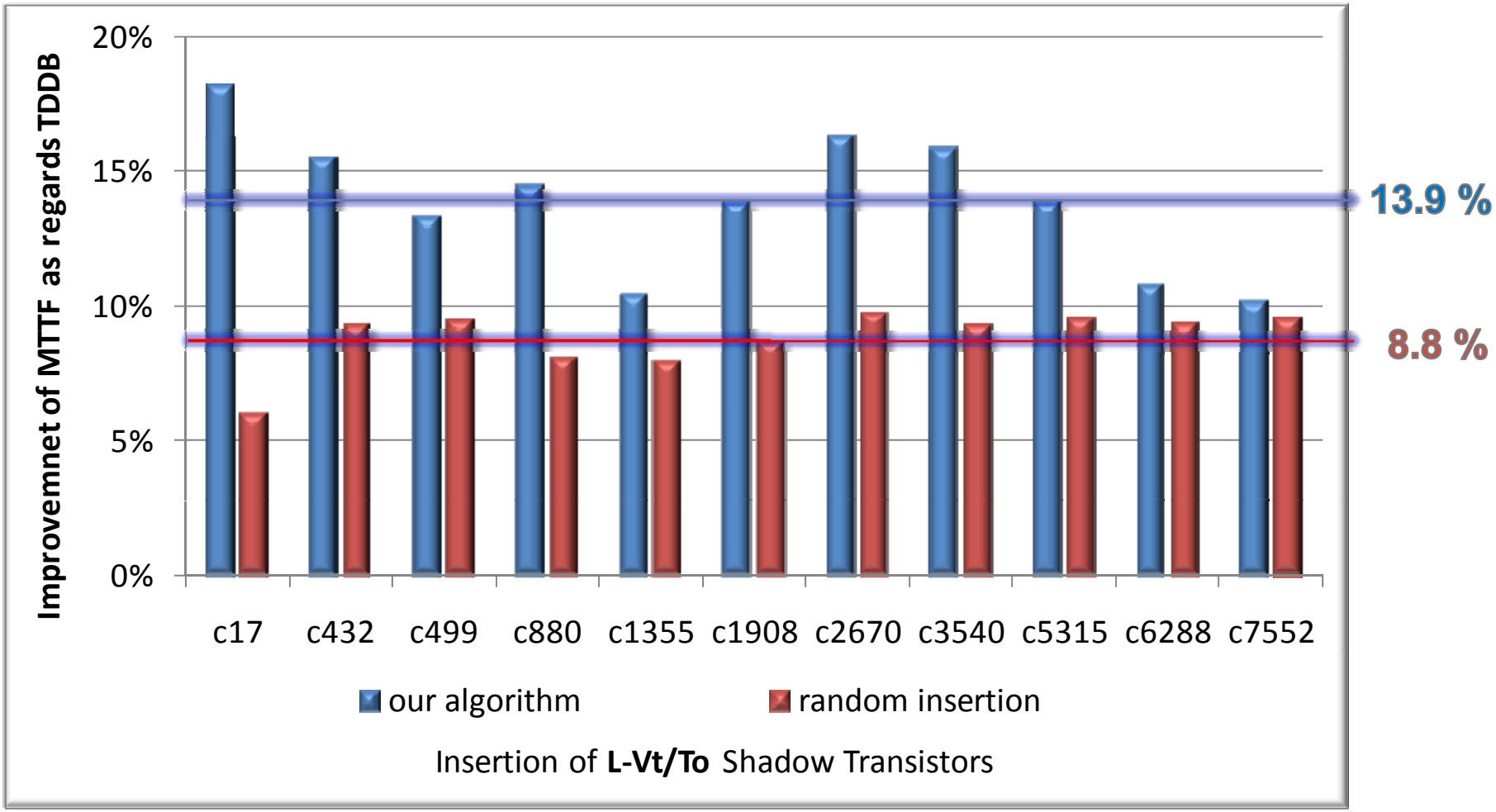
Algorithm



Results

Improvement MTTF (L-Vt/To)

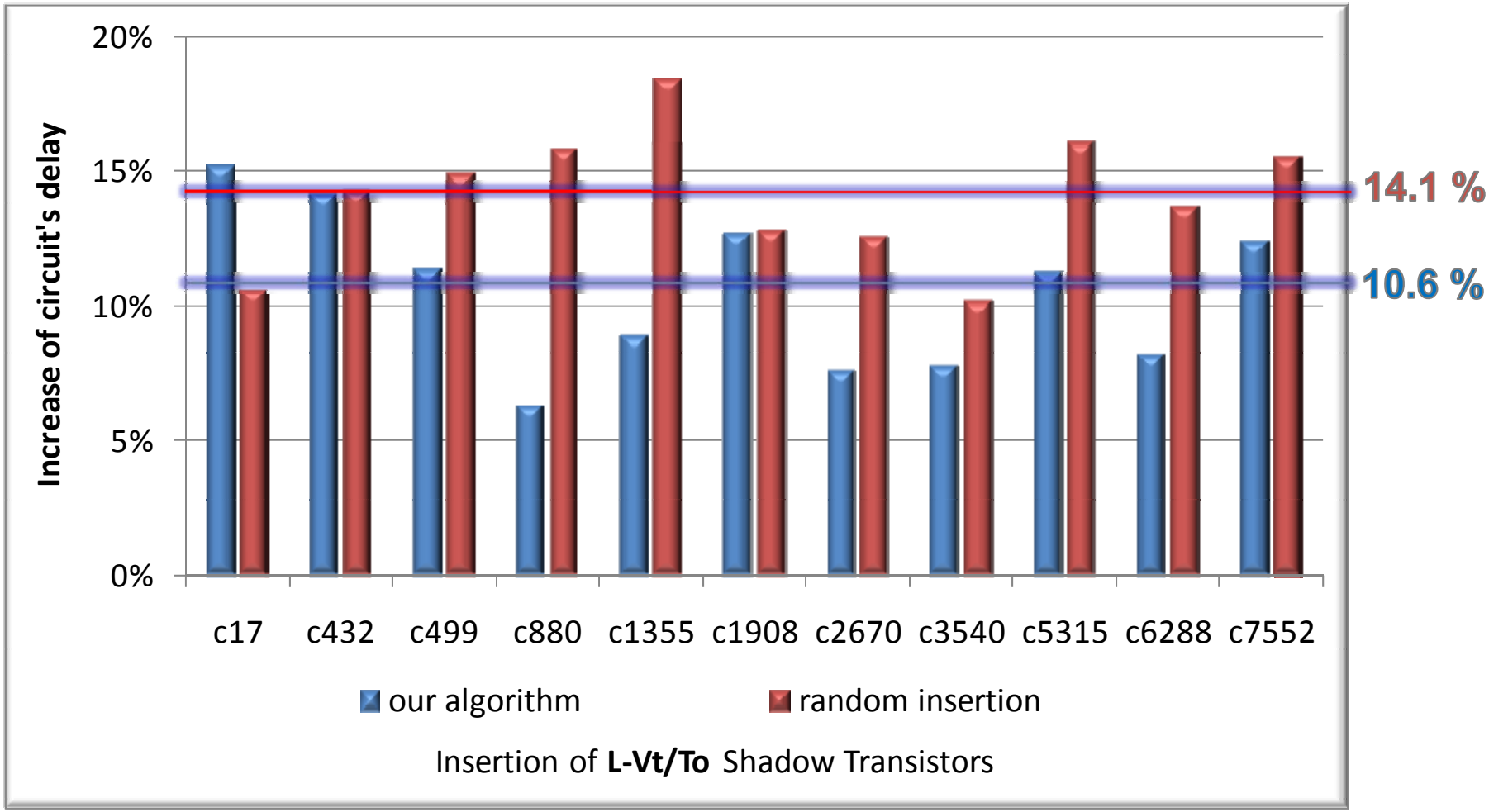
≈ 23 % additional transistors



Results

Performance Reduction (L-Vt/To)

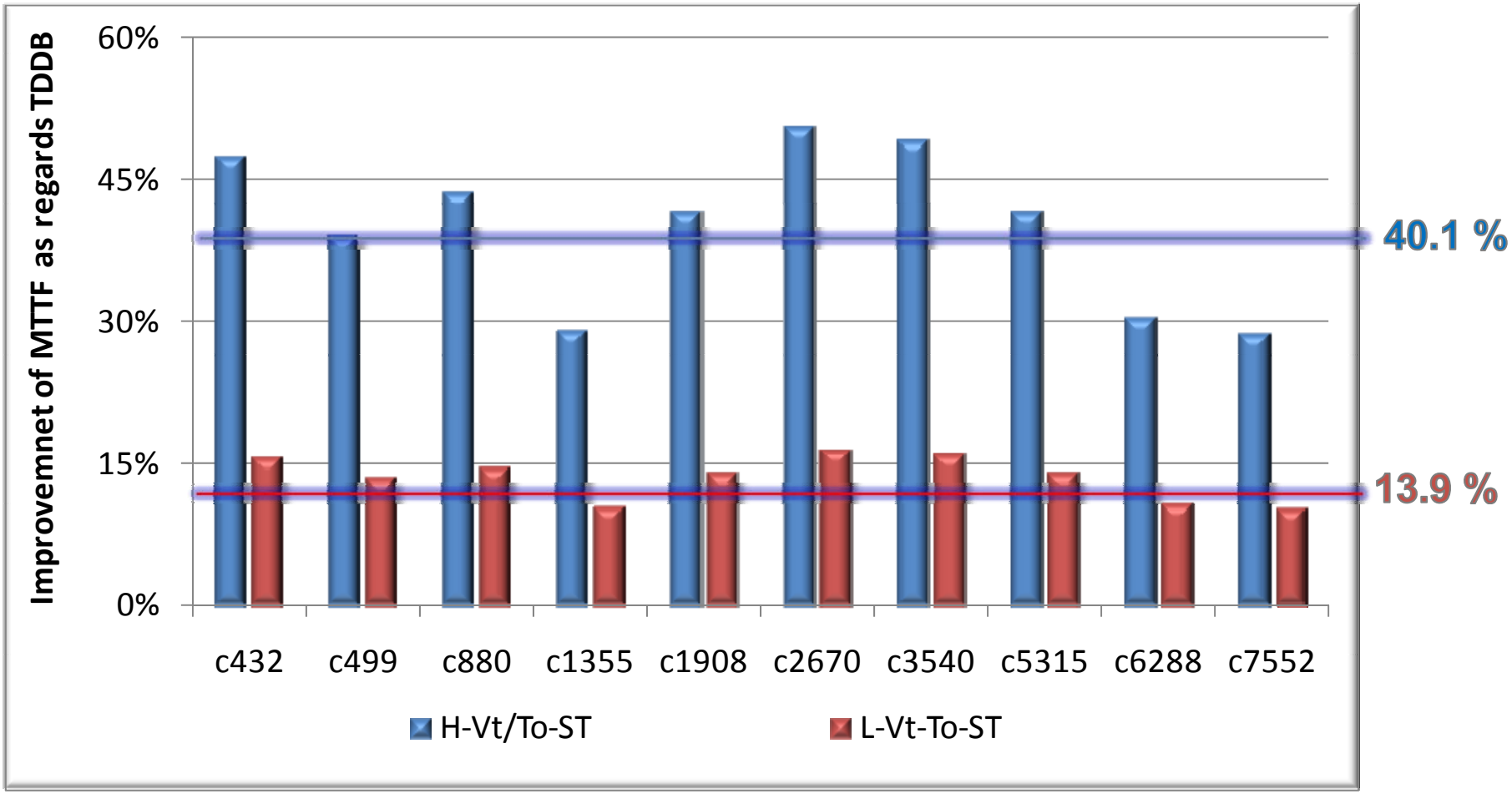
≈ 23 % additional transistors



Results

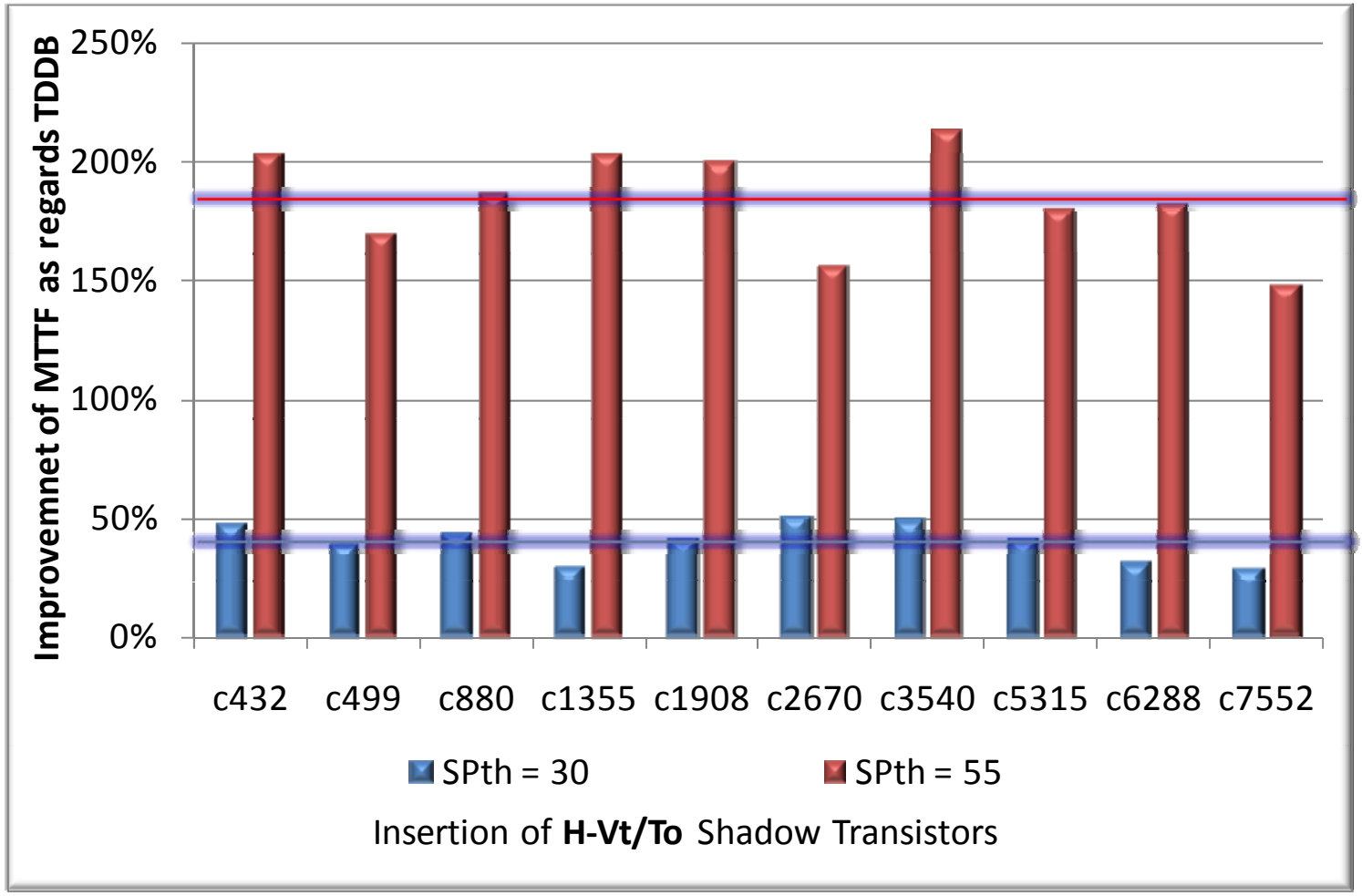
Application of H-Vt/To-ST

≈ 23 % additional transistors



Results

Modification of C_{crit}



Average:
MTTF: +183.7%
Delay: +20.2 %
P_{dyn}: +56.1 %
Trans: + 64.5 %

Average:
MTTF: +40.1 %
Delay: +10.1 %
P_{dyn}: +13.0 %
Trans: +22.0 %

Conclusion

- System reliability decreases with shrinking technologies and rising transistor count
- Increasing probability of Time-Dependent Dielectric Breakdown (TDDB)
- Insertion of Shadow Transistors (ST) increases system lifetime
- Remarkable improvements by application of transistors with thick gate-oxide
- Selective insertion of ST improves trade-off between reliability and performance
- Impact and amount of redundant transistors can be adapted by the threshold value SP_{th}

Thank you!

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