High-Level Simulations of On-Chip Networks

Claas Cornelius, Frank Sill, Dirk Timmermann

9th EUROMICRO Conference on Digital System Design (DSD)
- Architectures, Methods and Tools -

University of Rostock
Institute of Applied Microelectronics and Computer Engineering

Outline

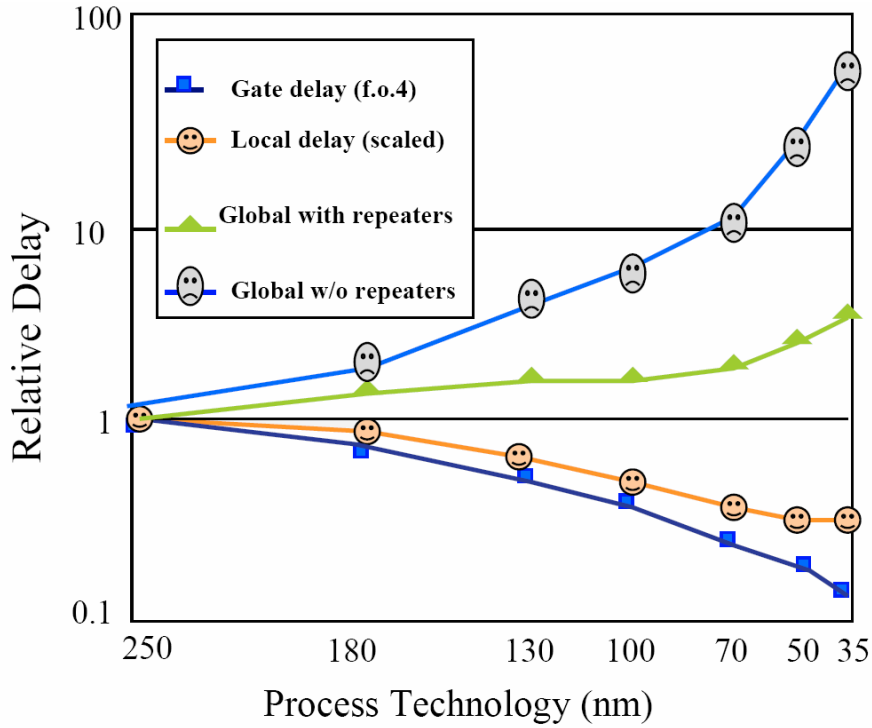
- Current situation
  - Development of technology
  - Bus-based system design
- Network-On-Chip (NOC)
- Simulator
  - Related work
  - Chosen approach
  - Integration into a design flow
- Preliminary results
  - Communication
  - System control/monitoring
- Outlook

Claas Cornelius, September 2006
Institute of Applied Microelectronics and Computer Engineering, University of Rostock

Current situation

Development of technology

- Power dissipation, leakage, power density
- Performance (frequency, MIPS)
- Interconnects
- Parameter variability
- Reliability
- Costs



[Tenhunen, 2005]

Requirements:

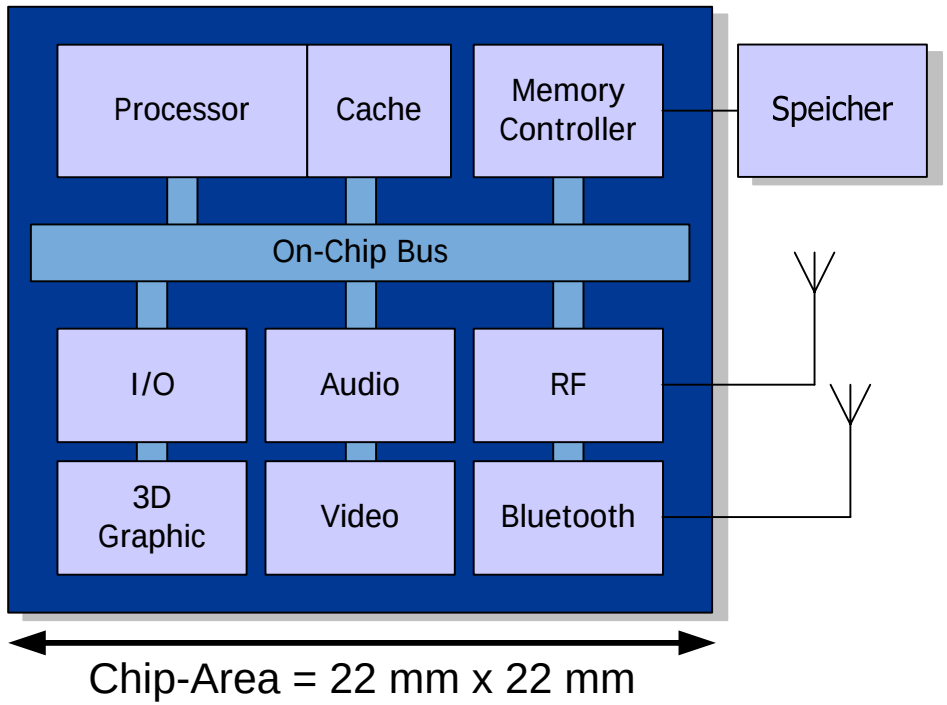
- More MIPS/mm²
- More MIPS/Watt

Current situation

Bus-based system design

- Shared communication medium

- Connected problems:
  - Synchronous design



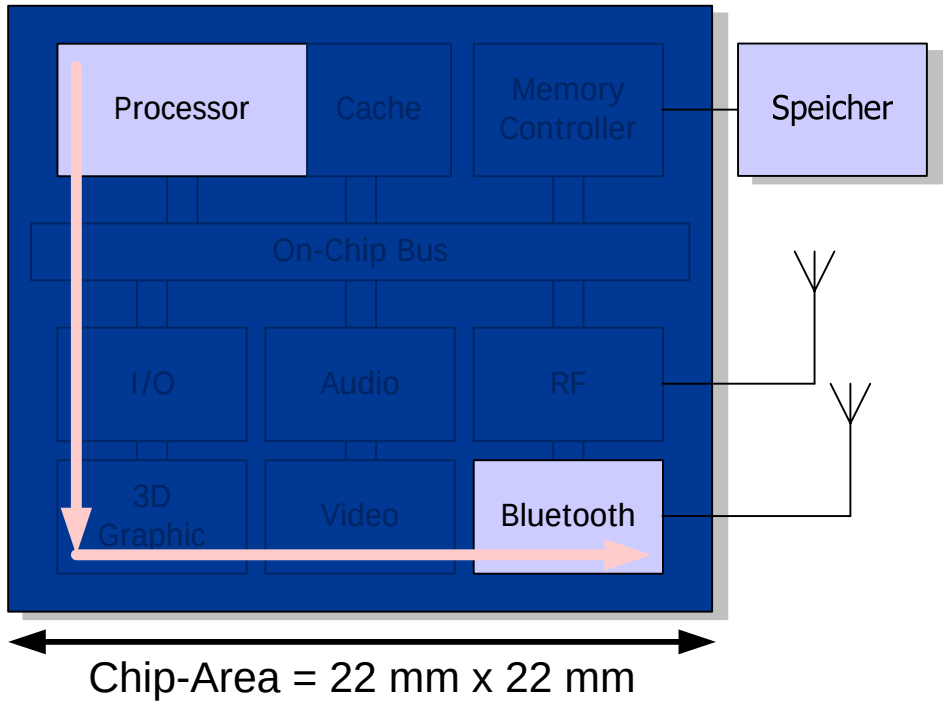
Claas Cornelius, September 2006
Institute of Applied Microelectronics and Computer Engineering, University of Rostock

Current situation

Bus-based system design

➔ Shared communication medium

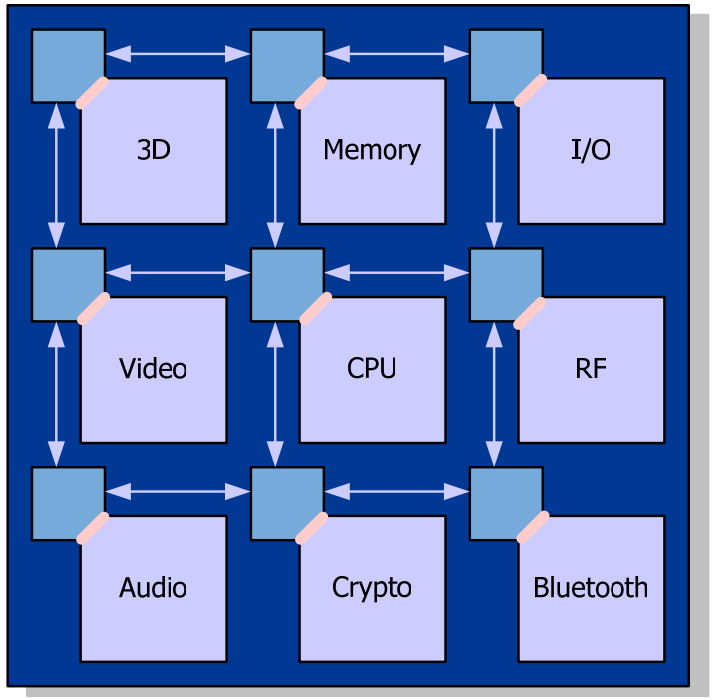
- Connected problems:
  - Synchronous design
  - Design-Productivity-Gap
  - Memory-Bottleneck
- Worsening the situation:
  - Chip-Size
  - Interconnects
  - Integration density
  - Parameter variability
  - ... and many more



Network-On-Chip (NOC)

- “Route packets, not wires” (W. Dally)
- “The network is the computer” (J. Gage)

- Promising properties:
  - Modularity
  - Encapsulation
  - Portability
  - Reuse
  - Scalability
  - Parallelism
  - ...



Change of Paradigms:

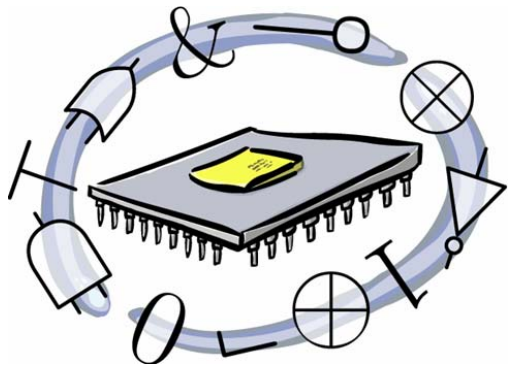
Computation → Communication

Computing-in-time → Computing-in-time-and-space

Claas Cornelius, September 2006
Institute of Applied Microelectronics and Computer Engineering, University of Rostock

Simulator

Related work

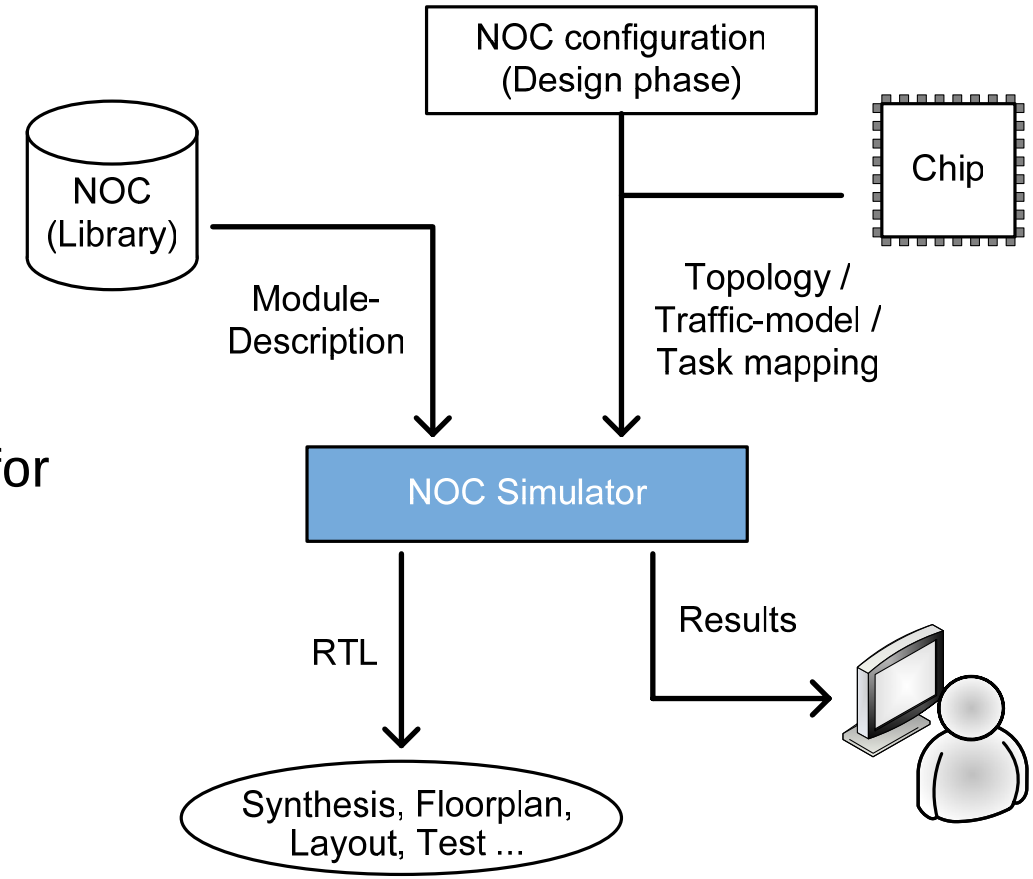


- Prototyping, Test-Chips
  - Star topology for multimedia applications [Lee, 2003]
  - 4x4 mesh network with traffic generators [Mullins, 2006]
- Parametrizable VHDL-model ported to FPGA [Zeferino, 2004]
- Emulation framework on an FPGA [Genko, 2005]
- High-level VHDL [Sigüenza, 2002]
- SystemC approach and design flow [Jalabert, 2004]
- Event-based C++ Simulator [Wiklund, 2004]

Claas Cornelius, September 2006
Institute of Applied Microelectronics and Computer Engineering, University of Rostock

Simulator

Chosen approach

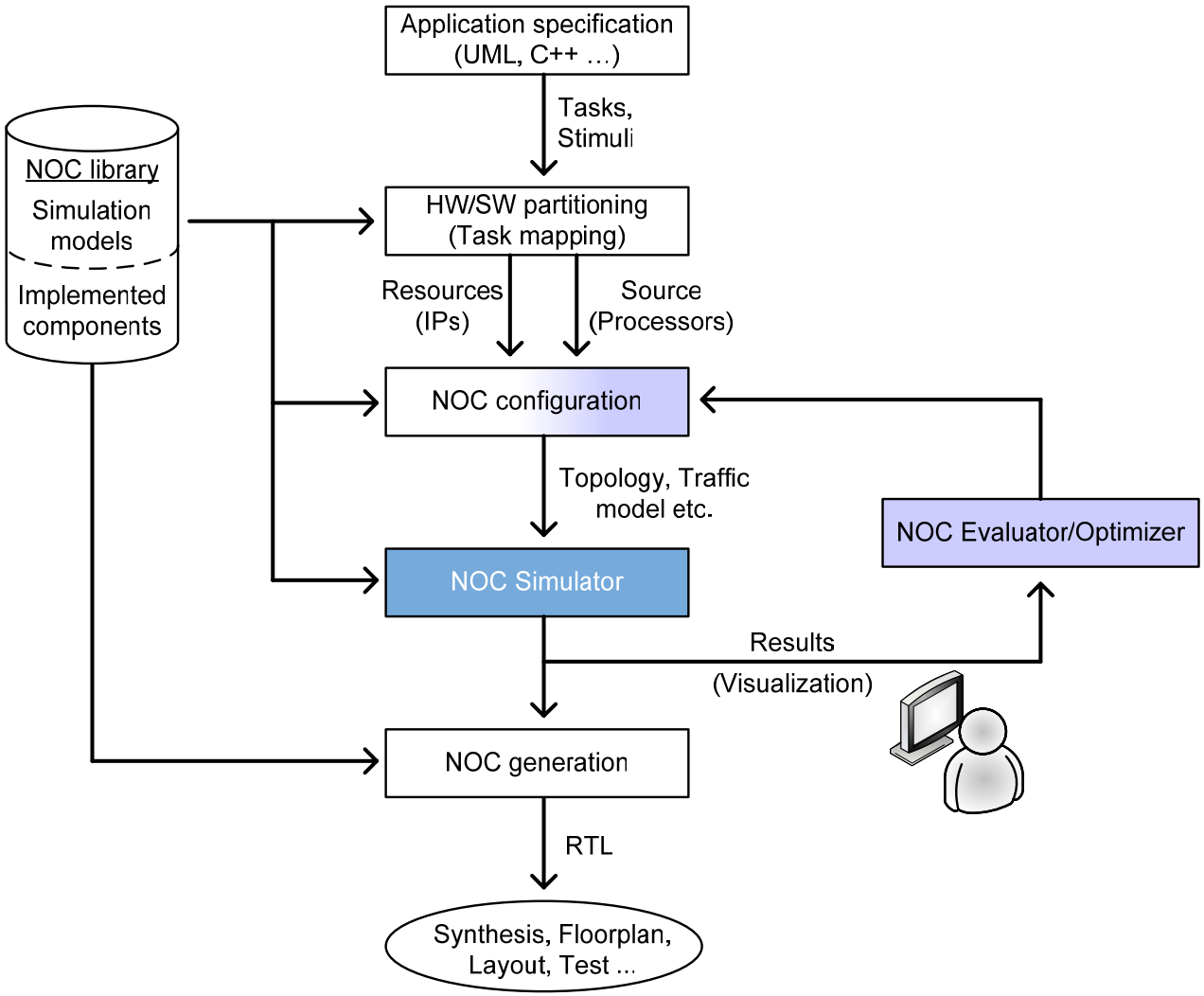


- Level of abstraction for System-Developers:
  - Modules
  - Logic-Gates
  - Transistors

Claas Cornelius, September 2006
Institute of Applied Microelectronics and Computer Engineering, University of Rostock

Simulator

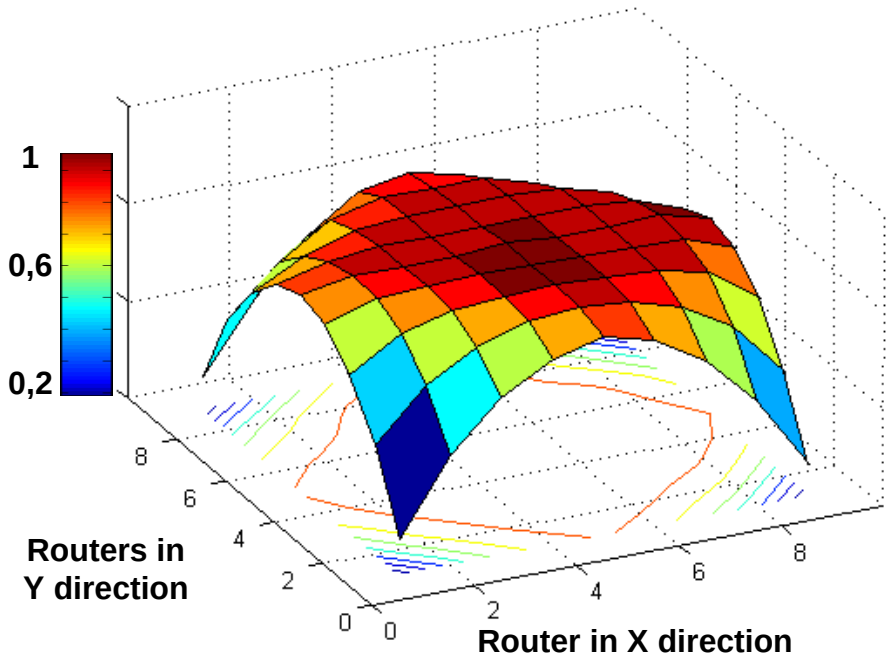
Integration into a design flow

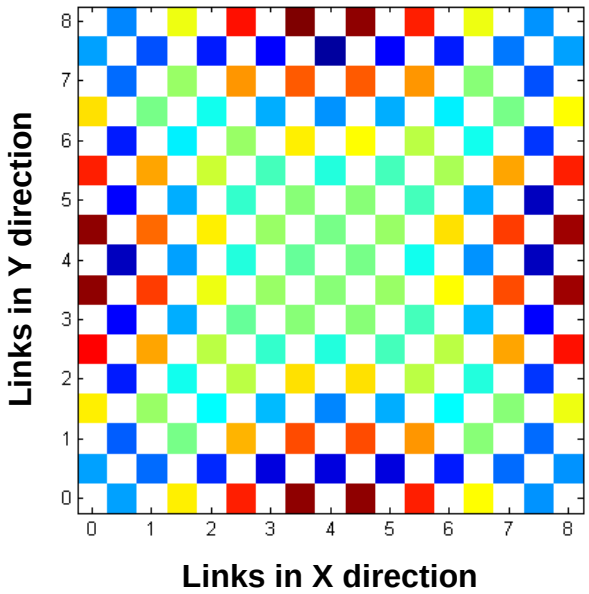


Preliminary results

Communication

- Network size
- Routing schemes
- Packet injection rate
- Packet congestion



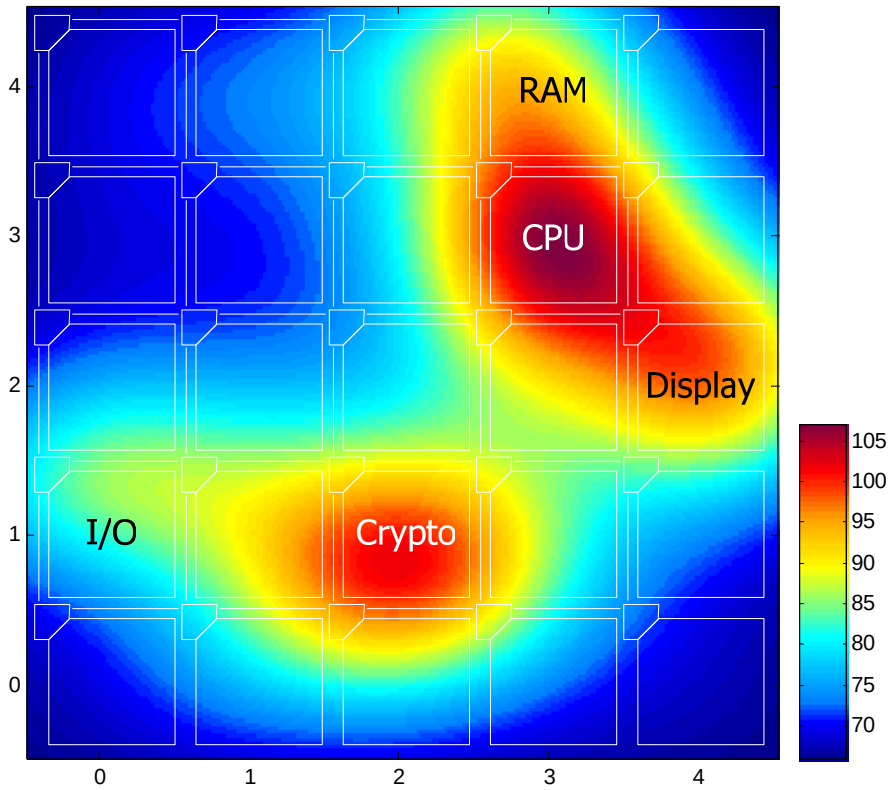


- Link implementation
- Link width
- Pipelining links

Preliminary results

System control / monitoring

- Dynamic power management
  - ➔ Power, supply voltage drop, and temperature
- Distribution of hot spots
  - ➔ Tasks, communication, and temperature
- Static, dynamic display



Application example for the temperature distribution of a 5x5 network

Outlook

Intended investigations / Open issues

- Operating system (centralized)
  System control (distributed)
  - Power, temperature
  - Communication-computation trade-offs
  - Hardware reconfiguration
  - Self-healing, Reliability
- Load balancing, task-mapping
- Composability of functions/tasks/services
- Exploitation of parallel structure
  - Programming models
  - Distributed memory
- Benchmarking
- Design-space exploration
- Test and verification