Noise Analysis of Integrated Bulk Current Sensors for Detection of Radiation Induced Soft Errors

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Abstract*— Current CMOS technologies show an increasing susceptibility to a rising amount of failure sources. This includes also radiation induced soft errors, which requires countermeasures on several design levels. Hereby, Bulk Built-In Current Sensors represent a promising approach on circuit level. However, it is expected that these circuits, like similar sensors measuring substrate effects, are strongly susceptible to substrate noise. The intention of this work is an in-depth noise analysis of representative bulk sensor based on extracted layout data. Thereby, several aspects are considered, like sensor activation thresholds, impact of the distance to the noise source, and noise generation by a test circuits. Results indicate that already rms values of 5 to 10 % of the supply voltage can lead to false detections and that these values are in the same order of magnitude as the noise generated by test circuits.

***Keywords*— Reliability; Noise, CMOS; VLSI; nanotechnology; Substrate model**

I. Introduction

The continuously downscaling of CMOS technologies leads to progress in nearly all areas of human society. It comes with a price, though. With the advancement of the technology nodes, new issues emerge which need to be overcome. This includes, for example, leakage currents due to short channel effects and tunneling. Another serious problem is gate oxide thickness as its traditional low value is leading to higher susceptibility to breakdown and consequent system failure [1].

Further, radiation induced particles, which have been a problem solely for avionics and aerospace environment and memories, are a rising concern for ground level applications and combinational logic [2]. This trend is based on the decreasing critical charge levels and supply voltages of the nanoscale integrated circuits realized. The resulting transition faults can lead to soft errors or even system crashes. Amongst the several strategies to detect this kind of effects, Bulk Built-In Current Sensors (BBICS) represent a promising approach [3]. Its advantages are a high sensibilities, fast response times and considerably increase in area and power consumption.

An additional challenge in integrated circuits is noise, which especially is critical in mixed-signal designs [4]. Due to diminishing voltage levels, increasing complexity, and steeper signals, though, also exclusive digital designs can be affected. Amongst the several noise sources, circuits with high switching activity, step signal slopes, and high complexity have a dominant role and should lead to a noise analysis of the design [5].

It is expected that sensors that measure substrate effects, like the mentioned BBICS, DEPFET sensors [6] or bulk pixel sensors [7], show a high susceptibility to noise. To our best knowledge, though, there is no published research done on noise analysis of integrated substrate sensors. Consequently, the intention of this work is the exploration of the noise susceptibility of integrated nanoscale circuits for bulk current measurements.

The rest of the work is structured as follows. Section II gives preliminary information, while section III explores the noise generation. The following section IV presents the executed experiments and discusses the results. Finally, section V concludes this paper.

II. Theoretical Background

A. Substrate modeling

In order to analyze the effects of the substrate parasitic, an appropriate model is required. Such a model consists of interconnected electrical components, which values are obtained from its composition and geometry.

This can be achieved by using the FEM (Finite Element Method) approach, which is the chosen method for this work. Hereby, the substrate is discretized into cubes, which center is considered as a node, and all the six faces, other six distinct nodes (see Fig. 1). From the central node to each cube face, there is a resistance and a capacitance connected in parallel, being values dependent on the dimensions of the cuboid and the electrical characteristics of the material. The means to calculate these is solving Gauss's law and applying the divergence theorem [5]. The reconstitution of the entire substrate is accomplished by interconnecting the appropriate nodes, obeying the spatial disposition of each element.

Finite Element Method provides a three dimensional modeling of the entire substrate. However, in order to obtain satisfactory modeling resolution, the computational time can easily reach impractical values. Consequently, a technique of fine discretization of heterogeneous areas (usually closer to the surface) and a coarser discretization of more homogeneous ones (deepest regions) are used to reduce de computational cost [5].

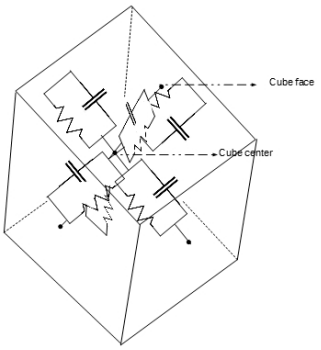

Fig. 1. Discrete element for substrate modeling.

Another approach is the Boundary Element Method (BEM), which realizes a discretization of selected structures, e.g. the contacts, well and substrate taps as well as diffusion regions [8]. Those structures are two dimensional, thus, BEM provides a 2-D substrate model, comprising only regions of the substrate surface. Although BEM provides computational efficiency, it cannot model deepest substrate characteristics [3].

B. Noise modeling

An in-depth noise analysis requires the modeling of different kinds of noise. In VLSI circuits, one can find essentially three kinds of noise: Thermal Noise, Shot Noise and Flicker Noise [5].

Thermal noise, as the name states, occurs due to inherent crystalline structure agitation of the material, which causes charge carriers in the conduction band to move randomly. Its realization in time is modeled by the Normal Distribution, and since its Power Spectral Density (PSD) shows ideally the same power density for all frequency bands, it is so-called white noise. Hence, thermal noise should be modeled as White Gaussian Noise (WGN) [9].

Shot noise is caused by temperature, too. However, its physical mechanism is different from thermal noise. A hole-electron pair is generated by temperature excitation, i.e. the electron at the valence band acquires energy and is then moved to the conduction band. This kind of noise is also white noise, although not necessarily Gaussian. Nevertheless, it can be modeled as such, and thus, shot noise is modeled in this work as WGN, too.

Since both Thermal and Shot Noise are WGN, they can be represented by just one Normal Distribution realization, with following variance v_{WGN}:

$$v_{WGN} = v_{thermal}^2 + v_{shot}^2$$

with $v_{thermal}$ means the variance of the "thermal noise", while v_{shot} represents the variance of the "shot noise". The mean of the applied noise, and thus of its components, is zero [4].

Flicker noise (also known as 1/f noise or pink noise) is a yet not fully understood phenomenon [9]. However, it is known to be present in VLSI circuits and to have a PSD that decreases with increasing frequency. Given that Flicker Noise actuates stronger at low frequencies, one can conclude that its power spectrum constitutes the WGN power spectrum, i.e. WGN is a more general type of noise. Hence, a signal that behaves like flicker noise can be filtered from WGN, which is the approach applied in this work.

C. Soft errors

As stated in the introduction, soft errors can cause system failure or information falsification. Those errors can be called Single Event Upsets (SEUs) or Single Event Transients (SETs), depending on its nature. Both are caused by energetic particles that strike the integrated circuits and form high levels of charge carrier generation through p-n junctions, which are then briefly short circuited [2].

SEUs are digital signal falsifications that change the signal state in memory elements such as flip-flops or latches, and consequently, affecting sequential logic. In contrast, SETs are perturbations that change a signal for a short time before it returns to its original state. If the effect of such perturbation reaches an enabled memory element it will cause incorrect behavior [3].

The mentioned carrier pair generation by particle strike is modeled by a rapidly increasing exponential current, followed by a decreasing exponential characteristic [3].

D. Modular Bulk Built-In Current Sensors

Built-In Current Sensors (BICS) are an efficient mechanism to detect permanent faults and SEU in CMOS circuits during its quiescent state, i.e. when the circuit is not switching [10]. However, this method is not applicable for detection of SET, as the amplitude of transient currents induced by radiation can have the same order of currents normally generated by switching activities in combinational logic circuits [11]. As alternative have been proposed Bulk Built-In Current Sensors (BBICS) that measure the anomalous currents that flow through the junction between a bulk and a reversely biased drain of a disturbed transistor [3][12][13].

Amongst the several implementations, the modular Bulk BICS (mBBICS) represents a promising trade-off between sensibility, response time, robustness, and area offset [14]. Further, its basic concept is similar to other BBICS. Hence, it was chosen as representative circuit.

The mBBICS is composed by two functional blocks: the head and the tail (see Fig. 2). The head circuits are connected to the bulk of the monitored transistors, while the tail circuit latches the output signal of several head circuits. In detail, the drain of transistor N_{h1} is connected to the bulk of the monitored transistors, its source is at GND, and its gate connected to VDD. In normal operation, the drain of N_{h1} acts as a virtual GND while the drain of N_{h2} is at VDD level. In the event of a strike, the fault current is conducted through N_{h1}. The consequent voltage drop increases the gate voltage of N_{h2}, which is switched on and pulls down the signal $head_{NMOS}$ that is connected to the drain of N_{h2} and the input of the tail circuit. The latter latches the input and actives the error flag. The circuit remains in that state, until the reset transistor is activated, causing the circuit to go to initial state and be ready

for another detection [14]. For sake of simplicity, we concentrate solely on the NMOS version and omit the complementary mBBICS for monitoring PMOS bulks.

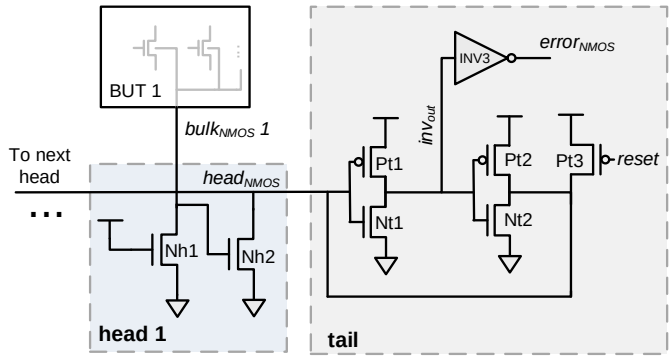

Fig. 2. Structure of a modular Bulk-BICS

III. NOISE AND FAULT INJECTION

A. Substrate extraction

The substrate extraction leads to a network of capacitors and resistors. Thereby, the rules that drive the modeling workflow depend on the process characteristics and doping profiles [15]. The resulting circuit is connected to the system itself by tie devices, i.e. the network corresponding to the substrate has as many terminals as there are different taps in the layout. Further, the frequency of the signal being processed by the circuit determines how the substrate will be modeled. Thus, it is important to determine the AC response of the resulting substrate network and assure that the chosen input signal has only frequencies that can be handled by the extracted network.

B. Substrate probing strategy

Since the substrate is not a perfect conductor, signals generated by the operation of a circuit that influence current and voltage levels at the transistor bulks are conducted through the substrate network. Moreover, the very noise that is present in transistor bodies traverses such a grid.

Fortunately, as already presented, it is possible for the designer to estimate the equivalent circuit that represents the substrate. Hence, one can simulate and predict the behavior of substrate injected noise throughout the substrate, analyzing the signal by measuring it at different distances from the noise source, e.g. a digital circuit operating heavily and at high switching frequency.

The extracted substrate network provides an access terminal for each tap or group of connected taps. The analysis of the noise magnitude in different regions can then be done by placing an outtake tap in a set of regions, extracting the substrate and simulating it. The farther the tap is placed from the source circuit, the larger the area that composes the layout becomes. As a consequence, the substrate equivalent circuit becomes bigger, with more components and interconnections, and it is expected that noise will be attenuated with increasing distance.

C. Noise generation and injection

Noise is constantly present in real electrical circuits and has to be considered by the designer. There are different ways to introduce noise in a circuit. One way of analyzing noise is to generate its waveform and inject it in the circuit by using voltage or current sources. Even though this is only a simplified model of real noise profiles, this method is appropriate for a general analysis of noise susceptibility of integrated circuits.

Referring back to the theoretical background, the three common forms of noise in VLSI circuits are thermal, shot and flicker noise [5]. Both thermal and shot noise can be modeled as WGN. To generate a signal with WGN characteristics, one could make successive realizations of a Gaussian random variable, and multiply the resulting signal by a scaling factor. Flicker noise can be obtained by filtering white noise by a low pass.

An important choice to be made is the number of random variable sampling to be executed in conjunction with the overall duration time. Since the signal is discrete, it will have a sampling rate, thus, a frequency up to which the simulation will provide true results. Theoretically, considering the Nyquist Theorem, a sampling rate equal to the doubled maximum signal frequency must be achieved to correctly predict the system behavior.

IV. SIMULATION AND RESULTS

A. Simulation environment

In order to realize an in-depth analysis of the noise robustness of the mBBICS, it was necessary to design and execute the extraction of the circuit layout. Therefore, the transistor level representation of the mBBICS circuit was realized, including appropriate transistor sizing and verification. Hereby, a predictive 90 nm process development kit with a VDD of 1.2 V has been applied [16]. This was followed by the layout design (see Fig. 3) and its extraction.

The results presented in this work are those obtained from the layout extracted netlist, including the substrate parasitics. A notably advantage of this method in comparison to solely schematic based analysis is the consideration of not only components, but also interconnects dimensions and physical constitution. In this case, the substrate as a network of undesired components is additionally included.

Two noise waveforms were applied to stimulate the input of the sensor that is connected to the bulk of the monitored transistors. One noise was WGN, generated from the realization of a Normal distributed random variable with zero mean and variance equal to one, corresponding to thermal and shot noise. The second noise was the result of the WGN subjected to a low pass filter, yielding the so-called flicker noise. Both waveforms were multiplied by an iteratively adjusted factor in order to adapt the rms value. The duration of each simulation was set to 1 µs.

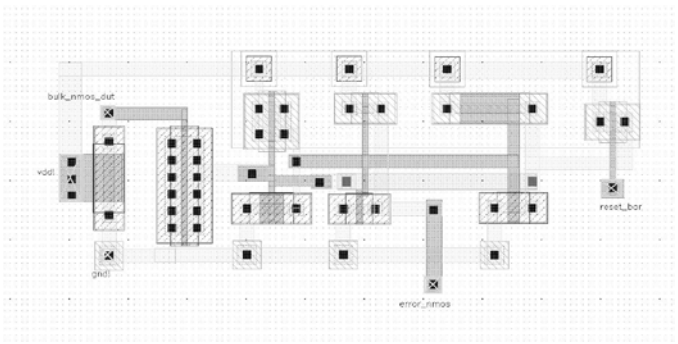

Fig. 3. Layout of the NMOS mBBICS

B. *Noise based Sensor Activation Analysis*

In a first attempt have been determined the level of the rms voltage V_{rms} of the noise on the bulk that lead to an activation of the sensors, i.e. to an undesirable false detection.

Fig. 4 and Fig. 5 summarize the results of this analysis for the NMOS and PMOS versions of the implemented mBBICS. Hereby, W means WGN, F means flicker noise, V indicates that the noise was input to the circuit as voltage, and C as current. As example, FC stands for flicker noise input as a current signal.

It can be concluded that the sensors are most susceptible to White Gaussian voltage Noise, while flicker voltage noise requires the highest rms value to activate the sensor. Further, it can be seen that the noise sensibility of both types of mBBICS is similar.

C. *Distance Analysis*

In the next step has been analyzed the behavior of conducted noise for different locations of the noise source in the substrate. The analysis was done for WGN, inserted as voltage, and the NMOS version of mBBICS.

Two substrate ties were added to the layout. One of them

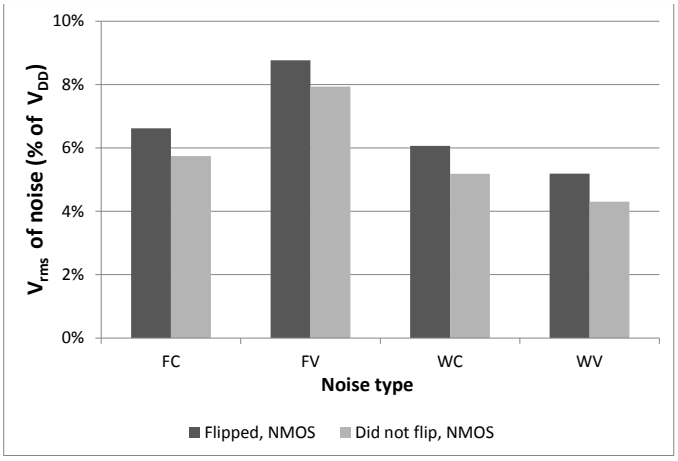

Fig. 4. Flag activation of mBBICS (NMOS version) depending on rms value of noise signal

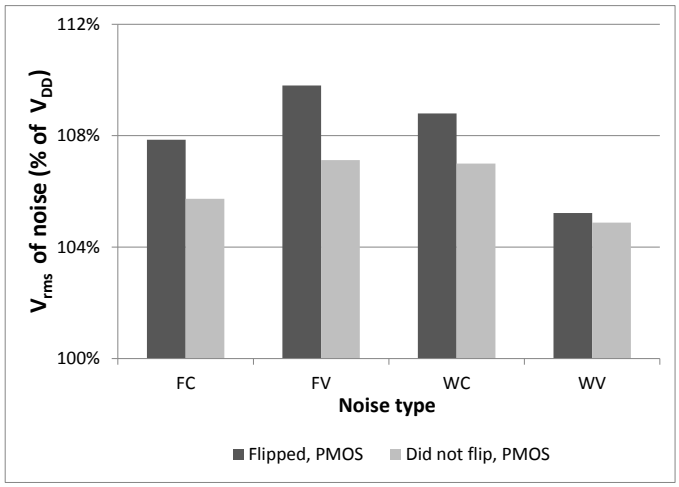

Fig. 5. Flag activation of mBBICS (PMOS version) depending on rms value of noise signal

was placed 100 nm afar from transistor N_{h1} (see Fig. 1) in order to measure the noise signal that enters the mBBICS. The second tie was placed in a number of different distances. The rms value of the input signal of the distant substrate tie was increased until the rms value that reached the tie close to the sensor was similar to the rms values that activate the sensor (see Fig. 4).

As expected, the noise rms value diminishes with increasing distance, i.e. it is attenuated by the substrate network (see Fig. 6). The results indicate further that the increase of the attenuation of the noise is stronger if the noise is originated near the circuit. With logarithmically increasing distances, the relative change of the attenuation diminishes. For long enough distances, such as 10 mm, virtually the entire signal is attenuated. Further, for distances more than 100 µm the required rms value to activate the sensor was higher than $V_{DD}/2$, which is rather unlikely value for noise in integrated circuits [5].

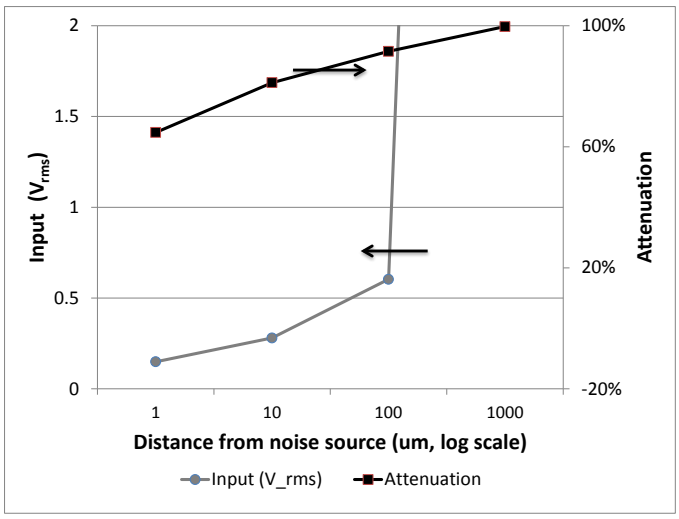

Fig. 6. Noise measurements at different distances from the source.

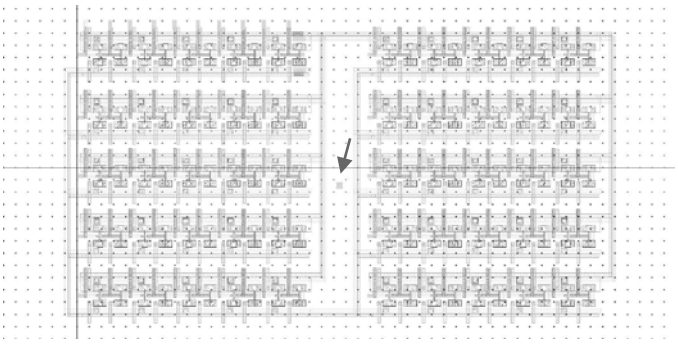

Fig. 7. Layout of inverter chains and measure tap in the middle.

The size of the minimum inverter of the applied technology is ca. 1μm^2 [16]. Hence, it can be concluded that noise sources that are located in the range of tenths to hundreds times of the size of a minimum inverter can be ignored for the noise analysis.

D. Noise generation by digital test circuit

The final analysis focused on the generation of real noise in the applied technology. In order to simulate realistic noise profiles, a digital circuit with high switching frequency was designed and set in operation. The circuit consists of ten inverter chains, each one operating at 5 GHz and with different phase shifts. Each inverter chain is composed by ten inverters (see Fig. 7). While switching, these chains generate an undesired signal in the substrate. The noise measurement was done in the same way as before by a substrate tie that was placed in the middle of the circuit (see Fig. 7).

Fig. 8 depicts the measure noise signal, while Fig. 9 shows the spectrum of the signal. The rms value of the generated noise is 14.6 mV, i.e. 1.2 % of V_{DD}. Thus, the generated noise did not activate the sensors. Nevertheless, generated noise and determined flag activation thresholds have the same magnitude order (see Fig. 4), and thus, noise must not be neglected at design time.

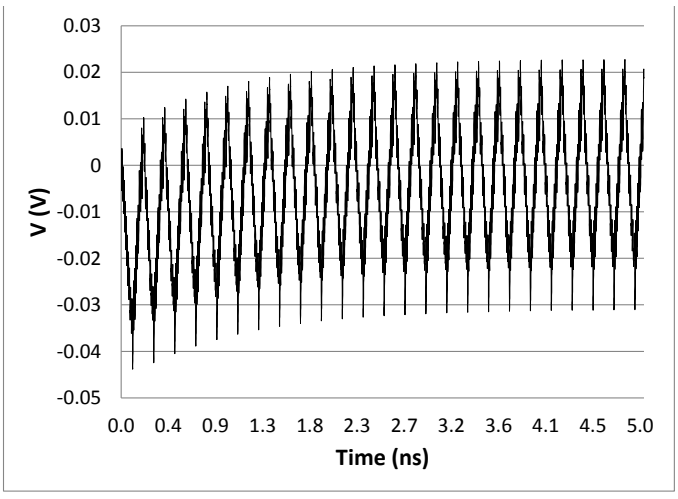

Fig. 8. Noise generated by digital test circuit

The spectrum of the generated noise (see Fig. 9) has a low pass characteristic, thus reinforcing the theoretical information of the presence of low frequency dominant noise, such as flicker noise. The peak at 5 GHz denotes the circuit operating frequency.

V. Conclusions

The increasing amount of noise source in current designs requires a detailed analysis of noise susceptibility of integrated circuits. This is all the more important for analog sensors measuring substrate effects.

This work presents the investigation of the noise tolerance of modular Bulk Built-In Current Sensors for detection of radiation induced transient faults. The analysis is based on extracted layout data, including the substrate profile and different kind of generic noise sources. The results indicate that noise sources close to the sensors lead to false detections if the rms value is in the range of 5 % of V_{DD} (White Gaussian Noise) to 10 % of V_{DD} (Flicker Noise). Further, it could be determined that noise sources with distances corresponding to the size of more than 100 minimum inverters can be disregarded. Finally, it could be indicated that noise generated by digital activity has comparable order of magnitude in relation to the activation values presented. Therefore, such a noise can induce false detection in the sensor circuit if not properly engineered.

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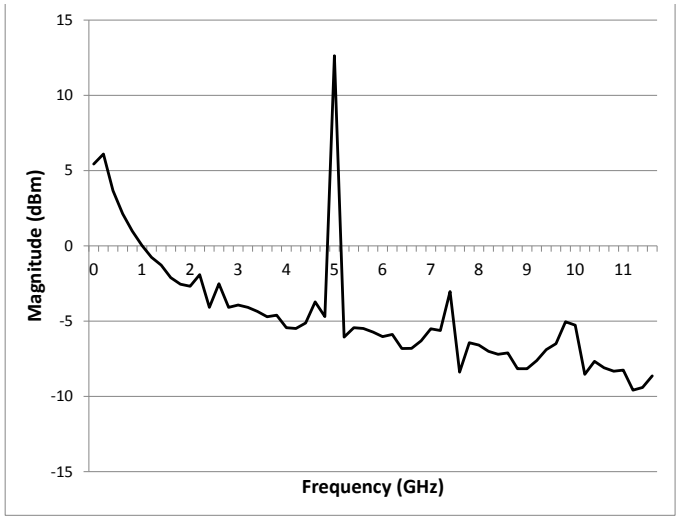

Fig. 9. Spectrum of the noise generated by digital test circuit

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