CHIP IN ARACAJU 2014
ARACAJU - SERGIPE - BRAZIL - SEPTEMBER 1ST TO 5TH, 2014

CLEVER: **C**ross-**L**ayer **E**rror **V**erification **E**valuation and **R**eporting

Rafael Kioji Vivas Maeda, Frank Sill Torres

Federal University of Minas Gerais (UFMG)

School of Engineering

Belo Horizonte, Brazil

FAPEMIG PRPQ PRÓ-REITORIA DE PESQUISA CNPq UFMG

Focus / Principal idea:

System Health Management approach for

Embedded Systems / SoCs

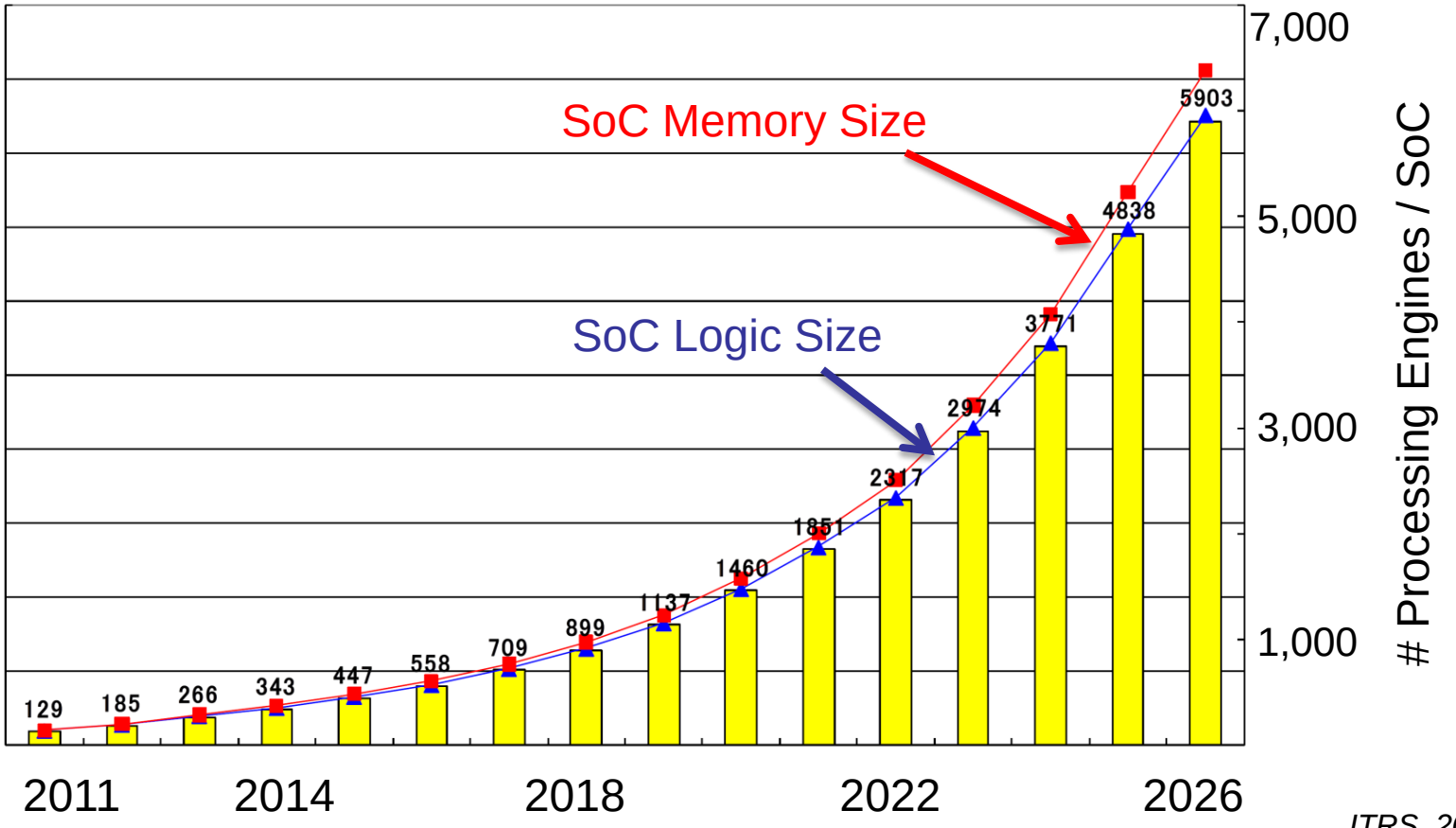
Outline

1. Motivation
2. Preliminaries
3. CLEVER
4. Verification Environment
5. Conclusion

Motivation

System Complexity

- Rising complexity of Embedded Systems / Systems-on-Chip (SoC)

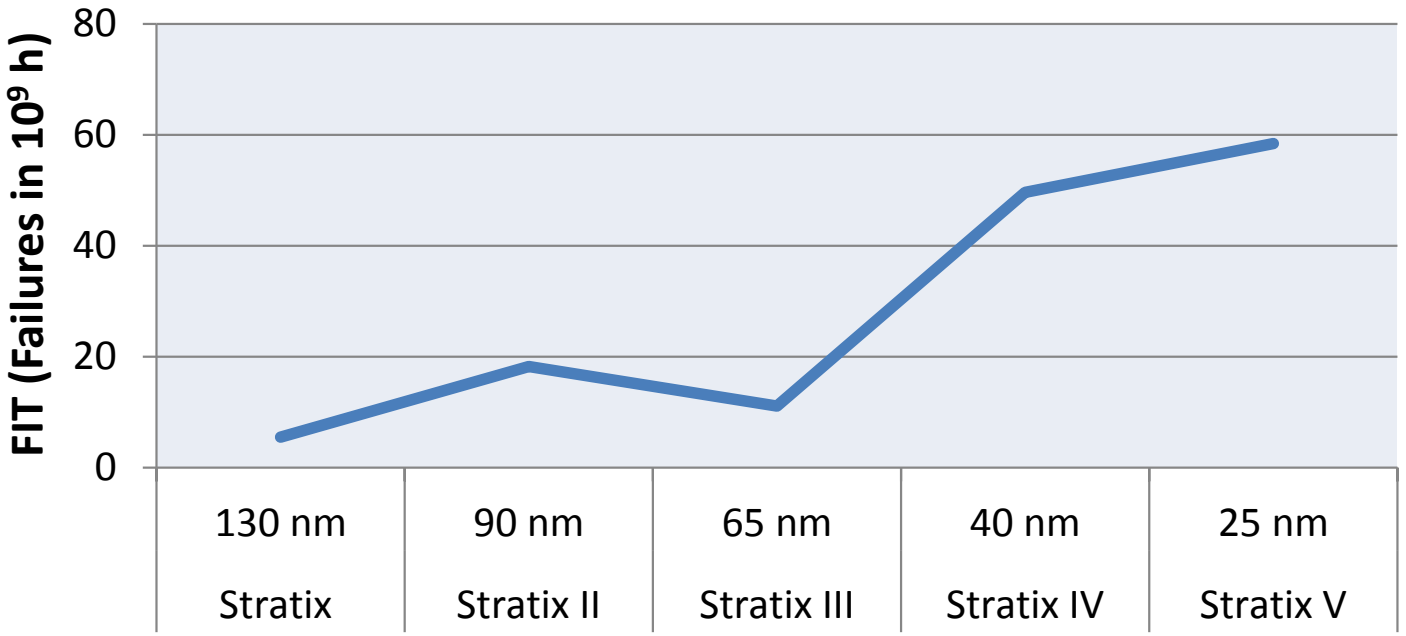


ITRS, 2013

Motivation

Faults

- Due to technology scaling considerable increase of:
  - Temporary faults
  - Aging and permanent faults

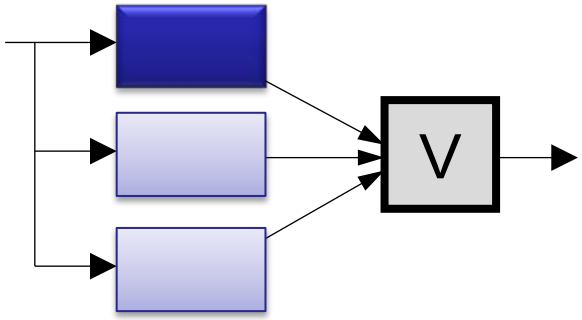


Altera, RELIABILITY REPORT 56, 2013

Preliminaries

Reliability

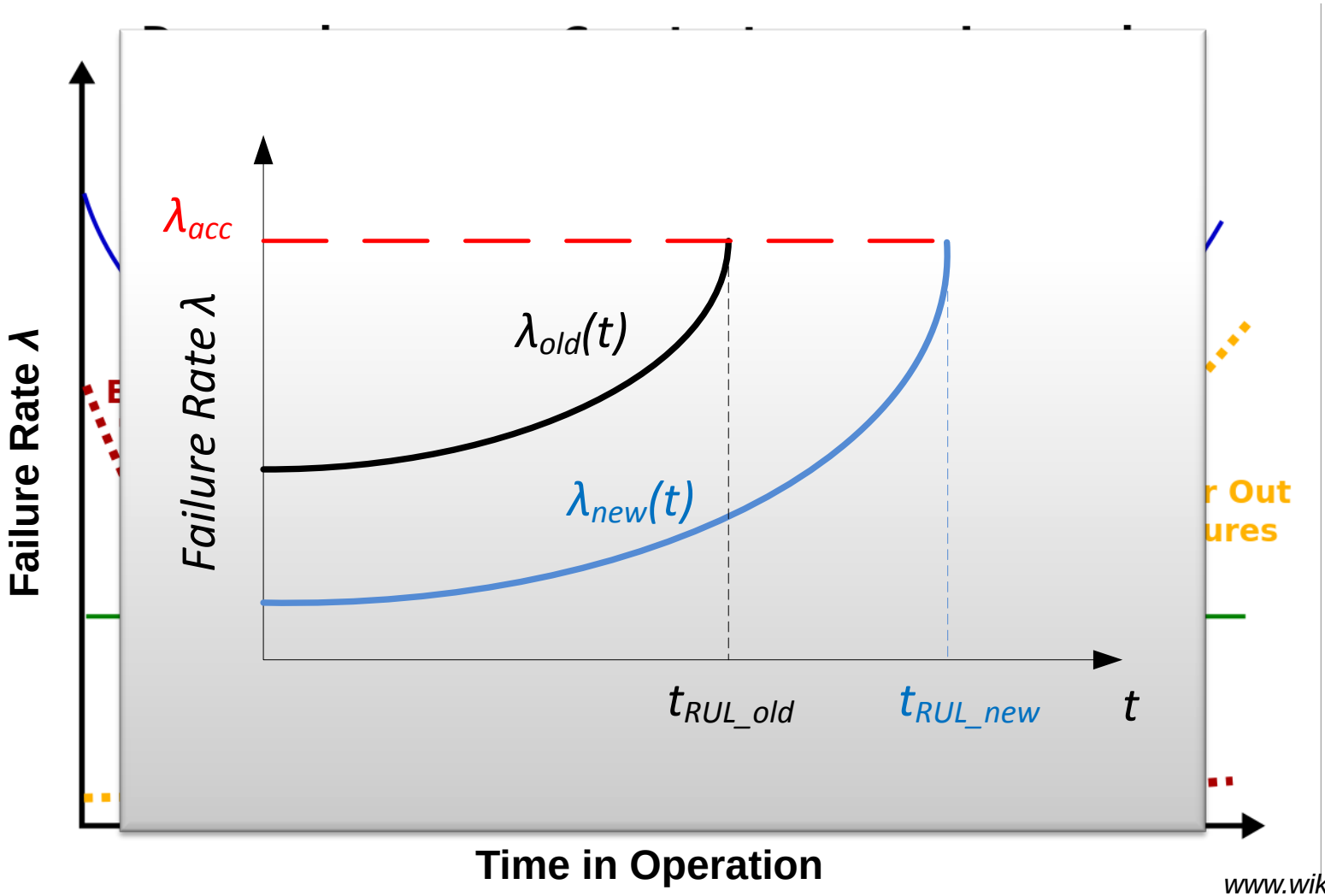
- Technique classification
  - Avoidance (e.g.: Triple Modular Redundancy)
  - Detection and Recovery (e.g.: Rollback)
  - Prediction (e.g.: PHM, S.M.A.R.T)



- Prognostics and Health Management (PHM)
  - Runtime monitoring
  - Remaining Useful Liftetime (RUL) estimation and extension

Preliminaries

Remaining Usefile Lifetime (RUL)



www.wikipedia.com

CLEVER

Origination of Approach

- **Prediction** of possible **system failure** important for future **SoC**
- **Limited effectiveness** and efficiency of **single layer** solutions
- **Straightforward** system **integration** required

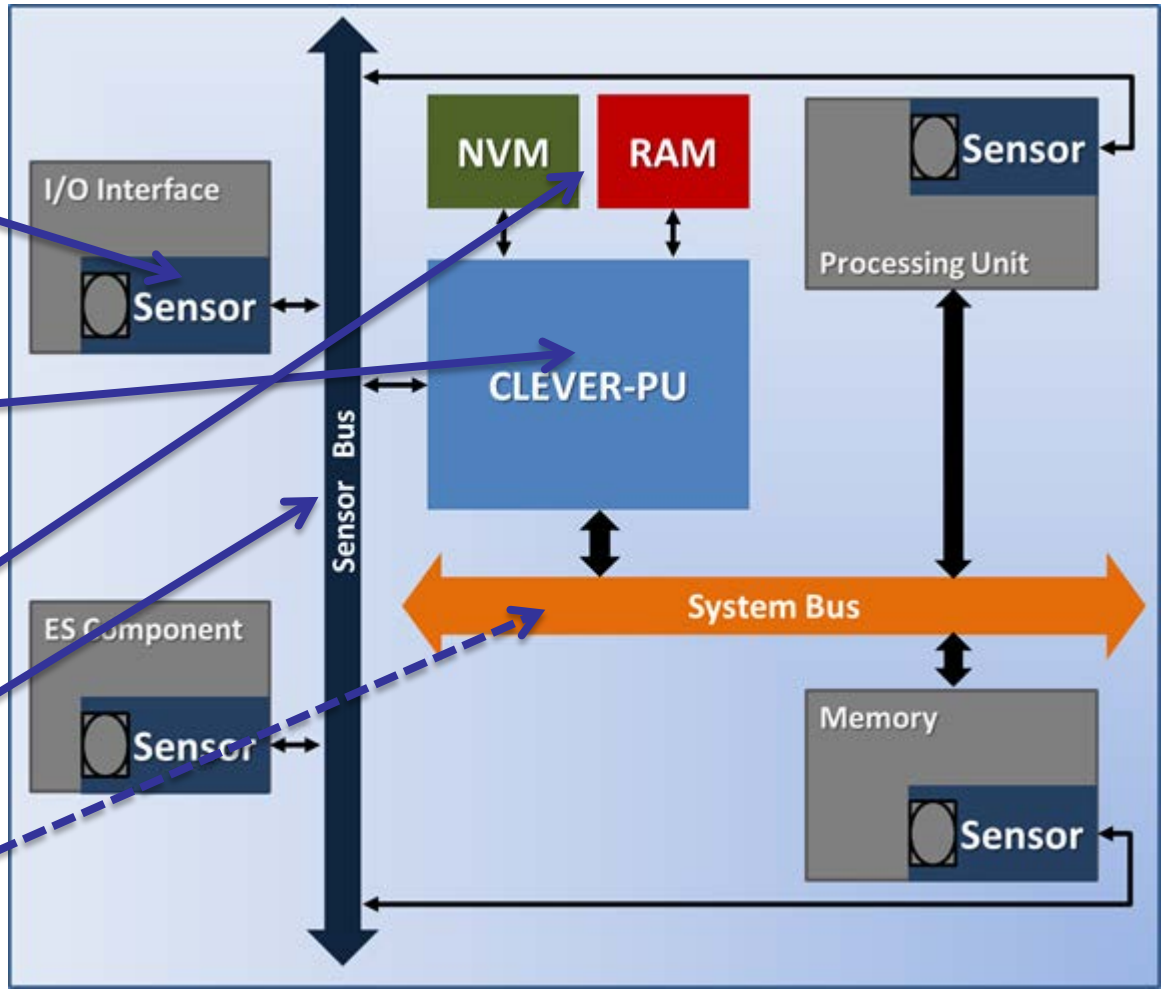
CLEVER

- **C**ross-**L**ayer
- **E**rror **V**erification
- **E**valuation and
- **R**eporting

CLEVER

Architecture

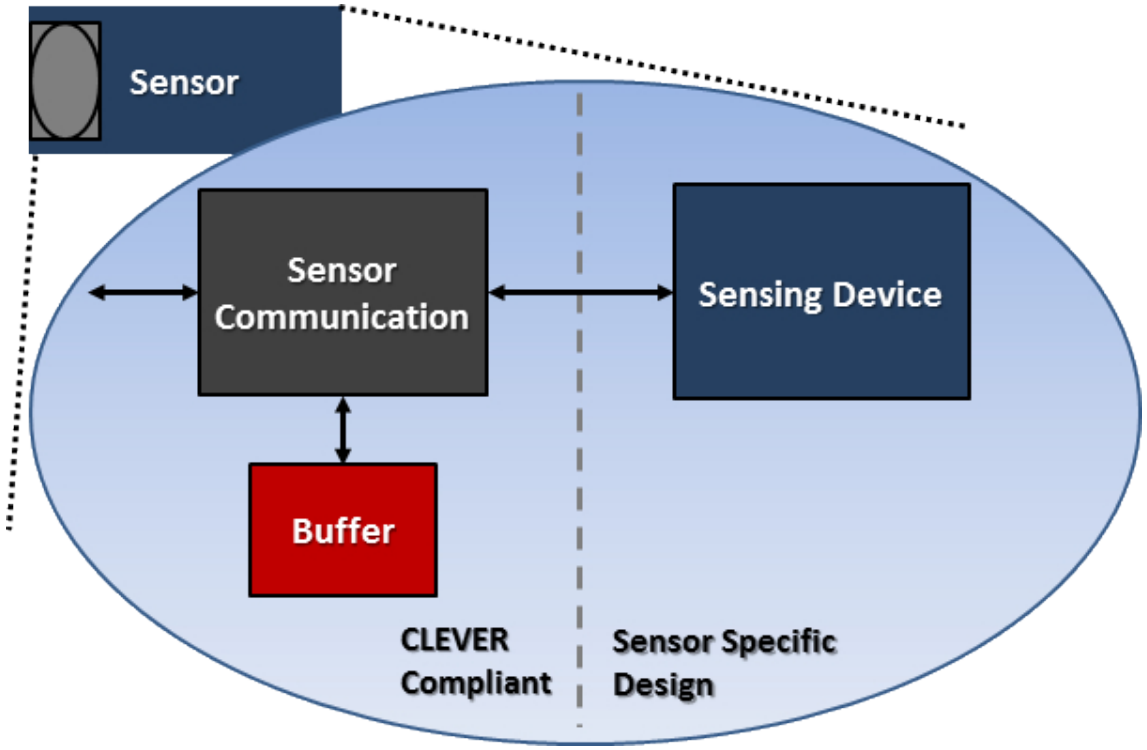
- Sensors
  - Sensing Device
  - Communication
- Processing Unit (PU)
  - Data acquisition
  - Prediction
  - Scheduler
- Memories
- Sensor Bus
- *System Bus*



CLEVER

Architecture - Sensor

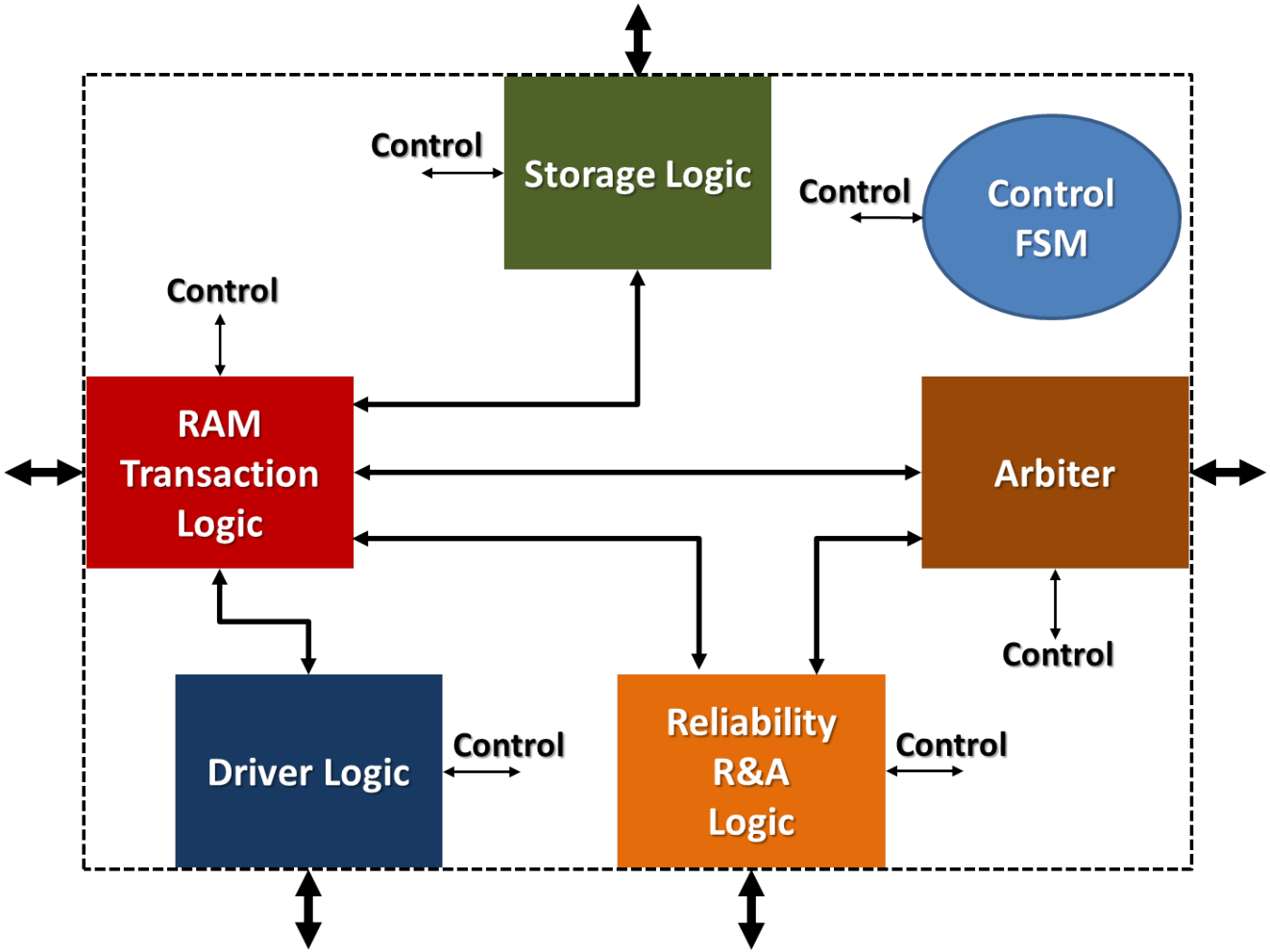
- Two principal parts
  - Sensing device
  - Communication with PU
- Sensing on different level:
  - Physical / electrical (Temp., Voltage, …)
  - Architectural (NBTI, detected faults, …)
  - System (active time, load, …)



CLEVER

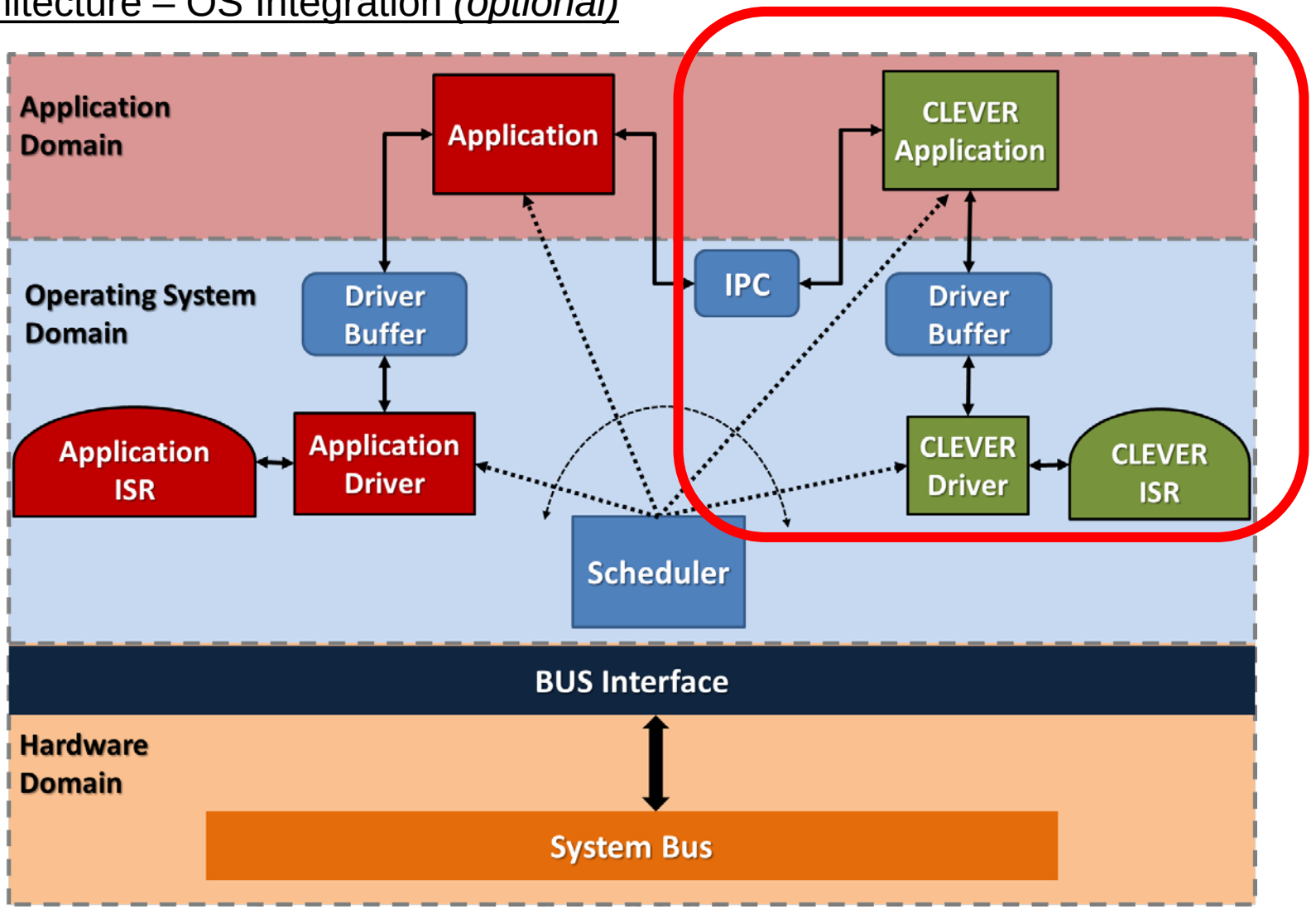
Architecture - Processing Unit

- Sensor data acquisition
- Error Prediction
- Arbitration
- Interface to Operating System *(optional)*
- Memory access



CLEVER

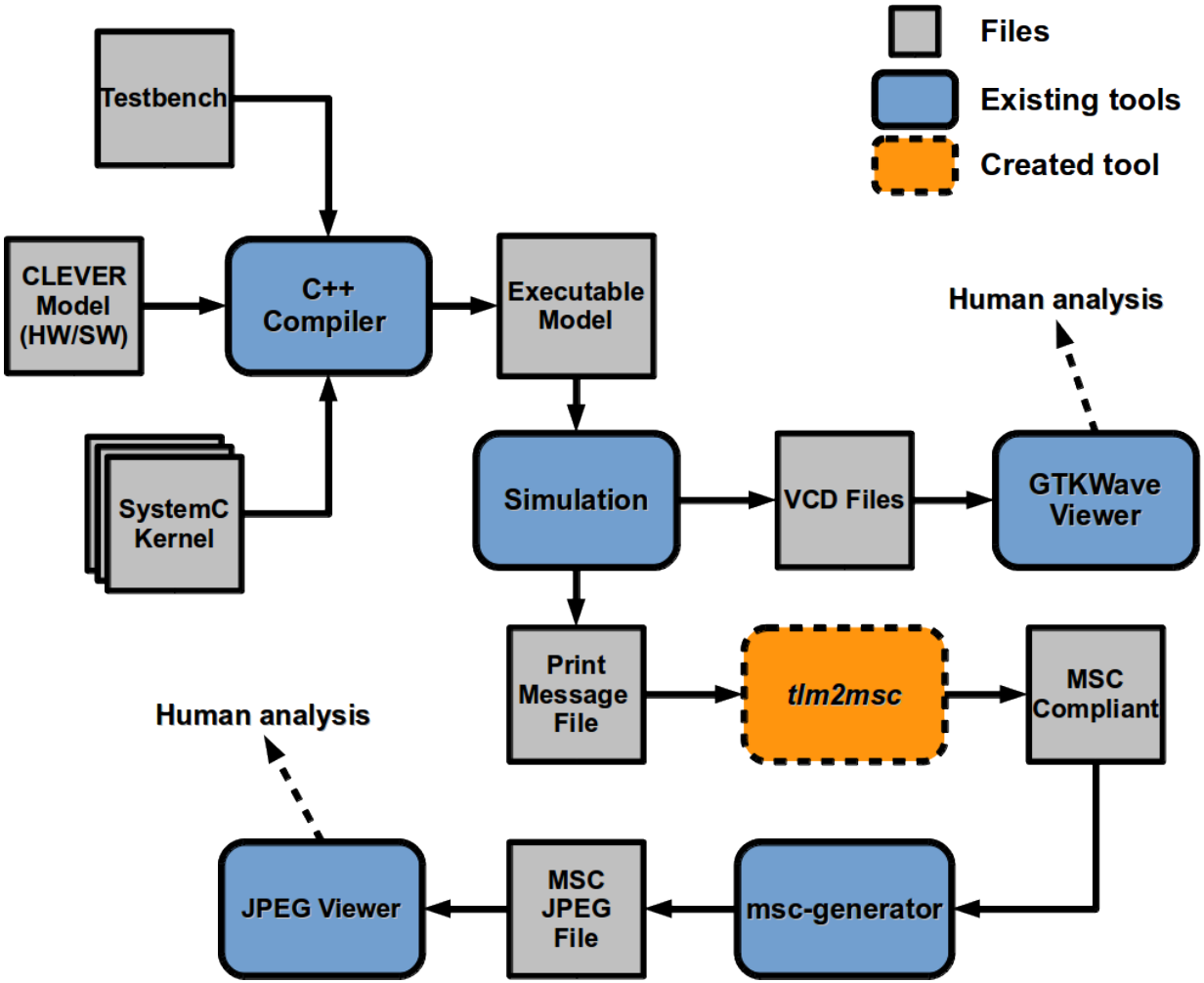
Architecture – OS Integration *(optional)*



CLEVER

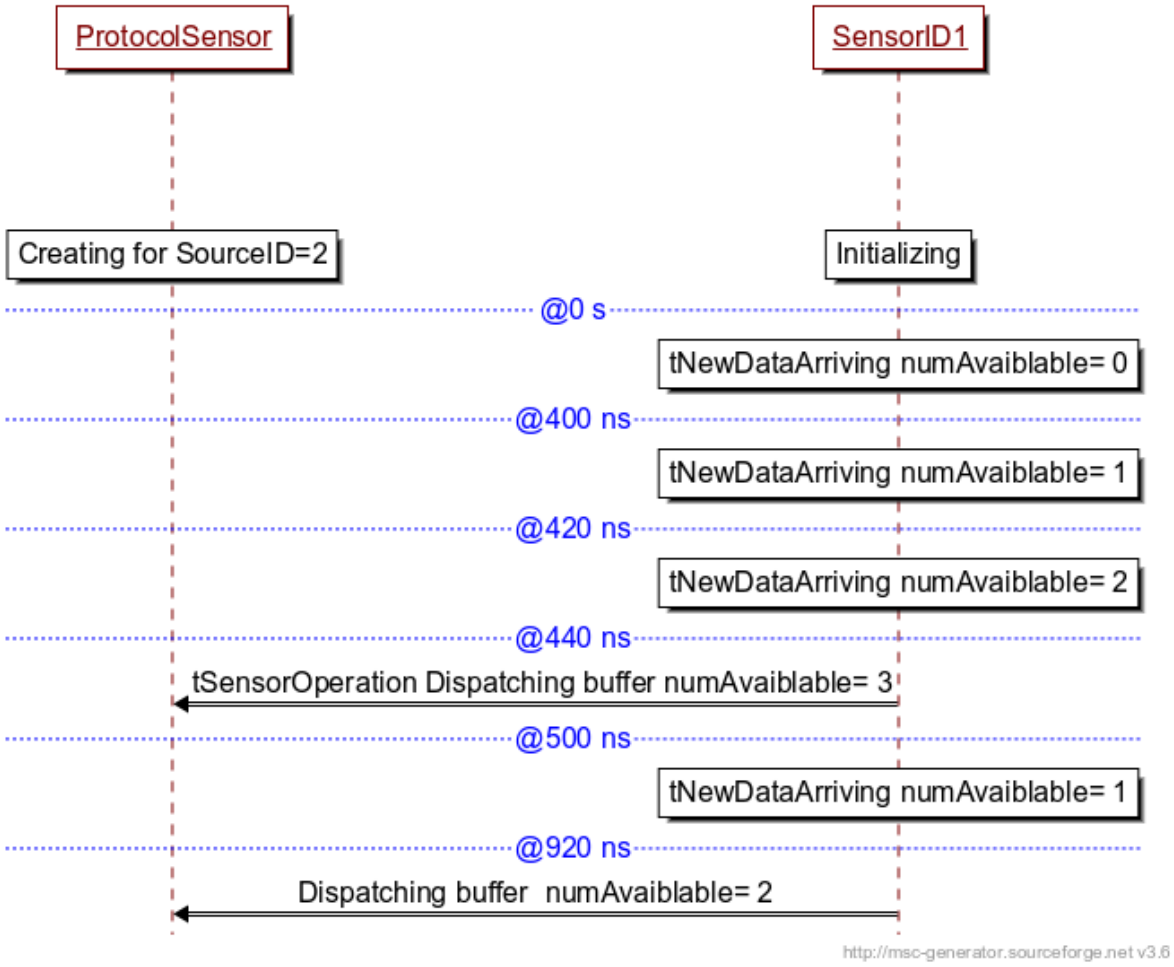
Verification Flow

- SystemC implementation
- Communication based on TLM (Transaction Level Modeling)
- Verification based on Message Sequence Chart (MSC)



CLEVER

Verification – TLM2MSC



Conclusion

- Increasing design complexity and fault probability demand solutions
- PHM solutions permit prediction of (*probable*) system failure
- CLEVER: Cross-layer approach for Error Detection and Reporting
- System Architecture of CLEVER defined
- Verification by simulation of feasibility of CLEVER architecture

- Next steps:
  - Implementation of prediction algorithm
  - Test case

Thank you!

OptMA[lab] / ART
www.asic-reliability.com