

Exploration of Noise Robustness and Sensitivity of Bulk Current Sensors for Soft Error Detection

João Guilherme Mourão Melo
Dept. of Electronic Engineering
Federal University of Minas Gerais
Belo Horizonte, MG, Brazil
jgmelo@gmail.com

Frank Sill Torres
Dept. of Electronic Engineering
Federal University of Minas Gerais
Belo Horizonte, Brazil
franksill@ufmg.br

Rodrigo Possamai Bastos
TIMA Laboratory
Université de Grenoble
Grenoble, France
Rodrigo.Bastos@imag.fr

Abstract—Radiation induced soft errors are a serious concern not only for memories but also logic circuits. Amongst the several proposed countermeasures, Bulk Built-in Current Sensors represent a promising approach with fast response times and reasonable costs in terms of area and power. However, these circuits, as well as similar sensors that measure substrate effects, are strongly susceptible to substrate noise. The intention of this work is a thorough analysis of activation mechanism and noise behavior of these sensors as well the exploration of strategies to increase noise robustness.

Keywords—reliability; noise; CMOS; VLSI; nanotechnology; substrate model

I. INTRODUCTION

The continuously downscale of CMOS technologies leads to improvements in nearly all fields of contemporary life. However, the advancements in integration density and performance come with the price of several new challenges. This includes, amongst others, leakage currents due to short channel effects and tunneling. Another serious trend is the increase of reliability related problems, mainly due to aging effects and radiation-induced failures. Sources for the former are, for example, the breakdown of the gate oxide, electromigration, or negative-bias temperature instability [1].

Faults due to radiation-induced particle strikes are historically a problem for aerospace application. However, as integrated circuit technologies enters the nanoscale age, radiation is turning to a rising concern for ground level applications, too [2]. Possible consequences of such faults can be soft errors or even system crashes. Amongst the several strategies to detect radiation-induced faults, Bulk Built-In Current Sensors (BBICS) represent a very promising approach [3]. Its advantages are high detection sensitivity, fast response times, and considerable decrease in area and power consumption [4].

Noise is an important challenge in integrated circuits, in particular for mixed-signal designs [5]. This problem is even more amplified due to the trends of increasing complexity,

diminishing voltage levels, and steeper signals [6]. As the substrate is a very good conductor, sensors that measure substrate effects, like the mentioned BBICS, but also DEPFET sensors [7], or bulk pixel sensor [8], are especially affected by noise. To our best knowledge, though, there is no published research done on noise analysis of integrated substrate sensors.

Consequently, the intention of this work is the exploration of circuit characteristics of bulk sensors in order to enhance the noise robustness, while preserving its level of detection sensitivity.

The rest of the work is structured as follows. Section II gives preliminary information, while section III explores the figures of interest. The following section IV describes the simulation environment. Section V presents and discusses the results obtained by the simulations concerning the fault signal detection, pointing out an important characteristic of the mBBICS. Section VI presents simulation results regarding noise and introduces a design strategy for enhancing noise robustness at constant sensitivity, and section VII concludes this paper.

II. PRELIMINARIES

This section presents basic information about effects that lead to soft errors and its modeling, noise, and sensors for detection of radiation induced faults.

A. Soft Errors

As previously stated, soft errors can cause system failure or information falsification. Those errors are called Single Event Upsets (SEUs) or Single Event Transients (SETs), depending on its nature. Both are caused by energetic particles that strike reversed-biased p-n junctions of integrated circuits, e.g. the drain-substrate region of an NMOS in off-state, and form high levels of charge carrier generation (see Fig. 1). The following charge collection phase, accelerated by funneling and diffusion effects, can lead to voltage peaks at the affected transistor terminal and, consequently, to an error within the circuit [2].

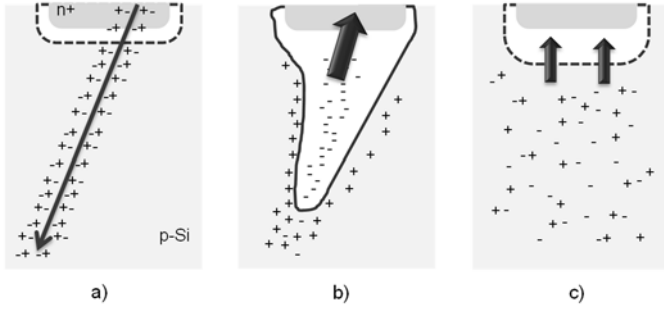


Fig. 1. a) Radiation-induced particle strike in a reversed-biased p-n junction, e.g. drain and substrate of a NMOS in off-state, and electron-hole pair generation, b) initial charge collection phase (drift/funneling), c) final charge collection phase (diffusion) [10].

SEUs are digital signal falsifications that change the signal state in memory elements such as flip-flops or latches, and consequently, affecting sequential logic. In contrast, SETs are perturbations that change a signal for a short time before it returns to its original state. If the effect of such perturbation reaches an enabled memory element it will cause incorrect behavior, too [9].

B. Fault signal modeling

The incidence of a radiation-induced particle in a reversed-biased p-n junction generates electron-hole pairs throughout the particle path, as can be seen in Fig. 1 [10]. Once the electron-hole pairs are generated, carrier collection takes place, which can be observed as a current on the affected node. The carrier collection process can be divided into two phases: a rapid collection phase due to the electrical field, accelerated by a creation of a funnel (see Fig. 1b), and a slower collection due to diffusion (see Fig. 1c) [11].

The resulting current pulse I_{strike} at the affected node can be approximated by a double exponential function as follows [12]:

$$I_{strike}(t) = \frac{Q_{coll}}{t_f - t_r} \left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}} \right) \quad (1)$$

with Q_{coll} is the total charge collected, t_r labels the time constant for the initially collection phase, and t_f means the decay time of the current pulse.

C. Noise modeling

An in-depth noise analysis requires the modeling of different kinds of noise. In VLSI circuits, one can find essentially three kinds of noise: Thermal Noise, Shot Noise and Flicker Noise [6].

Thermal noise, as the name states, occurs due to inherent crystalline structure agitation of the material, which causes charge carriers in the conduction band to move randomly. Its realization in time is modeled by the Normal Distribution, and since its Power Spectral Density (PSD) shows ideally the same

power density for all frequency bands, it is so-called white noise. Hence, thermal noise should be modeled as White Gaussian Noise (WGN) [13].

Shot noise is caused by temperature, too. However, its physical mechanism is different from thermal noise. A hole-electron pair is generated by temperature excitation, i.e. the electron at the valence band acquires energy and is then moved to the conduction band. This kind of noise is also white noise, although not necessarily Gaussian. Nevertheless, it can be modeled as such, and thus, shot noise is modeled in this work as WGN, too.

Since both Thermal and Shot Noise are WGN, they can be represented by just one Normal Distribution with variance v_{WGN} , which follows from equation (2):

$$v_{WGN}^2 = v_{thermal}^2 + v_{shot}^2 \quad (2)$$

With $v_{thermal}$ meaning the variance of the Thermal Noise, while v_{shot} represents the variance of the Shot Noise. The mean of the applied noise, and thus of its components, is zero [5].

Flicker Noise (also known as 1/f noise or pink noise) is a yet not fully understood phenomenon [13]. However, it is known to be present in VLSI circuits and to have a PSD that decreases with increasing frequency. Given that Flicker Noise actuates in stronger manner at low frequencies, one can conclude that its power spectrum constitutes the WGN power spectrum, i.e. WGN is a more general type of noise. Hence, a signal that behaves like flicker noise can be filtered from WGN, which is the approach applied in this work.

D. Modular Bulk Built-In Current Sensors

Built-In Current Sensors (BICS) are an efficient mechanism to detect permanent faults and SEU in CMOS circuits during its quiescent state, i.e. when the circuit is not switching [14]. However, this method is not applicable for detection of SET, as the amplitude of transient currents induced by radiation can have the same order of currents normally generated by switching activities in combinational logic circuits [9]. As an alternative have been proposed Bulk Built-In Current Sensors (BBICS) that measure the anomalous current that flows from the bulk of the disturbed transistor to the supply [3][15]. This current is created by the charge carriers that are opposite to the ones collected by drain. The BBICS for Silicon-on-Chip (SOI) technologies was explored in [16].

Amongst the several implementations, the modular Bulk BICS (mBBICS) represents a promising trade-off between sensitivity, response time, robustness, and area overhead [17]. Further, its basic concept is similar to other BBICS. Hence, it was chosen as representative circuit.

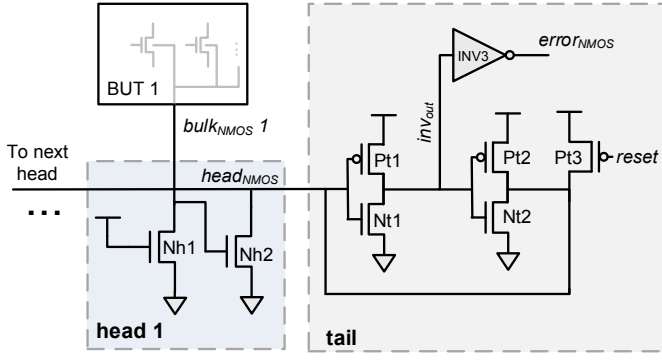


Fig. 2. The modular Bulk Built-In Current Sensor.

The mBBICS is composed by two functional blocks: the head and the tail (see Fig. 2). The head circuits are connected to the bulk of the monitored transistors, while the tail circuit latches the output signal of several head circuits. In detail, the drain of transistor N_{h1} is connected to the bulk of the monitored transistors, its source is at GND, and its gate connected to VDD. In normal operation, the drain of N_{h1} acts as a virtual GND while the drain of N_{h2} is at V_{DD} level. In the event of a strike, the fault current is conducted through N_{h1} . The consequent voltage drop increases the gate voltage of N_{h2} , which is switched on and pulls down the signal $head_{NMOS}$ that is connected to the drain of N_{h2} and the input of the tail circuit. The latter latches the input and activates the error flag. The circuit remains in that state, until the reset transistor is activated, causing the circuit to return to initial state and be ready for another detection. For the sake of simplicity, we concentrate solely on the NMOS version and omit the complementary mBBICS for monitoring PMOS bulks.

E. Noise impact on Bulk sensors

We could show in previous work that noise transported via the substrate is an important concern for bulk sensors, as it can lead to false detections [18]. In case of the mBBICS, the most susceptible element to noise is the transistor N_{h1} , located in the head structures, as it is directly connected to the substrate. Identified critical noise Root Mean Square (RMS) levels are 5 % of V_{DD} in case of White Gaussian Noise and 10 % of V_{DD} in case of Flicker Noise [18].

III. FIGURES OF INTEREST

This section introduces the principal focus of this work.

A. Load capacitance variation and false activation

As presented in section II, the bulk terminal of a device to be monitored by the BBICS must be connected to the drain terminal of transistor N_{h1} . It can be noticed that such a connection will introduce to the BBICS input an additional capacitance due the bulk capacitance of the monitored device. Moreover, the capacitances of further monitored devices will

sum, since they are in parallel. Hence, it is expected that these capacitances will diminish the sensor's sensitivity, *i.e.* the minimum radiation-induced bulk current it can measure. This reduction is based on the decrease of the voltage peak on the gate of N_{h2} due to higher load (capacitance) on this node.

However, considering noise that enters the sensor via N_{h1} , it comes to sight that this capacitance will act as a low-pass filter, potentially eliminating part of the noise at the drain. Therefore, an objective of this work is the analysis of the relation between noise susceptibility, sensitivity and the capacitive load introduced by the monitored devices.

B. Design Exploration

The design of Bulk-BICS is driven by achieving the highest sensitivity possible, *i.e.* it must be capable to detect every particle strike that can cause a SET. Furthermore, even higher sensitivity than necessary should be pursued in order to compensate variations of process and environmental parameters [17]. Nevertheless, sensitivity to SETs comes along with sensitivity to noise as weaker signals can activate the sensor. Hence, one should guarantee that the sensor is able to detect SETs reliably, but must as well keep sensitivity low enough to prevent false detections due to noise.

Hence, an objective of this work is the analysis of design decisions that optimize sensitivity as well as noise robustness of the bulk sensors.

IV. SIMULATION ENVIRONMENT

All tests have been executed using the NMOS version of modular Bulk-BICS (mBBICS) monitoring the number of N_{trans} devices [17]. The bulks of these devices were connected to the drain of transistor N_{h1} , while its gate and source were connected to GND, and the drain to VDD. The dimensions of the monitored transistors were set to minimum length and width.

The transistor level representation of the mBBICS circuit was realized, including appropriate transistor sizing and verification. Therefore, a predictive 90 nm process with a V_{DD} of 1.2 V has been used [19].

Noise analysis was realized by two current noise waveforms, which are applied to stimulate the input of the sensor that is connected to the bulk of the monitored devices. The first noise is WGN, generated from the realization of a Normal distributed random variable with zero mean and variance equal to 1, corresponding to Thermal and Shot Noise. The second noise is the result of the WGN subjected to a low-pass filter, yielding the Flicker Noise. Both waveforms were multiplied by an iteratively adjusted factor for each load transistor area, in order to adapt the RMS value. Each noise simulation lasted 3ns, being each noise waveform composed by 1×10^3 samples, in order to comply with the random nature of noise.

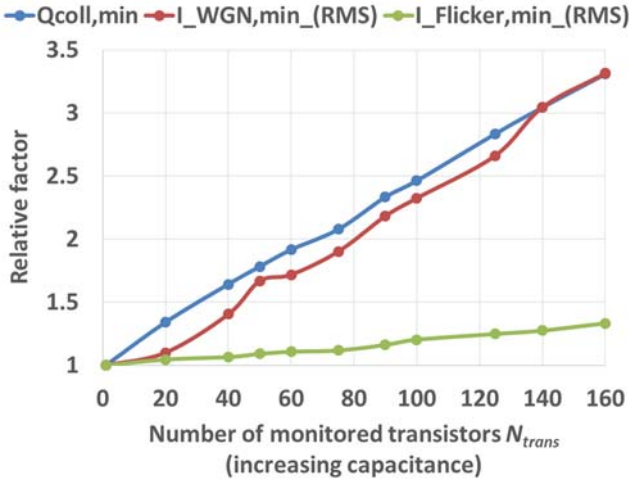


Fig. 3. Relative increase of minimum $I_{RMS,min,WGN}$ and $I_{RMS,min,Flicker}$ of WGN and Flicker noise, and minimum collected charge $Q_{coll,min}$ that activates the sensor as function of number of monitored transistors N_{trans} . The number of transistors represent the load capacitance.

V. LOAD CAPACITANCE ANALYSIS

This analysis focuses on the relation between the load capacitance, the sensors capability to detect radiation induced faults, and the noise susceptibility of the sensor. As stated before, the signal that enters the mBBICS at the input that is connected to the bulk, *i.e.* at the drain of transistor N_{h1} (see Fig. 2), is facing a low-pass filter structure. This structure consists of the channel resistance of N_{h1} and the load capacitance induced by gate capacitance of N_{h2} and bulk capacitance of the monitored devices. Consequently, it is expected that noise might be filtered which should reduce the noise susceptibility of the sensor.

The analysis was executed for different amounts of monitored transistor N_{trans} and was separated in two phases. The first phase was related to the reduction of the mBBICS's sensitivity due to increasing load. Therefore, for each value of N_{trans} the minimum collected charge $Q_{coll,min}$ that the sensor could measure was determined. The slope parameters t_r and t_f were set to 10 ps and 100 ps, respectively. It should be noted that the minimum charge that leads to a Soft-Error is independent of the amount of monitored transistors.

The second phase focused on the analysis of the noise robustness for varying N_{trans} . Therefore, WGN and Flicker current noise were applied to the input of the mBBICS that is connected to the bulk, *i.e.* the drain of N_{h1} . Next, the minimum RMS values $I_{RMS,min,WGN}$ and $I_{RMS,min,Flicker}$ of the WGN and Flicker noise that lead to an activation of the sensor were determined.

In order to compare the results, the relative increase of $I_{RMS,min,WGN}$, $I_{RMS,min,Flicker}$, and $Q_{coll,min}$ were estimated (see Fig. 3). The results indicate comparable tendencies for WGN and minimum collected charge required to activate the mBBICS.

That is, both increase approximately by factor 1.4×10^{-3} with the amount of monitored transistors. Hence, it can be concluded that with increasing amount of monitored transistors the sensor's sensitivity decreases. At the same time, the robustness against WGN increases in the same measure. Hence, it can be concluded that the filtering effect has no considerable impact on WGN. This conclusion is reinforced by Fig. 4 which shows that minimum WGN actually tends to rise more than the strike generated current. More important, all of the absolute RMS values of minimum WGN are higher than the peak fault current.

In contrast, the noise $I_{RMS,min,Flicker}$ required to activate the sensor increases considerably lower, by a factor of 0.2×10^{-3} . That is, for larger numbers of monitored transistors, the circuit is more prone to be affected by flicker noise in detriment of real fault causes, leading to false detections.

This fact can be explained by the presence of a low-pass structure in the sensor's input. The fault current profile is composed by high frequencies, since it presents short slopes (from zero to $50 \mu A$ in 10 ps). In contrast, flicker noise is dominated by low frequencies. Therefore, only a small fraction of its spectral power is attenuated even with increasing load.

In order to verify how the fault signal slope is affected, it is proposed to subject fault currents with different rising slopes to the mBBICS input, with a load of one unit transistor, which in the technology in use, consists of a transistor with $W = 120$ nm and $L = 100$ nm. Such fault currents should have different rise times (*i.e.* different slopes), and the consequent voltage across N_{h1} should suffer different attenuations, depending on its frequency composition.

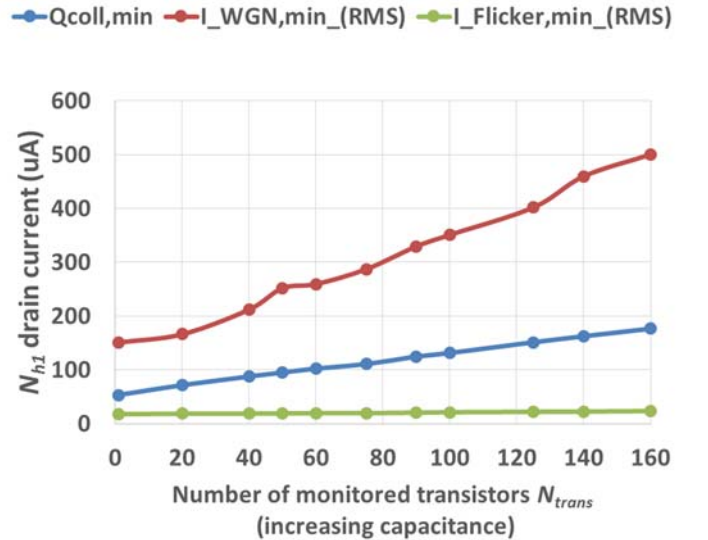


Fig. 4. Absolute values for $I_{RMS,min,WGN}$ and $I_{RMS,min,Flicker}$, as well as the current due to the minimum charge $Q_{coll,min}$ that activates the sensor, as a function of number of monitored transistors N_{trans} .

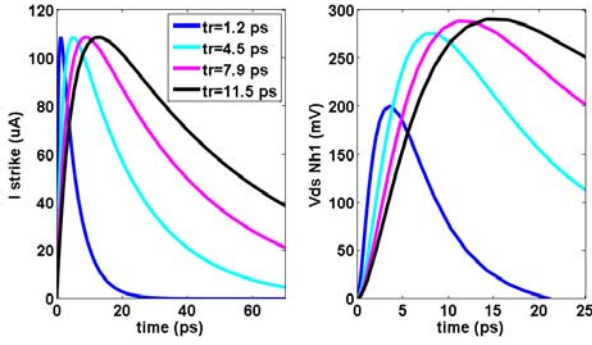


Fig. 5. Left plot: current peaks (I_{strike}) injected into the mBBICS's input: with increasing t_r (from 1.2 ps to 11.5 ps), $t_f=10 \times t_r$, $I_{peak} = 108 \text{ uA}$. Note: In order to maintain the peak current, Q_{coll} varies accordingly. Drain-Source voltages ($V_{ds, nh1}$) in transistor N_{h1} after injection of currents I_{strike} are shown in the plot at the right. Fault signals with shorter rise times (steeper increase) show more attenuation than those with longer rise times.

Fig. 5 depicts the results of such simulation. The left plot shows four fault currents with different rise times between 1 ps and 100 ps, but same peak current. The resulting voltages across drain and source of transistor N_{h1} are depicted in the right plot. It can be noticed that the voltages that are generated by higher rise times reach smaller peak voltages. Such a behavior can be justified by the attenuation provided by the low-pass effect introduced by the load transistors and N_{h1} resistance.

VI. DESIGN EXPLORATION

The results of the previous section indicate that the capacitance of the monitored devices not only affects the sensitivity of the sensor, but also its noise susceptibility. Thereby, the designer faces the decision of choosing a

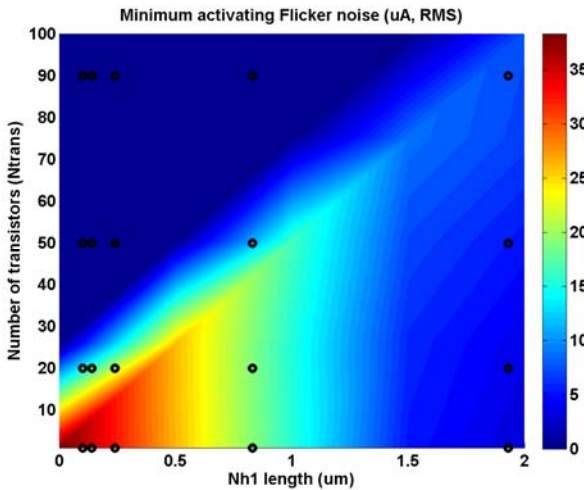


Fig. 6. Minimum flicker noise $I_{RMS,min,Flicker}$ for sensor activation. Smaller L_{Nh1} and load are least susceptible to flicker noise (area in red), while larger L_{Nh1} and smaller load are most susceptible (deep blue). The simulated values are represented by the black markers, while the remaining colored areas are a linear interpolation of those.

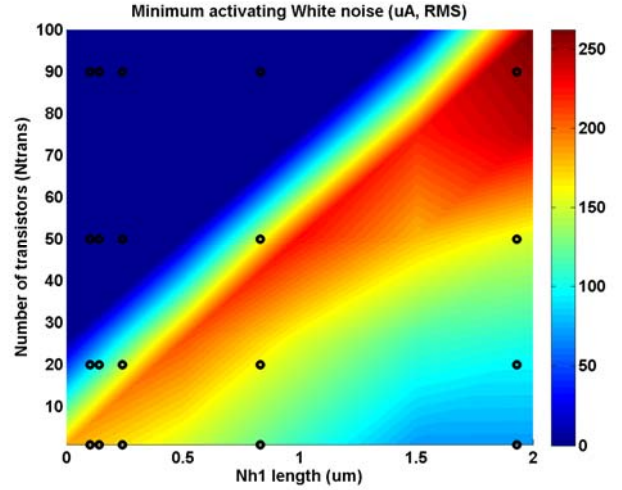


Fig. 7. Minimum white noise $I_{rms,min,WGN}$ for sensor activation. For larger loads, the sensor tends to be more robust (areas in red), since they introduce a low-pass effect and attenuate the white noise's high frequency components. The same considerations for the markers and color map of Fig. 7 apply.

maximum number of transistors for monitoring, while dealing with the reliability issues that come along with it. Hereby, it is

valuable to explore those variables relations in order to obtain guidance about correct choosing, *i.e.* using the greater number of monitored devices per sensor while keeping robustness to noise.

In order to explore this effect, the sensitivity of the sensor was modified by changing the length of transistor N_{h1} , which is acting as shunt resistor (see Fig. 2). This modification affects the channel resistance of N_{h1} , and consequently, the input signal of transistor N_{h2} in case of a current pulse that passes through N_{h1} . A longer channel, *i.e.* a greater channel resistance, results in higher voltage drop over N_{h1} , and thus, in higher input voltages to N_{h2} .

The analysis was executed in two phases: Firstly, for five values of W_{load} , a range of five lengths L_{Nh1} was determined, which enabled the activation of the sensor for a collected charge of $Q_{coll} = 11.28 \text{ fC}$, and rise and fall times of $t_r = 10 \text{ ps}$ and $t_f = 100 \text{ ps}$. Next, the minimum current noise level $I_{rms,min}$ that leads to an activation of the sensor, was determined in the estimated design space for L_{Nh1} and W_{load} .

Fig. 6 and fig. 7 illustrate the results of this analysis for Flicker noise and WGN, respectively. Here, all L_{Nh1} and W_{load} combinations with an $I_{rms,min}$ value greater than 0 (deep blue) lead to an activation of the sensor for the selected current profile. It can be noted that for each load there are values of L_{Nh1} , which still allows a SET detection but leads to minimum susceptibility to noise.

By analyzing Fig. 6, it is possible to see how the increase in the shunt transistor's length penalizes the sensor functionality.

From the origin, the sensor becomes rapidly more prone to flicker noise as the length increases. The explanation for such a characteristic is that a greater channel resistance causes higher voltage and an increase in the load (and, consequently, in the parasitic capacitance) hardly opposes to that effect, since Flicker noise is composed mainly by lower frequencies and are not attenuated by the introduced filtering effect, which is a low-pass.

In a different manner, one can notice by analyzing Fig. 7 that the opposite behavior occurs. Given a number of monitored devices, an increase in N_{h1} 's length practically does not change the noise sensitivity. This is because the low-pass characteristic introduced by the load dominates the effect of increase in length, attenuating a considerable portion of the WGN's spectral power. It can be seen that, in general, higher loads cause a better performance from the white noise's point of view.

Thus, during design phase, noise robustness can be achieved by adequate selection of the length of the shunt resistor length, given the required number of devices to be monitored. Similarly, one can establish a noise robustness level (*i.e.*, depending on the application) and then determine the number of loads and the L_{Nh1} that performs better, with a certain margin for choice.

VII. CONCLUSION

Radiation-induced soft errors are a rising challenge in today's integrated circuits and require appropriate countermeasures. A possible solution is the Bulk Built-In Current Sensors (BBICS) approach that is characterized by fast response times, high sensitivity, and reasonable costs in terms of area and power. However, as all bulk sensors the BBICS is highly susceptible to noise.

The contribution of this work is the exploration of the relation between the circuit characteristics of the bulk sensor and its noise susceptibility and how this knowledge can be applied to improve its noise robustness. A further outcome of this analysis is the determination of the importance of the consideration of the current profile for modeling of the radiation-induced current.

It should be noted that these results do not apply exclusively for Bulk Built-In Current Sensors, but also for similar sensors that are based on shunt structures in order to measure current or voltage signals.

REFERENCES

- [1] Srinivasan, J.; Adve, S. V.; Bose, P.; Rivers, J.A., "The impact of technology scaling on lifetime reliability." Int. Conf. on Dependable Systems and Networks, , pp. 177-186, 2004.
- [2] Karnik, T.; Hazucha, P.; Patel, J., "Characterization of soft errors caused by single event upsets in cmos processes." IEEE Trans. on Depend Secure, pp. 128-143, 2004.
- [3] Neto, E.H.; Ribeiro, I.; Vieira, M.; Wirth, G.; Kastensmidt, F.L., "Using Bulk Built-in Current Sensors to Detect Soft Errors," IEEE Micro, vol.26, no.5, pp.10-18, 2006.
- [4] Wirth, G. and Fayomi, C. "The Bulk Built In Current Sensor Approach for Single Event Transient Detection". IEEE Int. Symp. on System-on-Chip, pp. 1-4, 2007.
- [5] Stanic, B.R.; Verghese, N.K.; Rutenbar, R.A.; Carley, L.R.; and Allstot, D.J., "Addressing substrate coupling in mixed-mode ICs: simulation and power distribution synthesis", IEEE Journal of Solid-State Circuits, vol.29, no.3, pp.226-238, Mar 1994.
- [6] Salmann, E., "Switching noise and timing characteristics in canoscale integrated circuits." Ph.D. Thesis. New York: University of Rochester, 2009.
- [7] Velthuis, J.J., et al. "A DEFPET Based Beam Telescope With Submicron Precision Capabilit", IEEE Trans. on Nuclear Science, vol.55, no.1, pp.662-666, Feb. 2008.
- [8] Bugiel, S.; Dasgupta, R.; Glab, S.; Idzik, M.; Kapusta, P., "Development of pixel detector in Novel sub-micron technology SOI CMOS 200 nm", Proc. of the 21st Int. Conf. on Mixed Design of Integrated Circuits & Systems (MIXDES), pp. 205-208, 2014.
- [9] Narsale, A.; Huang, M.C., "Variation-tolerant hierarchical voltage monitoring circuit for soft error detection", Int. Conf. on Quality of Electronic Design (ISQED), pp.799-805, March 2009.
- [10] Baumann, R.C., "Radiation-induced soft errors in advanced semiconductor technologies," IEEE Trans. on Device and Materials Reliability, vol.5, no.3, pp.305-316, 2005.
- [11] Hsieh, C. M.; Murley, P. C.; O'Brien, R., "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices", IEEE Trans. on Electron Device Lett., vol. 2, no. 4, pp. 686-693, Dec. 1981.
- [12] Srinivasan, G. R.; Murley, P. C.; Tang, H. K., "Accurate, predictive modeling of soft error rate due to cosmic rays and chip alpha radiation", Proc. of IEEE Int. Reliability Physics Symposium, 1994. 32nd Annual., IEEE International, pp. 12-16, 1994.
- [13] Arnaud, A.; Galup-Montoro, C., "Consistent noise models for analysis and design of CMOS circuits", IEEE Tran. on Circuits and Systems I: Regular Papers, vol.51, no.10, pp.1909-1915, Oct. 2004.
- [14] Vargas, F.; M. Nicolaidis, "SEU-tolerant SRAM design based on current monitoring", Digest of Papers of 24th Int. Symposium Fault-Tolerant Computing,(FTCS-24),pp. 106-115, 1994.
- [15] Bastos, R. P.; Sill Torres, F.; Dutertre, J.-M.; Flottes, M.-L.; Di Natale, G.; Rouzeyre, B., "A single built-in sensor to check pull-up and pull-down CMOS networks against transient fault", Proc. of 23rd Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 157-163, 2013.
- [16] Champeix, C.; Borrel, N., S.; Dutertre, J. -M.; Goessel, M.; Robisson, B.; Lisart, M.; Sarafianos, A., "Experimental Validation of a Bulk Built-In Current Sensor in Detecting Laser-Induced Currents," On-Line Testing Symposium (IOLTS), 2015 IEEE 21st International , in press.
- [17] Sill Torres, F.; Bastos, R. P., "Detection of transient faults in nanometer technologies by using Modular Built-In Current Sensors." Journal of Integrated Circuits and Systems. , v. 8, p. 89-97, 2013.
- [18] Melo, J.G.M.; Sill Torres, F., "Noise analysis of integrated bulk current sensors for detection of radiation induced soft errors", 16th Latin-American Test Symposium (LATS), pp.1-6, March 2015.
- [19] Reference Manual for Generic 90nm Salicide 1.2V/2.5V 1P 9M Process Design Kit (PDK) Revision 4.3. Cadence Design Systems, Inc. (2008).