A Methodology for Standard Cell Design for QCA

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***Abstract*—QCA (Quantum-Dot Cellular Automata) is an emerging nanotechnology that has the potential to replace current CMOS technologies. QCA permits extremely low power consumption, since its working principle is not based on electric current flow but on Coulomb interaction. The development of Electronic Design Automation (EDA) tools and flows is an essential step towards the applicability of QCA for integrated designs. However, the scarce number of works in this field highlights that there is plenty of room for the development of new EDA methodologies for emerging nanotechnologies. Standard cells play an important role in this context, since the development of routing and placement algorithms are strongly related to their existence. This work presents a methodology for standard cell design for QCA as well as the exemplary QCA cell library ONE, which is based on the recently proposed USE (Universal, Scalar and Efficient) clocking scheme. Two representative case studies indicate the feasibility of the approach.**

Keywords— Quantum-Dot Cellular Automata, Clocking schemes, Standard cell library, EDA, nanotechnologies.

I. INTRODUCTION

The increasing integration density in CMOS technology has been possible thanks to the scaling of its devices. However, the continuous reduction of the transistors feature size resulted in several severe problems, including power consumption and reliability concerns [1]. Emerging nanotechnologies such as Quantum-Dot Cellular Automata (QCA) or Carbon Nanotubes (CNTs) possess promising characteristics that can overcome problems of current technologies. In case of QCA, the absence of electric currents for the transport of information and execution of logic operation allows ultra-low power consumption. Furthermore, the expected QCA basic unit length is within the range of 2 – 18 nm [2], which is comparable or shorter than the channel lengths in modern CMOS fabrication processes. Moreover, it has been reported that QCA may be operable in the THz range [3]. Despite its advantages in comparison to CMOS, QCA has to overcome several challenges, such as issues related to its physical implementation.

The QCA basic unit is a cell, which comprises two electrons allowed to tunnel between four positons. However, the tunneling mechanism must be controlled by external clock signals in order to ensure that changes in the polarization level of the cells will occur adiabatically and at a desirable moment [2]. As evidenced, a clock circuit performs tasks related to timing and synchronism. If the information is running out of time in a circuit, it might cause wrong processing of logic implying in concerns on reliability.

Since clocking is an essential concept for QCA devices, it becomes necessary to use a methodology to ensure that the clock signal will be efficiently delivered to each cell in a circuit. Clocking schemes, such as USE [4] have been proposed in order to establish design rules that enable the development of placement and routing algorithms, as well as the specification of QCA standard cells.

Standard cells are logic cells which perform specific functions, have similar geometric dimensions and can be used as building blocks for integrated designs. Further, standard cells allow tools to automatically synthesize a circuit and optimize area, power consumption and timing. Additionally, standard cells can comprise the layout of the physical implementation, allowing placement and routing programs to apply these information to automatically generate the final design implementation.

This work presents a methodology for standard cell design for QCA based on the USE design rules. The methodology was used to develop the library QCA ONE, implemented as an extension of the tool QCADesigner [5]. The methodology concepts are suitable for the whole QCA paradigm including other simulation tools. Thus, the results of this work are important steps toward the consolidation of the QCA nanotechnology.

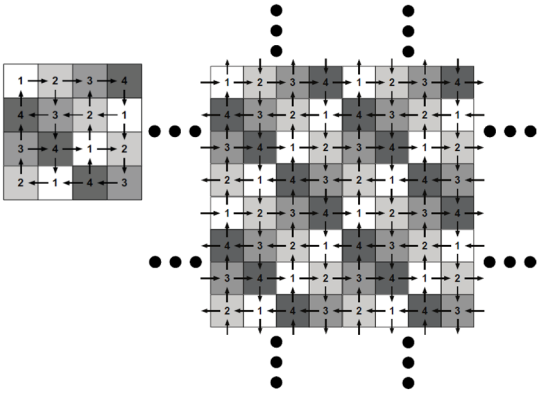
The remaining paper is organized as follows. Section II introduces the clocking of QCA circuits, while section III presents briefly the basics of USE clocking scheme. Section IV focuses on the methodology for standard cell design for QCA, and introduces QCA ONE. Section V discusses the implementation of two case studies, and section VI concludes the paper.

II. PRELEMINARIES

QCA is a new computation paradigm based on transferring information and performing logic by means of Coulomb interactions, and consequently, without electric current flow [2][6].

The transition between the two logic states occurs adiabatically. Sudden changes in the polarization level set the system into a metastable state, resulting in undesirable delays or wrong logic processing [7]. Thus, the QCA cells inter-dot potential barriers must be gradually adjusted in order to allow or deny electron tunneling. This can be achieved by an external clock circuit providing clock signals that control the adiabatic change process. The clock circuit should be able to deliver its signals to every cell in the circuit. In order to meet such requirement, it should be precisely positioned below the QCA layer.

A clock signal has four phases: switch, hold, release and relax. In the switch phase, the rising inter-dot barriers allow



(a) A single USE grid (b) An extended USE grid

Fig. 1. (a) A single 4x4 USE grid. Each number indicates the clocking zone of the particular square. Further, each square consist of a predefined number of QCA cells. Note that information flow manner allows several possibilities for QCA structures design and routing. (b) An extended USE grid, which can be achieved by positioning the individual grids side by side.

polarization level changes. In the hold phase, the cell is unsusceptible to external influences and keeps its polarization level. In the release phase, the falling inter-dot barriers are responsible lead to the depolarization of the cell. In the final relax phase, the cell remains depolarized until a new cycle restarts with the following switch phase.

A QCA circuit is usually divided into sub sections. Thus, the same clock signal is applied to more than one cell at a time. A set of cells under the same clock signal is named clock zone. The zones arrangement enables the transport and processing of information in a pipeline fashion. More information about QCA and QCA clocking can be found in [8]-[10].

III. USE Clocking Scheme

USE clocking scheme is a recently proposed approach for clock distribution in QCA circuits. It is based on the principle exposed in Section II that the clock zones must be sequentially arranged in order to establish the information flow. A 4x4 grid ensures the right arrangement for the clock zones, by associating the cells located within each of its division boundaries to one of the four clock zones. Each grid division has square dimensions that are defined by the designer.

In USE, two adjacent rows or columns always pass on the information by opposite directions, which enables several possibilities for routing and an easy establishment of feedback paths. Moreover, USE allows the implementation of coplanar and multilayer wire crossings and can be easily extended by positioning multiple grids side by side in both directions (horizontal and vertical) as depicted in Fig. 1. More information regarding USE, including possibilities for its physical implementation, can be found in [4].

IV. Methodology

A. Description

Standard cells are widely applied in CMOS in order to enable the realization of complex designs. Its similar geometric dimension permits the automation of placement and routing.

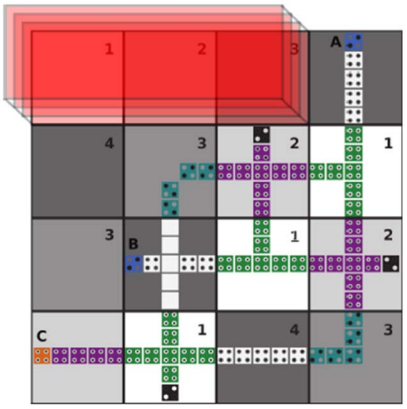


Fig. 2. An XOR standard cell placed in a 4x4 USE grid. The squares highlighted in red represent free space that might be used for routing.

Although these geometric restrictions come with the cost of area, power and delay penalties, the automation of the design flow compensates this drawback by far.

The design of a QCA standard cell library requires two principal definitions: (1) the applied clocking scheme and (2) a specification format. The former is essential for the architectural implementation of the standard cells, while the latter is mandatory for placement and routing tools.

The proposed methodology applies the USE clocking scheme and its related design rules presented in section III. The underlying grid of USE permits the structured placement of QCA circuits and its routing [4]. Consequently, the minimum size of a standard cell is one square. Fig. 2 depicts an exemplary XOR standard cell with a square size of 5x5 QCA cells. Further, spaces for possible routing in different layers are highlighted in red.

The proposed specification format for each cell contains following information:

- name: Standard cell name, also providing details about the technology type used in the manufacturing process (if available).
- n_input/ n_output/ input/ output: Number and name of the inputs and outputs.
- expression: The expression format for the logic functions performed by the standard cell.
- zone_dimension: Dimensions of each clock zone grid square.
- width/ height/layers: Width and height in terms of QCA cells and number of layers used.
- l_reference_zone/ r_reference_zone: Parameters used to guide the placement of the standard cell, ensuring that the cell is located in agreement with the data flow direction.
- delay_table: Definition of the delays between each input/output pair.
- port_location: Coordinates for inputs/ outputs placement.
- free: Indicates whether empty places within standard cell bounding box could/could not be used for routing.

```
name: maj

n_input: 3
n_output: 1
input: in0 in1 in2
output: out

expression:
out = (in0 & in1) + (in0 & in2) +
      (in1 & in2)
zone_dimension: 5

width: 5
height: 5
```

```
layers: 1
l_reference_zone: 1
r_reference_zone: 2

delay_table:
/ in0 in1 in2
out 0 0 0

port_location:
in0 0 2 0
in1 0 4 0
in2 2 4 0
out 4 2 0
```

Fig. 3 Specification of majority gate standard cell.

Fig. 3 depicts an exemplary specification of a majority gate standard cell.

B. Application example: QCA ONE

QCA ONE is a standard cells library for QCA EDA developed according to the proposed methodology. The square dimension is defined with 5x5, which leads to compact clock zones. This characteristic is favorable for avoiding thermodynamic effects, while still big enough to contain small gates, such as INV, AND and OR, within only one clock zone. Since this dimension is used along all the circuit, it is important to notice that a 5x5 zone can handle up to two parallel wires without signal interference, bent wires and wire crossing with multilayer without any problem. So far, the library is comprised of ten standard cells, depicted in Fig. 4.

In order to explore QCA ONE capabilities along with USE, both have been implemented as an extension to the simulation tool QCADesigner. The implementation includes the option to display a reference grid on the substrate (Fig. 5(a)), suitable to the USE clocking scheme design rules, where default dimensions (5x5 cells) may be changed if necessary (Fig. 5(b)). The grid uses the same colors pattern as QCADesigner in order to represent the four clock zones boundaries. This color pattern is depicted in the Fig. 5(c). Once USE clocking scheme is activated in the tool, the extended grid is exhibited and the

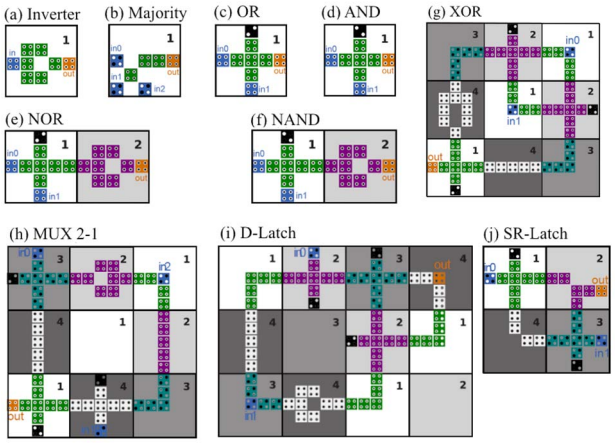


Fig. 4. QCA ONE standard cells represented within the USE grid, where the numbers at the top-right corner of each square represent the clock zone to be assigned to the cells inserted within its limits.

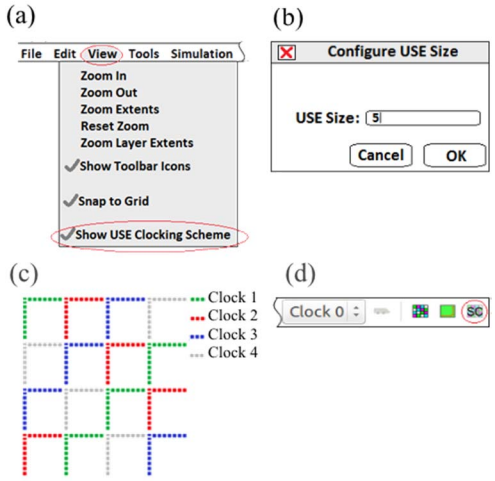


Fig. 5 (a) The path to the option to be assigned in order to show the USE grid (circled). (b) The window for the setting of the USE grid configuration (c) A sample of the USE grid and its color pattern. (d) The shortcut to the importation of QCA ONE standard cells (circled).

clock zones are automatically assigned to each new cell positioned within the substrate. Moreover, any standard cell may be imported to any layer of the design by means of a shortcut inserted in the QCADesigner graphical interface (Fig. 5(d)). In order to preserve the standard cells, manual changes in their clock zones, size or positioning of the QCA cells are not allowed. The extension tool to QCADesigner aims to speed up the design of QCA circuits, while decreasing their susceptibility to errors due to wrong clock zones assignment. An automatic routing functionality will be included in a future extension of the tool.

V. RESULTS

The first adder is able to perform a 1-bit sum. The circuit is bigger than previous adders presented in the literature. However, the aim of this study case is to show the application of different QCA ONE standard cells and how they can be integrated in order to design a more complex logic. It has three inputs: Cin, In0 and In1, which represent respectively the bit carried in from the previous less significant stage in adder cascades, and the two bits to be added. The outputs are the sum and a carry out bit, which should be passed along to the next most significant stage. Five QCA ONE standard cells were used in order to design the 1-bit adder: two AND gates, one OR gate and two XOR gates, as highlighted in Fig. 6(a). The figure also depicts wire crossing in multilayer and wire extension for delay. The latter is important in QCA circuits in order to synchronize the input signals in the gates and can be easily implemented in USE due to the different ways of routing.

The gates AND/OR occupy an area of 25 QCA cells each one, while the XOR should be positioned into an area of 125 QCA cells. In summary, the circuit requires an area of 3,375 QCA cells in which some empty space that may be used for other purposes as routing is included.

In order to demonstrate the flexibility and scalability of QCA ONE and USE a simpler 1-bit adder, implemented with three majority gates and two inverters, were proposed. This

new adder is added in the QCA ONE library and thus used to implement an 8-bit Ripple Carry Adder (RCA), depicted in Fig. 6(b). Due to the important synchronization features of QCA, long wires are necessary before and after the 1-bit adders. These wires are easily implemented in QCA USE using a zig-zag fashion in order to save circuit area.

The adder possesses seventeen inputs: Cin, A_0 to A_7, B_0 to B_7. The first input represents the bit carried in from the previous less significant stage in 1-bit adder cascades. The bits from the inputs whose names begin with A should be added to their counterparts B bits. There are eight outputs for the sum result and another for the carry out bit, which should be passed along to the next most significant stage. Forty QCA ONE standard cells were used in order to design the 8-bit adder: twenty-four 3-input majority gates and sixteen inverters. Each majority gate/inverter occupies individually an area of 25 QCA. The RCA design requires an area of about 144,000 QCA cells, mostly due to the long wires necessary to delay compensation. Although more compact RCA adders were reported in the literature [11], the aim of the circuits presented in this work is to demonstrate that standard cells development are suitable for emerging nanotechnologies such as QCA. Likely in CMOS, it is expected that standard cells will considerably enhance the design process of more complex circuits.

VI. CONCLUSIONS

The development of CAD tools for design is a mandatory step toward the consolidation of the emerging nanotechnology QCA. Standard cells libraries may be useful to safely speed up the circuits design, as they provide basic elements in which clock zones were previously assigned according to the design rules of a given clocking scheme. A methodology for standard cells design for QCA is used to create the QCA ONE, implemented along USE as an extension to the tool QCADesigner. The designs and tests of two adders (1-bit/8-bit) are presented in this paper, certifying that more complex circuits may be obtained from standard cells.

As future works, the authors suggest the development of algorithms for automatic placement and routing of QCA circuits, as well as the development of an algorithm for logic synthesis. Both implementations would represent important contributions to the state of art in the development of EDA tools for emerging nanotechnologies.

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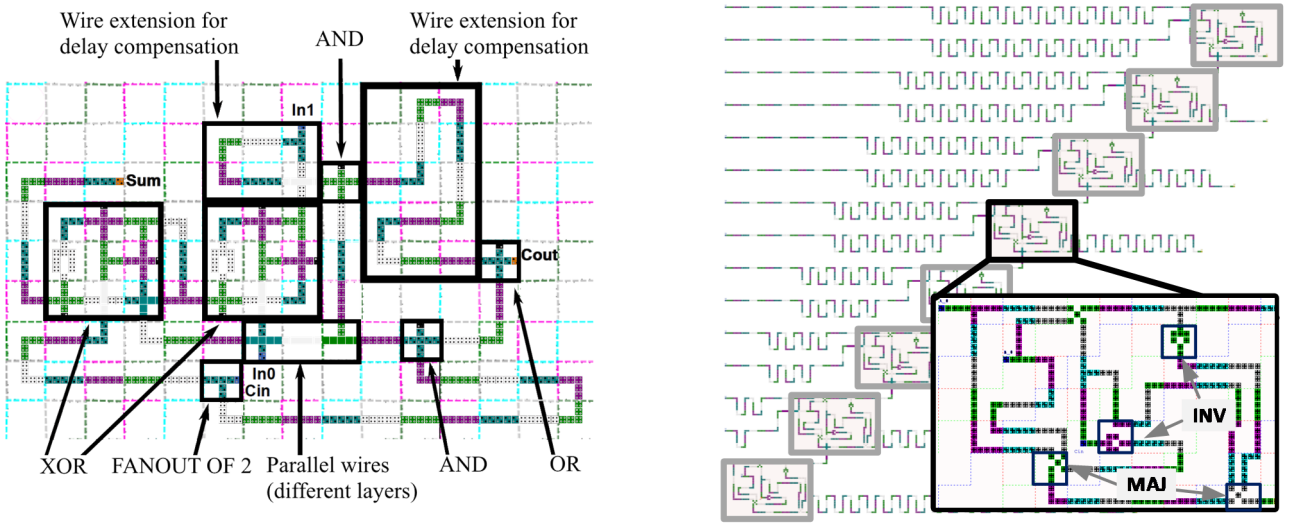

Fig. 6. 1-bit adder (a) and 8-bit Ripple Carry Adder (b), both designed from standard cells. The inlay in (b) depicts the applied 1-bit adder.