A Methodology for Standard Cell Design for QCA

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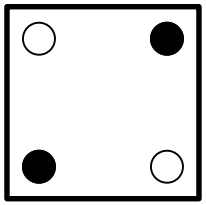
Outline

- Introduction
  - QCA
    - Clocking zones
    - Clocking schemes
- Proposed Clocking Schemes
- QCA ONE
  - Cells
  - Results
- Conclusion

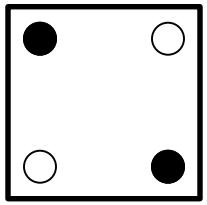
Quantum-Dot Cellular Automata - QCA

Paradigm of digital logic circuits for computing. Nanoscale; Information is transmitted without the flow of electric current **(Coulomb Interaction)**; fast; low power dissipation.



Binary 1

Polarization 1



Binary 0

Polarization -1

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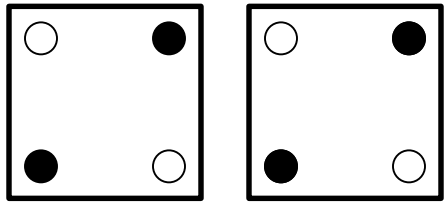

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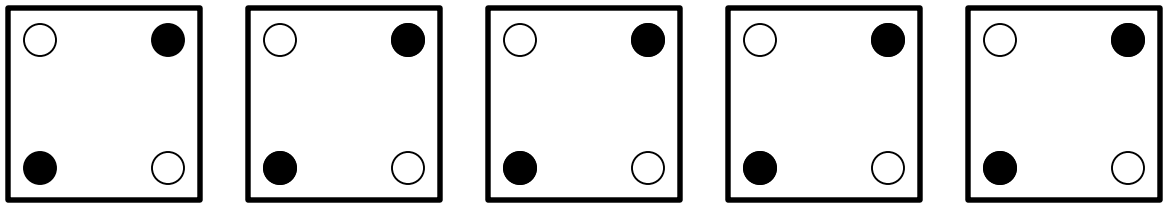

QCA Wire

Quantum-Dot Cellular Automata - QCA

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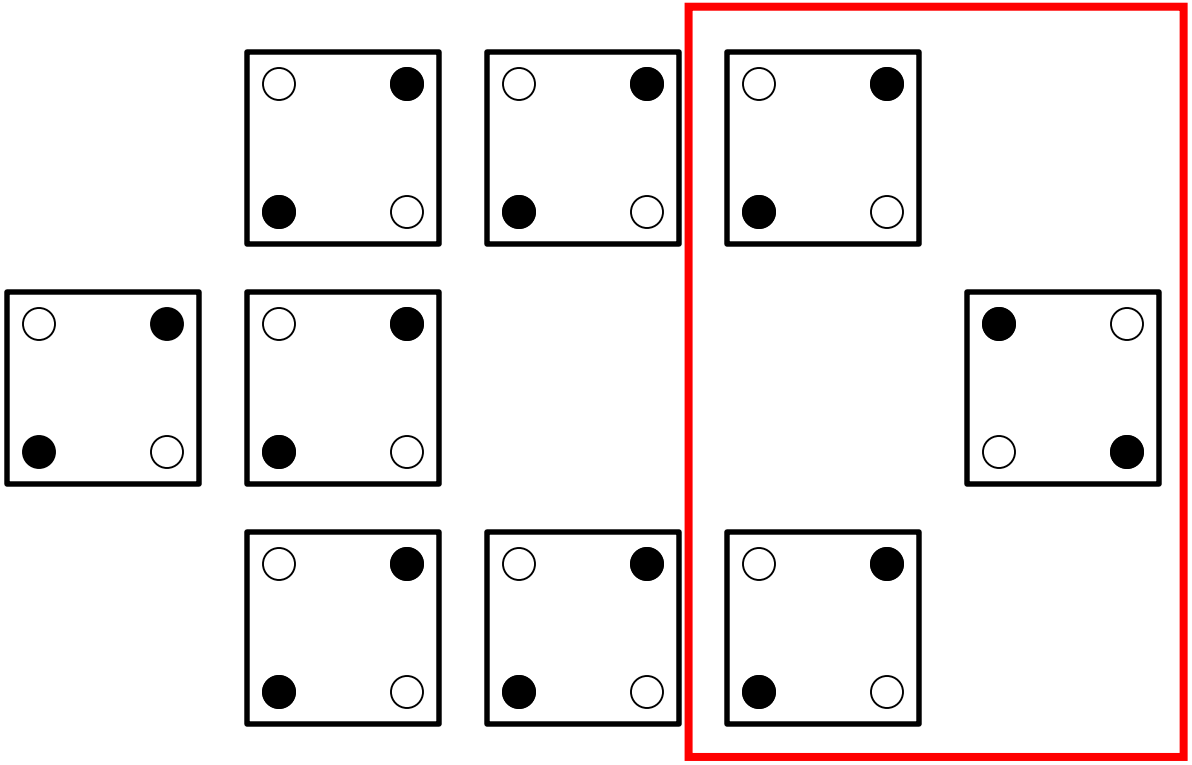
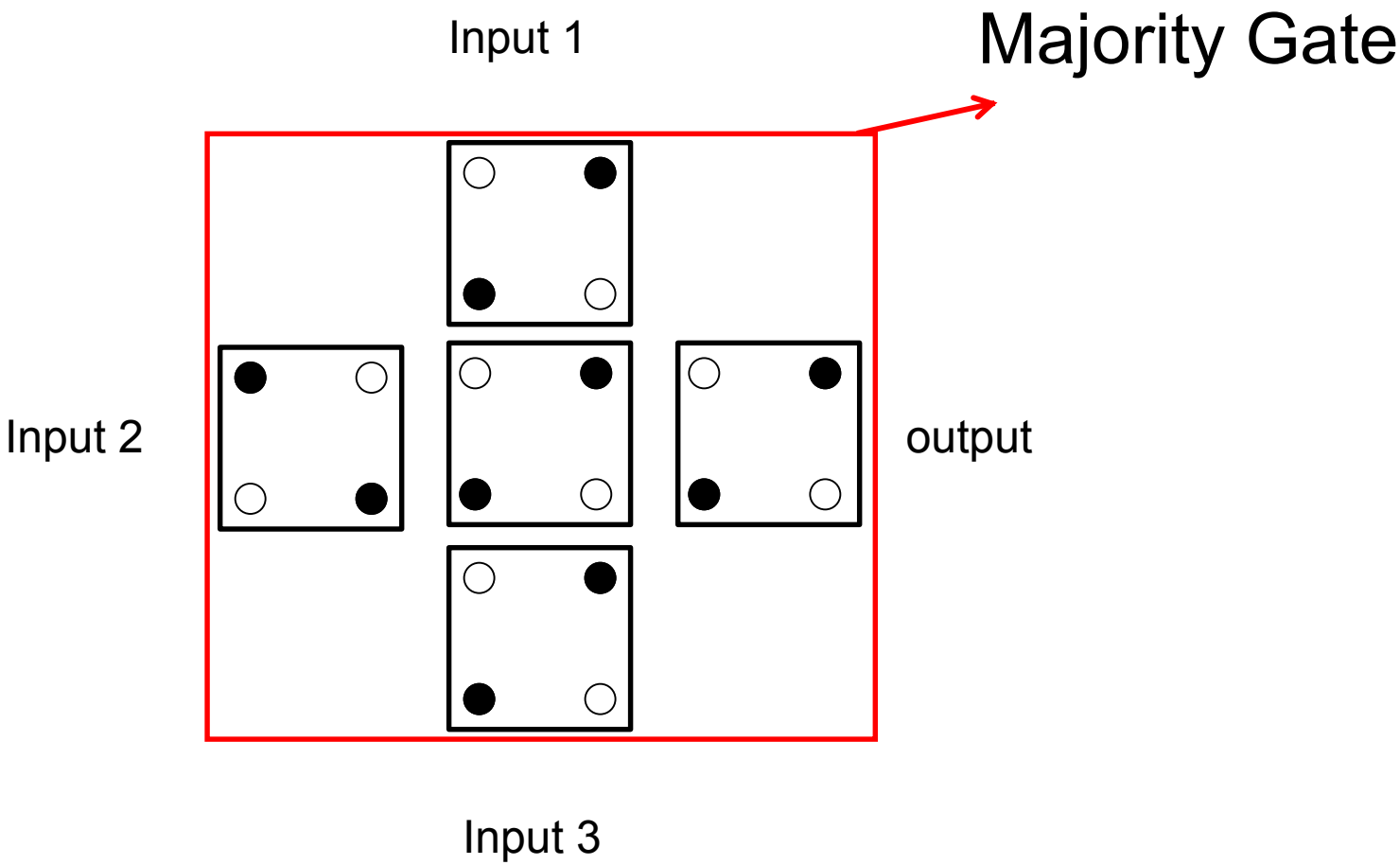


QCA inverter

Quantum-Dot Cellular Automata - QCA

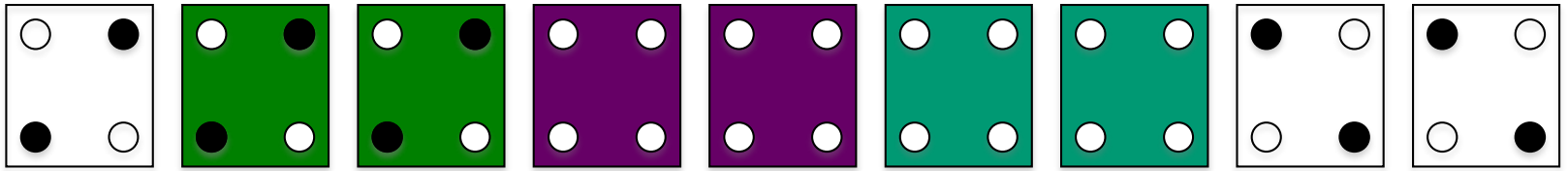


Clocking Zone, Phase and Cycle

- Allows adiabatic switching (energy efficient)
- 1 Clock cycle 4 phases

- Phase 1 – Switch: the cells can polarize;
- Phase 2 – Hold: the polarization of the cell can't change;
- Phase 3 – Release: the cells depolarize;
- Phase 4 – Relax: the cells still depolarized.

Time step 0



Clock zone 0 in switch phase	Clock zone 1 in relax phase	Clock zone 2 in release phase	Clock zone 3 in hold phase

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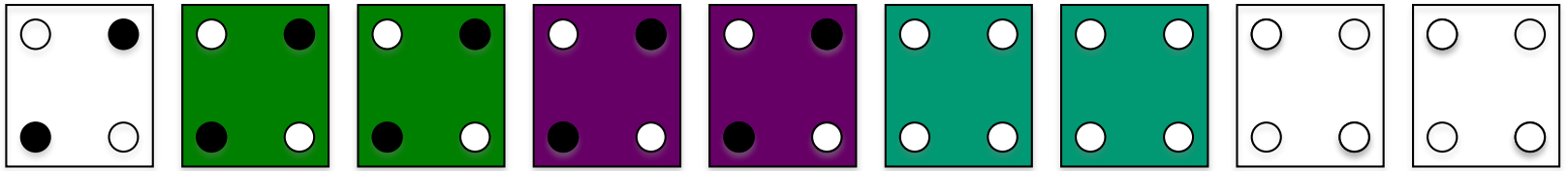

Clock zone 0 in hold phase | Clock zone 1 in switch phase | Clock zone 2 in relax phase | Clock zone 3 in release phase

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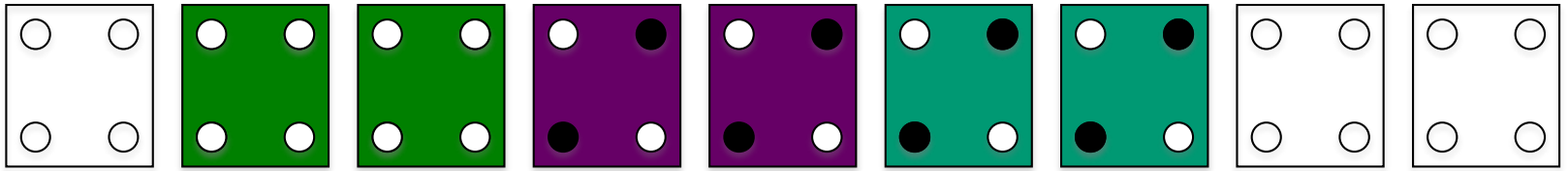
Time step 2



Clock zone 0 in release phase

Clock zone 1 in hold phase

Clock zone 2 In switch phase

Clock zone 3 in relax phase

Clocking Zone, Phase and Cycle

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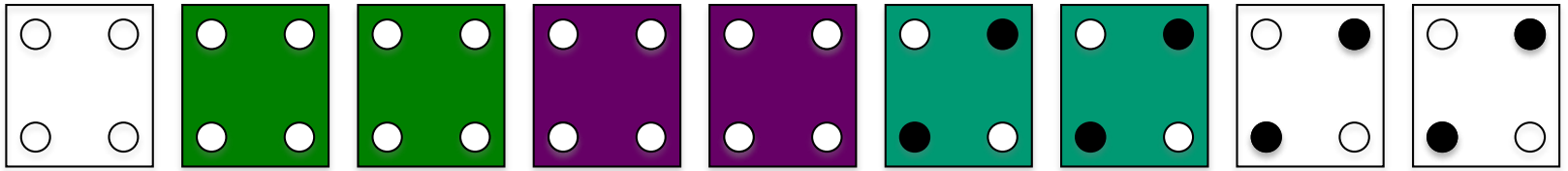
Time step 3



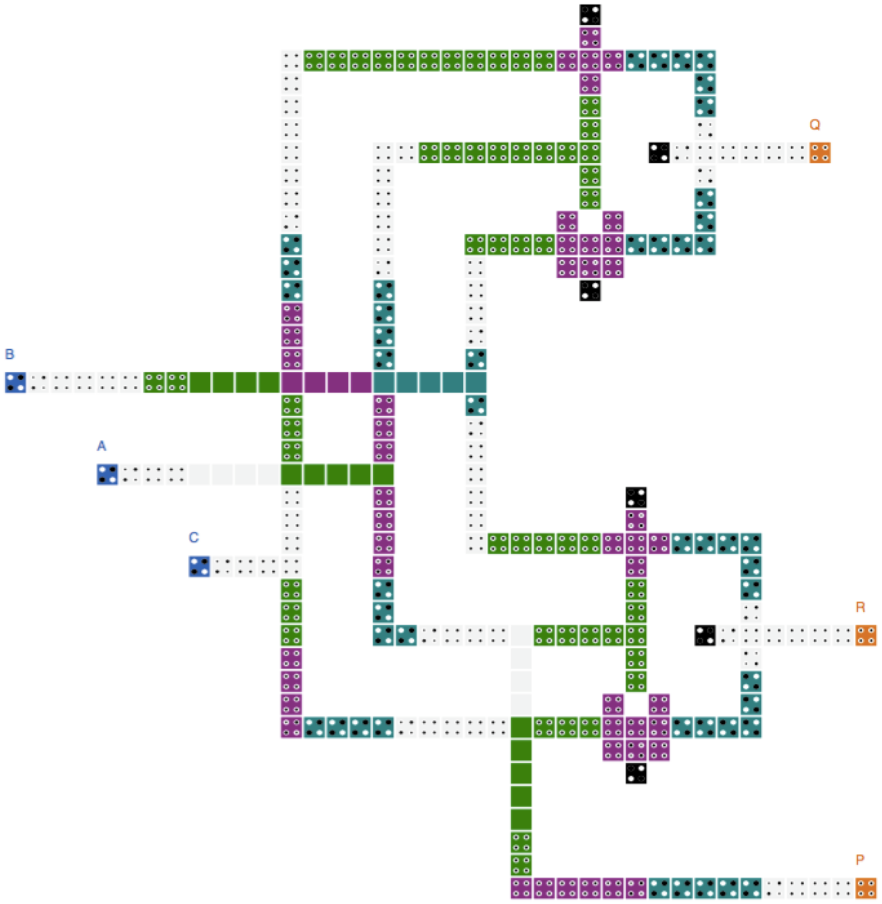
Clock zone 0 in relax phase

Clock zone 1 in release phase

Clock zone 2 In hold phase

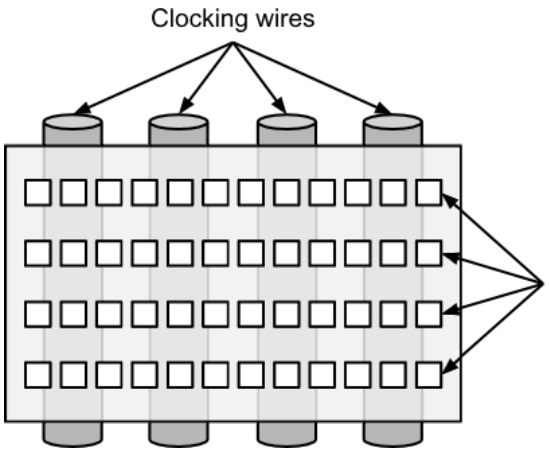
Clock zone 3 in switch phase

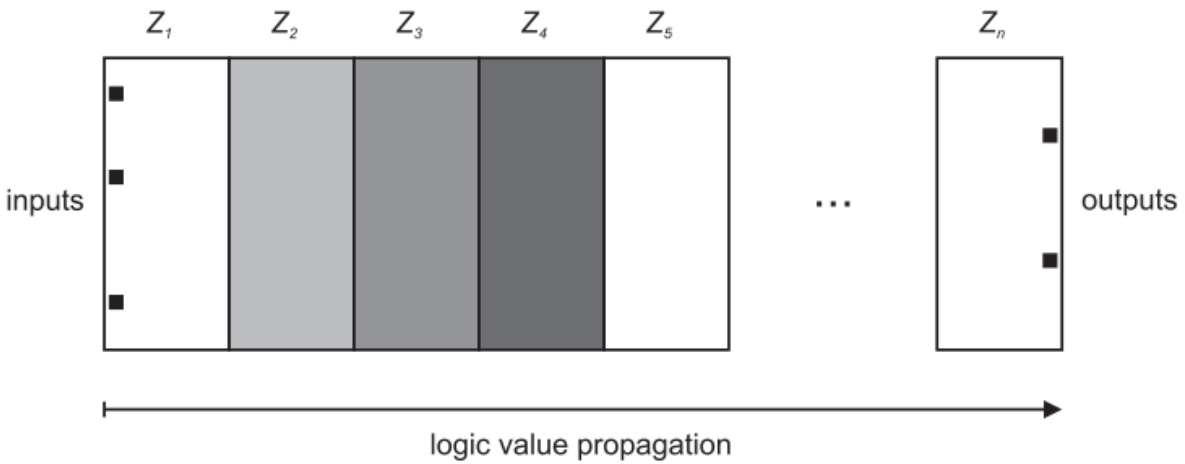
Free clocking scheme



- Colors define clocking zones;
- Designer defines the clocking zones;
- There is no clock standard;
- Does not work in **molecular or magnetic** (nanomagnet logic - NML) QCA.

Linear clocking scheme



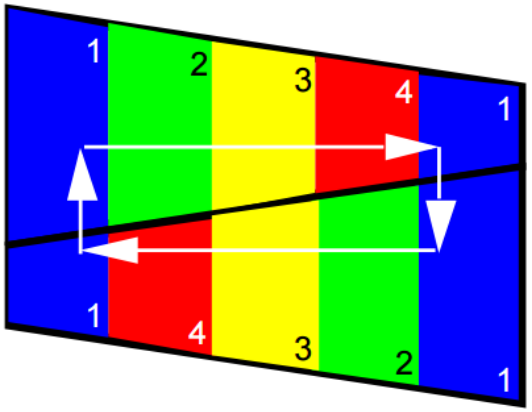


No feedback!

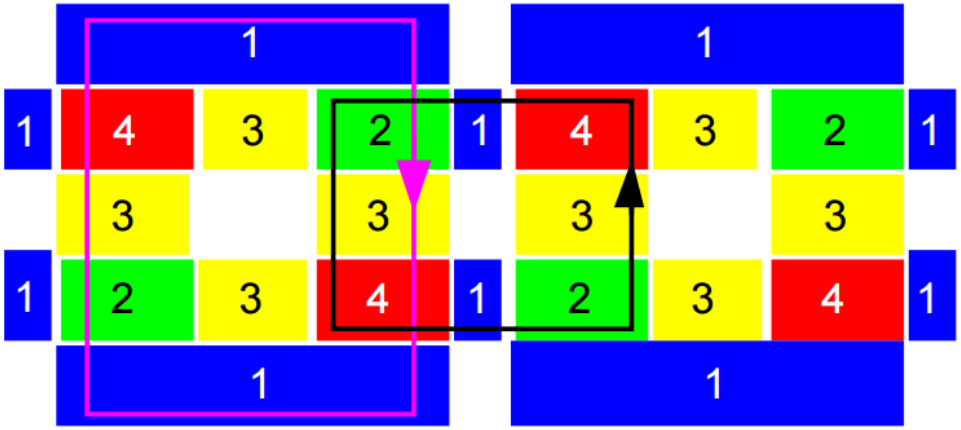
Hennessy, K. and Lent, C. S. (2001). Clocking of molecular quantum-dot cellular automata. Journal of Vacuum Science & Technology B, 19(5):1752--1755.

Janez, M., Pecar, P., and Mraz, M. (2012) Layout design of manufacturable quantum-dot cellular automata. Microelectronics Journal, 43(7):501--513.

Shape clocking scheme



Hard clock circuit implementation

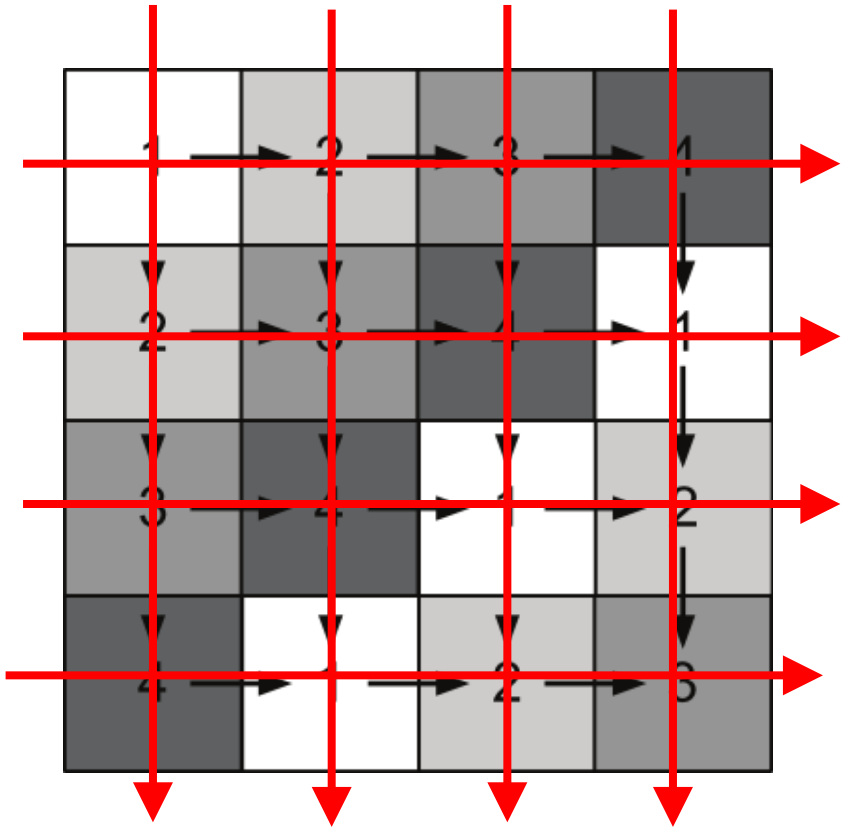


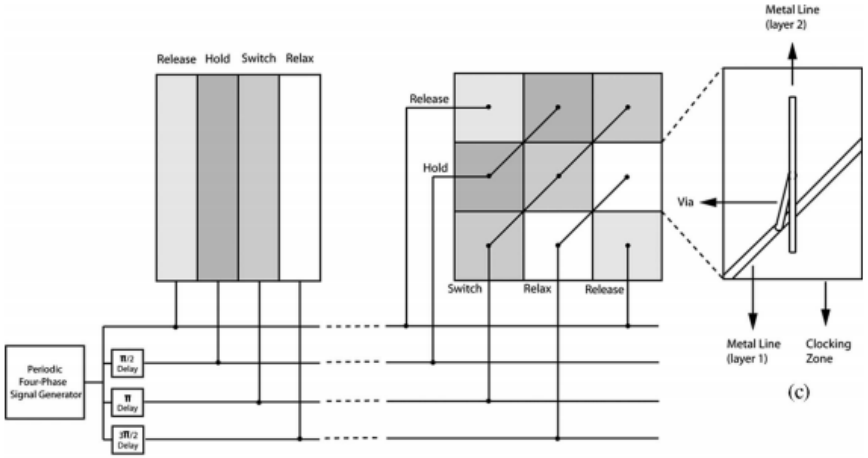
There are more zones 1 and 3 than 2 and 4!

Zones have different sizes and shapes!

Niemier, M. T. (2004). Designing digital systems in quantum cellular automata. PhD thesis, University of Notre Dame.

2DDWave clocking scheme





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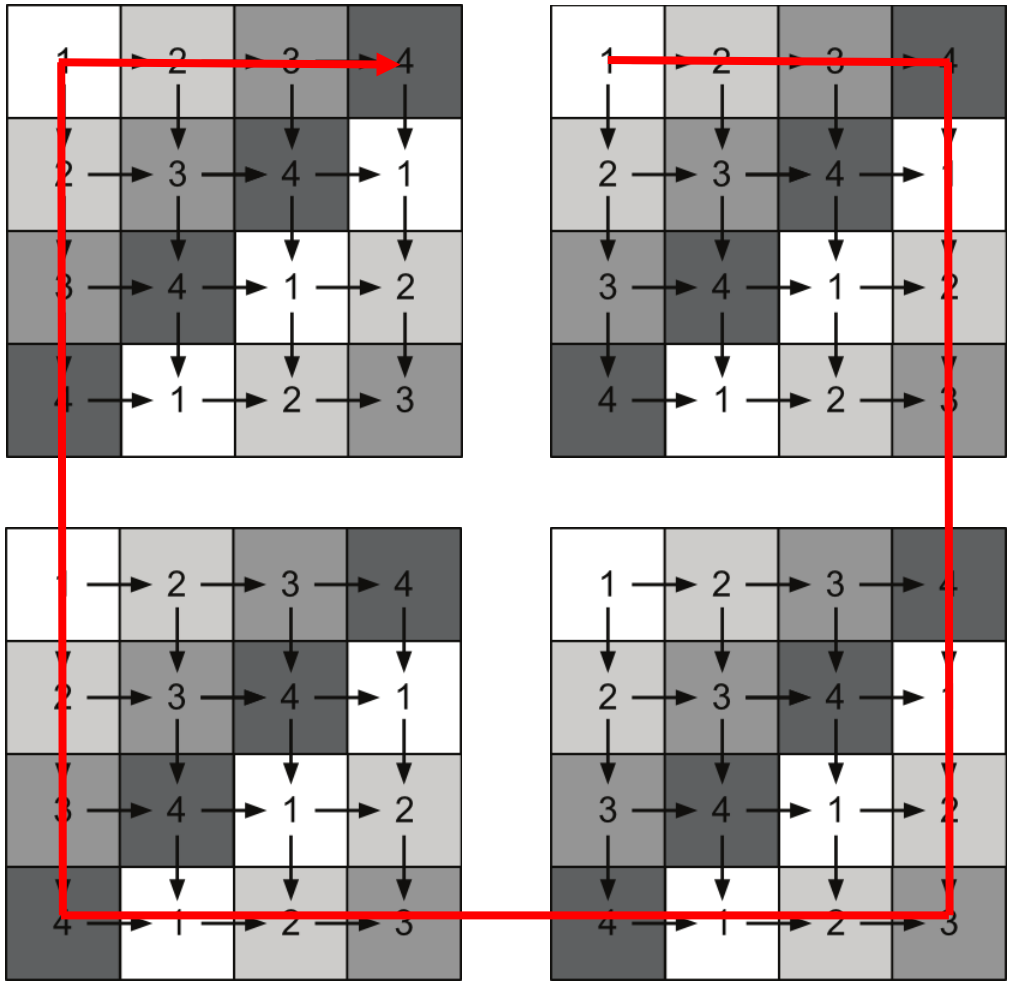

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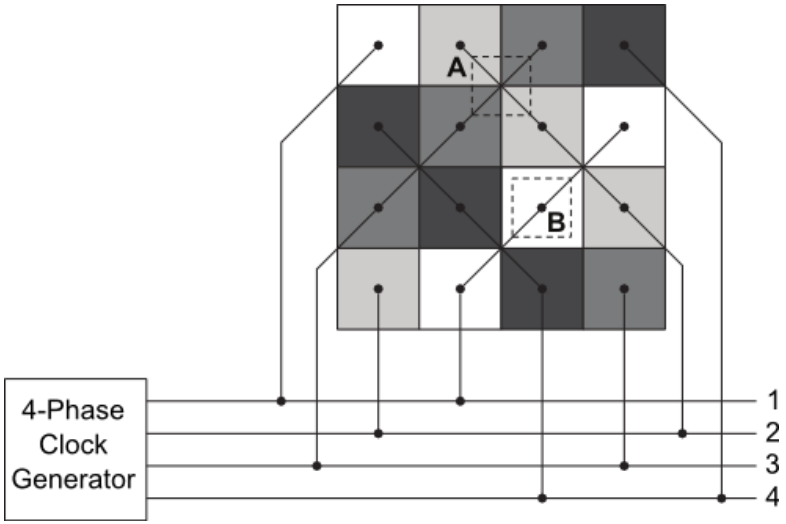
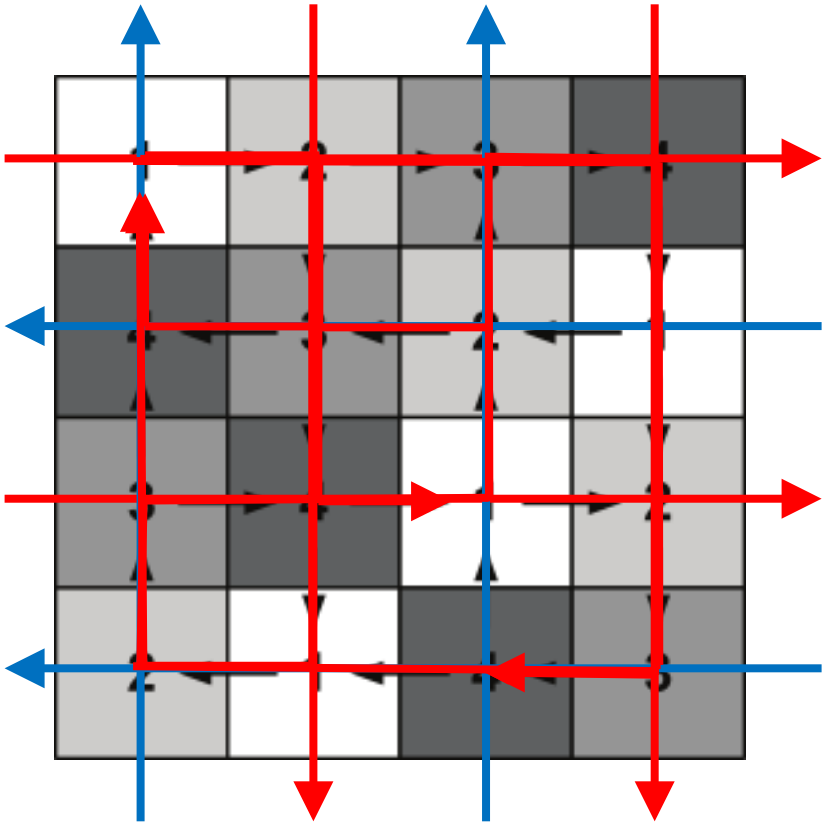
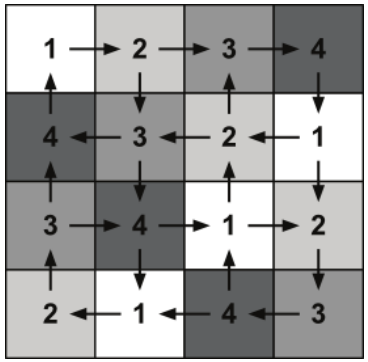
USE clocking scheme

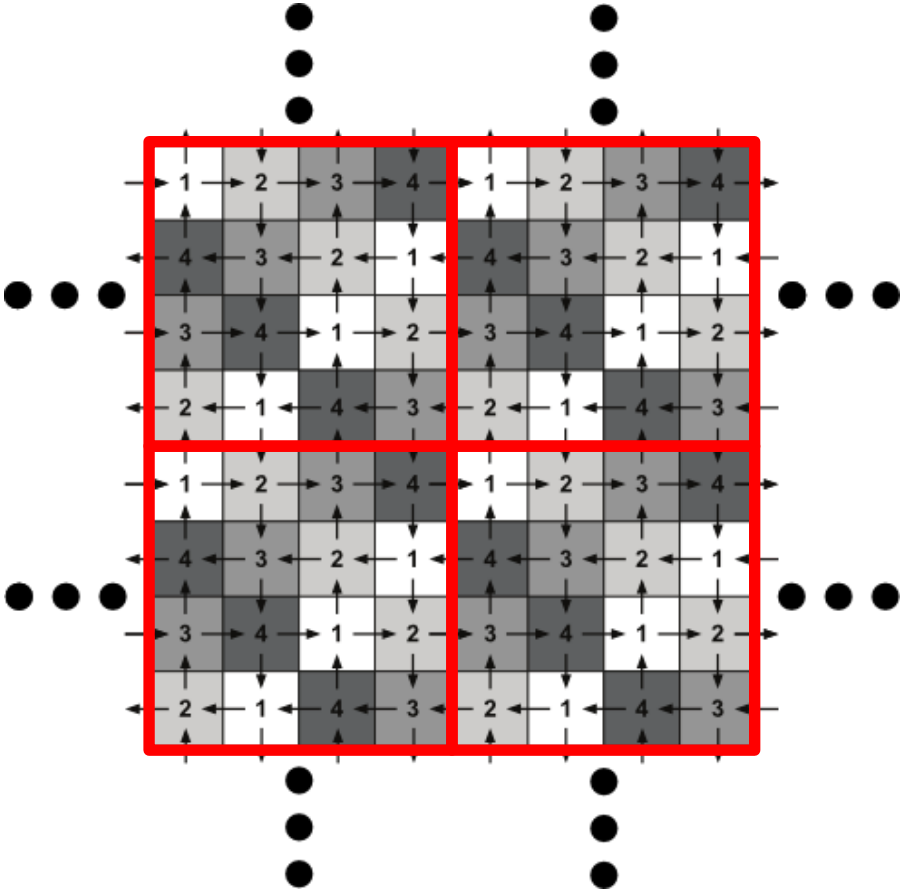




Campos, C. A. T., Marciano, A. F., Vilela Neto, O. P., Torres, F. S. (20016). USE: A Universal, Scalable, and Efficient Clocking Scheme for QCA. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, 35(4): 513--517.

USE clocking scheme





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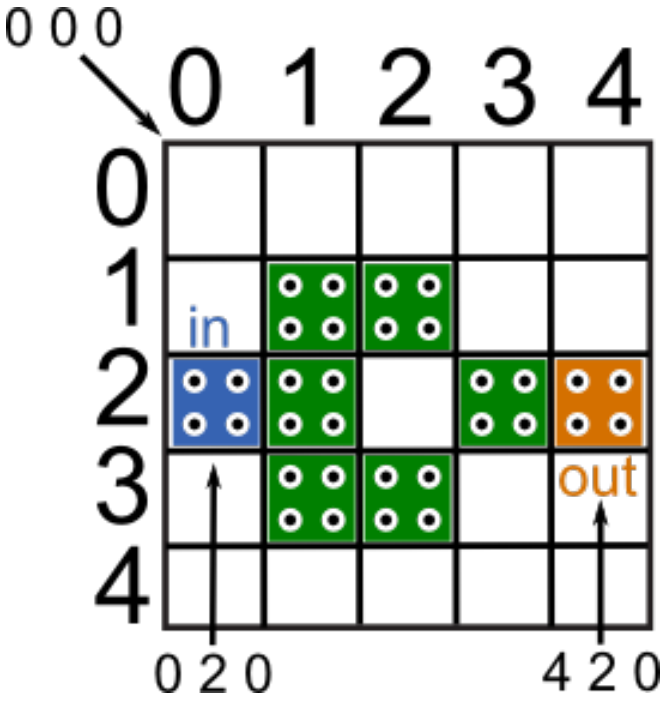
QCA ONE

- QCA Standard Cells;
- Using USE clocking scheme
  - Regular shape;
  - Enable placement & routing.

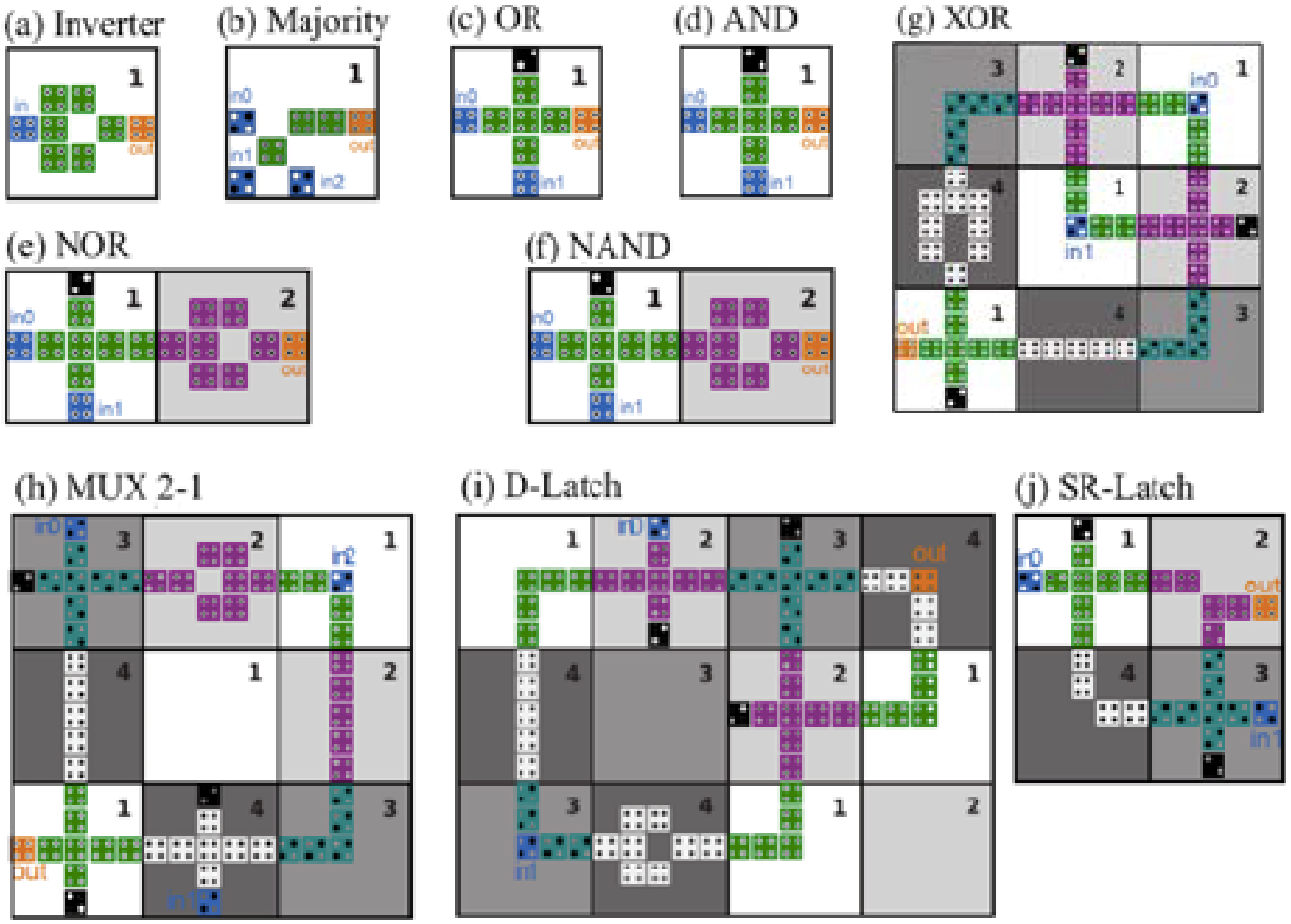
QCA ONE

Inverter

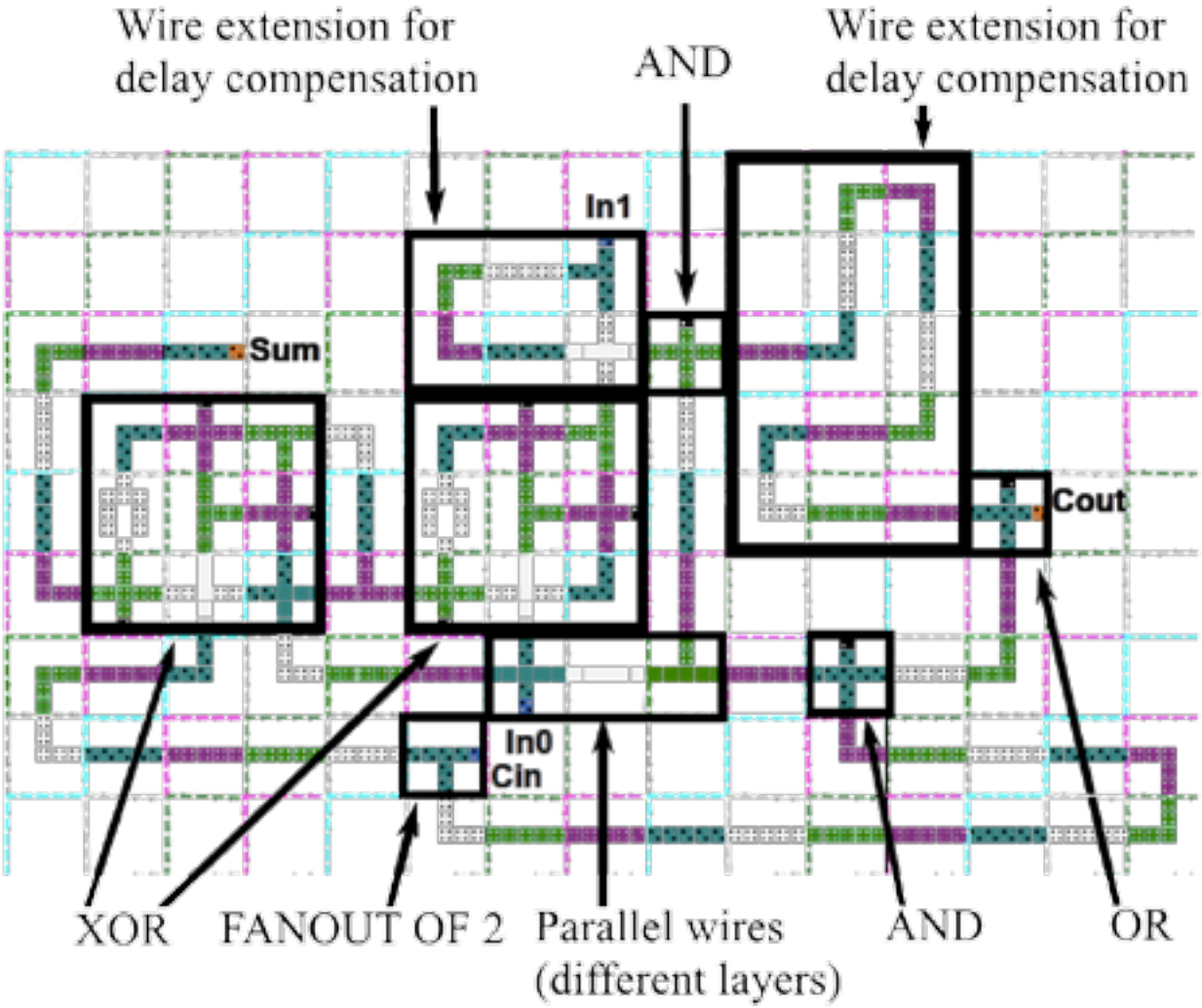



```
name: inv # cell name

n_input: 1 # number of inputs
n_output: 1 # number of outputs
input: in # list of inputs
output: out # list of outputs

expression: # expression corresponding to the function performed
out = -in

zone_dimension: 5 # dimension of USE zone in terms of QCA cells

width: 5 # width in number of QCA cells
height: 5 # height in number of QCA cells
layers: 1 # number of layers used
l_reference_zone: 1 # left reference zone
r_reference_zone: 2 # right reference zone

delay_table: # table of delays between each pair input/output
/   in
out 0

port_location: # coordinates for input and output ports
in   0 2 0
out 4 2 0

free:
```

QCA ONE


(a) Inverter
(b) Majority
(c) OR
(d) AND
(g) XOR
(e) NOR
(f) NAND
(h) MUX 2-1
(i) D-Latch
(j) SR-Latch

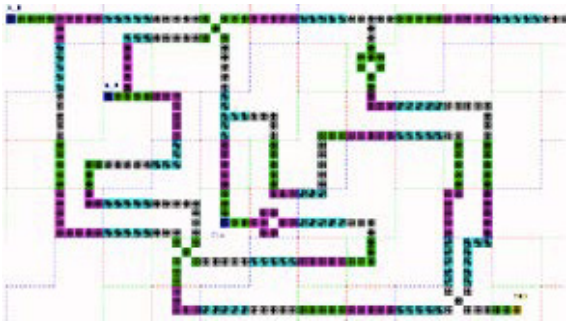
QCA ONE - Results



One bit full adder

QCA ONE - Results

8 bits
Ripple
Carry Adder



Conclusion & Future Works

- We proposed and implemented a QCA standard cell library;
- We presented some no optimized circuits implemented with the cells;

- **Placement and routing** must be developed;
- **More cells** are being created;
- A **QCADesigner** with **USE** and **QCA ONE** will released;
- **Clocking schemes and standard cells** library will be implemented to **NML**.