A novel methodology for robustness analysis of QCA circuits

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ABSTRACT
Although QCA (Quantum-dot Cellular Automata) is a promising nanotechnology to replace CMOS (Complementary Metal-Oxide-Semiconductor), it has several known reliability problems. Consequently, the design of robust QCA circuits is a mandatory step towards the consolidation of this new technology. This paper presents a novel methodology for error analysis of QCA circuits based on deterministic and random insertion of possible defects. Further features are an evaluation of circuit robustness and identification of the most susceptible design elements. Simulation results indicate the feasibility of this novel methodology and reveal starting-points for robustness improvements of known QCA structures.

Categories and Subject Descriptors
B.8.1 [**Performance and Reliability**]: Reliability, Testing, and Fault-Tolerance; B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids; B.6.1 [**Logic Design**]: Design Styles - *cellular arrays and automata*; B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies*.

General Terms
Design, Reliability, Experimentation.

Keywords
QCA; robustness, defects modeling; reliability.

1. INTRODUCTION
According to the Moore's Law predictions, the amount of transistors in a single chip should be doubled every twenty four months [1]. Practical observations have shown that this forecast has been fulfilled until nowadays, thanks to constant miniaturization of CMOS transistors. The vast knowledge of the manufacturing process of these devices, as well as their reliability, made the CMOS technology widely used for the realization of integrated circuits since the late sixties. However, the size reduction of transistors shall not continue to occur uninterruptedly. There are physical limits about to be reached, as evidenced by the problems that are strongly observed in nanoscale devices, such as high power dissipation due to leakage currents [2].

The nanotechnology QCA (Quantum-dot Cellular Automata) [3] is a candidate for CMOS succession [2]. Its fundamental devices are called cells, which can be arranged in a row or in another particular pattern in order to enable the transmission and processing of information. It is important to highlight that the transmission and processing of information in QCA circuits occurs without flow of electrons (electric current), resulting in considerable less power consumption than in the traditional CMOS circuits [4]. Furthermore, the size of cells is typically in the range of few nanometers, so that the design of QCA circuits generally requires less area than its CMOS counterpart. Furthermore, high clock frequencies in the range of several THz are supposed to be achieved [4].

Despite its many advantages in comparison to CMOS, QCA has to overcome several challenges, such as the physical implementation. So far, prototypes of Metal-Island QCA and NML (Nano Magnetic Logic) devices have been successfully implemented [5][6]. Molecular QCA have been widely studied [7] [8] and possess good potential for succeeding CMOS, but no devices or even prototypes have been realized yet. Another challenge of QCA technology is its susceptibility to errors that may occur due to defective cells, caused by variations in the manufacturing process [9]. Consequently, several works focus on the creation of robust QCA structures [10-13] as well as methodologies for error analysis in QCA circuits [14][15]. In order to enable evaluation of circuit robustness and verification of reliability enhancing techniques, this work proposes a novel methodology for error exploration. By means of this methodology, it is possible iteratively insert several kinds of defects in structures and analyze its impact on the operation of the circuit. Furthermore, this methodology is designed such that it can be also applied for other nanotechnologies besides QCA as long as positioning errors are critical for the properly operation of their devices. In this category, self-assembled devices such as DNA-based structures, Nanowires and CNFETs (Carbon Nanotubes Field Effect Transistors) may be highlighted. Some works present the investigation of the influence of defects in the operation of these nanodevices, proposing some error exploration methodologies [16][17].

The remaining paper is organized as follows. Section 2 introduces the QCA technology, while Section 3 focuses on conceptualizing defects and errors, presenting the four classes of QCA cells defects considered in this work. Section 4 introduces the novel methodology. Section 5 discusses simulation results and Section 6 concludes the paper.

2. BACKGROUND

Quantum-dot Cellular Automata (QCA) is a new computation paradigm whose working principle is based on Coulomb interactions between electrons [18]. A cell, which is the basic unit of QCA, can be represented by a square including four circles - one in each of its vertices. The circles refer to quantum dots, which are the specific positions at which an electron can or cannot be. Each cell hosts two electrons confined in those dots. Due to the Coulomb repulsion effect, the two electrons must be as far apart as possible. Consequently, there are two possible logic states (opposite diagonals), which permits a binary logic. By convention, the maximum polarization states, which correspond respectively to logic 0 and logic 1, are called -1 and +1. A cell can continuously assume any polarization level within those limits. The interpretation of the logic state of a cell depends on a threshold. Figure 1 depicts the two possible logic states interpretation, which depends on the comparison between the threshold and the QCA cell polarization level.

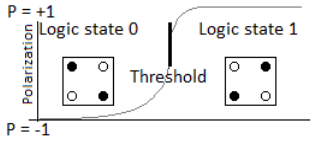

Figure 1. Two possible logic states of a QCA cell. Fulfilled circles indicate a electron confined into a quantum dot.

QCA cells may be arranged in such a way that is possible to transmit information and to perform logic operations. In the following, representative QCA structures are detailed.

2.1 QCA basic structures

The most basic QCA structure is the wire, which can be constructed by arranging the cells side by side as an array. When the polarization state of the first cell of the array changes, subsequent cells tend to assume the same polarization state due to Coulomb interaction effect, enabling the information transmission through the wire without electric current flow. Figure 2(A) illustrates a QCA wire.

Inverter is another basic QCA structure, which can be constructed essentially based on cells arranged in diagonal, which assume opposite polarization states. An example is depicted in Figure 2(B) [3].

The last essential QCA structure shown in this section is the majority gate. The logical value of its output is always equal to the logic value present in the majority of its inputs Figure 2(C) depicts an exemplary 3-input majority gate [3].

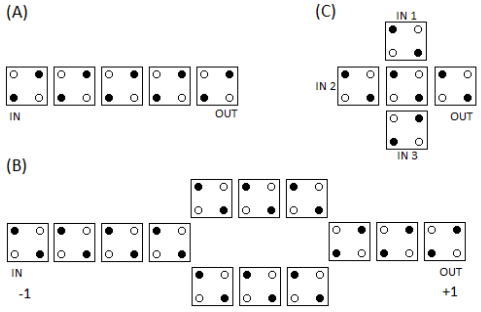

Figure 2. (A) QCA wire. (B) QCA inverter. (C) 3-input QCA majority gate.

The majority gate is considered, along with the inverter, the most important QCA gate. It enables the realization of AND or OR gates. To obtain an AND, one of the majority gate inputs must be fixed at logic state 0. Similarly, in order to obtain an OR, one of the majority gate inputs must be fixed at logic state 1. By using wires, inverters and majority gates any QCA circuit can be created. More complex circuits can be found in the literature [19][20].

2.2 Clocking

One of the main issues of QCA circuits is the switching of QCA arrays, i.e., the change of an array of cells from one state to another. For example, when a polarization change in the input cell of the QCA wire in Figure 2(A) suddenly occurs, the array of cells assumes distinct polarization states at the same time. This could cause the reach of a metastable state of the system which might lead to a significant delay or even to the inability to perform logic or information transport [21]. Adiabatic switching provides a solution for that problem [3]. In its first phase, the interdot barriers of the cells are decreased, removing gradually their old polarization values until they are depolarized. The second phase of adiabatic switching consists in raising cells interdots barriers at the same time as a new state is being applied to the input. The increased interdot barriers allow the repolarization of the cells into well-defined bistable states, reaching the ground state corresponding to the new inputs.

The approach aforementioned takes into account the adiabatic switching happening to all cells in the array at the same time. However, the array can be divided into subarrays (e.g. clock-zones), whereas each of them is in a different clock phase at a time. By means of the use of clock zones, a QCA subarray can perform some logic, has its states frozen and finally provide input to the next subarray, which must be in a distinct clock-zone. Moreover, this clocking strategy allows the information synchronism, avoids backpropagation due to the QCA duplex nature (symmetric behavior) and increases the probability of successful switching by limiting the length of QCA wires in a circuit [3].

3. ERRORS IN QCA CIRCUITS

Defects are flaws of the cells of a circuit, generally caused by manufacturing process variations. Defects can occur regardless of the technology and are subject of several researches for different technologies, such as CMOS [22] and Carbon nanotubes [23].

Errors are unexpected deviations in the behavior of a system. In the circuits context, an error occurs when, given a known input vector, the state of the outputs is unexpected. Errors can happen due to defects or even external factors.

A defective circuit can or cannot be an erroneous circuit, depending on the integrity of the response of its outputs. If the circuit is able to perform correctly its function, even when defects are present, they cannot be considered as erroneous. A great challenge for designers is to design reliable systems, which are able to get along with defects and other external factors.

Most of the reports in the literature regarding defects in QCA circuits are related to displacement and misalignment of the cells. Temperature effects are also occasionally investigated [6]. Defect classes of this work have a nomenclature similar to those reported in [15], which is based on an analogy to a two-dimensional crystal lattice. They are more detailed in the following subsections.

3.1 Dopant

Cells with dopant defects are unable to change their polarization state, or do it in an inefficient way. One or more dots left over or missed from a QCA cell can create a dopant defect, as illustrated in Figure 3.

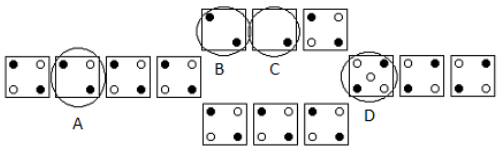

Figure 3. An inverter with dopant defects. In A, a quantum-dot is missing. In B, two quantum-dots are missing. In C, only one dot remains in the cell. At last, in D, there is a left over dot in the middle of the cell.

3.2 Dislocation

Dislocation defects are caused by cells that are moved around its axis (rotated), as illustrated in Figure 4.

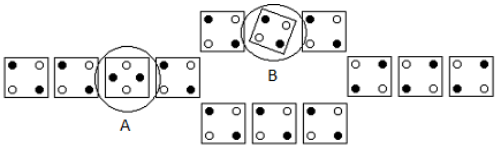

Figure 4. An inverter containing dislocation defects. Cell A is rotated around its axis by ninety degrees, while the rotation of cell B is about thirty degrees.

3.3 Vacancy

Vacancy defects happen when all dots of the same QCA cell are missing, as illustrated in Figure 5.

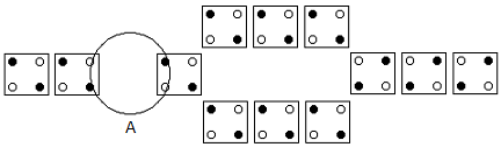

Figure 5. An inverter with a missing cell at position A.

3.4 Interstitial

Interstitial defects are caused by cells that are displaced in the horizontal / vertical axis in relation to the other cells of a QCA circuit, as illustrated in Figure 6.

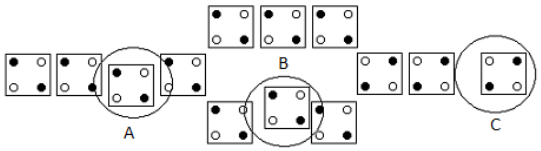

Figure 6. An inverter with interstitial defects. Cell A is displaced in the vertical axis. Cell B is displaced in both vertical and horizontal axis. At last, cell C is displaced only in horizontal axis.

Defects can cause polarization loss in QCA cells, affecting the transmission of information through a circuit. In more severe levels, polarization loss can induce undesirable logic states to other QCA cells of a circuit due to the reach of a metastable state [21]. A theoretical and experimental analysis of misalignment and displacement defects and their consequences can be found in [9]. Shifts within the range of 0 to 30% of the cell size are related to significant polarization losses, especially in 1-cell width devices, i.e., devices with no redundancy mechanisms. In general, a greater shift leads to stronger polarization losses.

In a QCA circuit, defects of distinct classes may be inserted into the same cell. Likewise, defects of a same class may be inserted into different cells. Both situations can cause error events in a circuit, not necessarily at the same proportion. The establishment of a cross-reference between defective cells and the error occurrence rates is crucial. Through that, a circuit can be mapped according to the contribution of its cells to the amount of its error occurrence rate.

4. NOVEL METHOLODOGY

Several methodologies for error exploration in QCA circuits have been previously proposed. In the following, two of them are exposed in more details. In [14], omission, displacement and misalignment defects of QCA cells are characterized by means of simulations. Insertion of defects into the cells obey a pre-established pattern, which means that in every simulation known cells are selected to be defective. The displacement/misalignment parameter *d* sets a shift value to each cell. Results are presented for a 3-input majority gate, a double wire and an inverter chain. The nature of the errors detected is presented as a correlation between the value of *d* and the position of the defective cell. All results of this work are shown by means of several tables, which is not always convenient, especially when numerous simulations are performed. Moreover, the methodology does not allow sufficient flexibility for defects insertion, once the defect insertion patterns are pre-defined. The methodology described in [15] applies a more extensive defect model consisting of four distinct defect classes: Dopant, dislocation, interstitial and vacancy. Similarly as in [14], defects are modeled by means of simulations. The methodology allows flexibility for defects insertion by means of probability models. However, the paper reports no results.

This section introduces a new methodology for error exploration, designed to be flexible and efficient. Defects are inserted into circuit cells according to user-set parameters. Thus, the circuit operation under different conditions can be verified. The error detection occurs by means of comparisons between simulations results of a reference circuit (defect-free) and of the very same circuit subjected to defects. Error events are registered for each simulation performed, so that when the whole process is completed, the percentage of error-free simulations can be obtained as well as a design heat map. The flow is illustrated in Figure 7. Subsections 7.1-7.3 provide a detailed explanation of each of the flow steps, grouped into three primary categories.

4.1 Initial procedures

The initial procedures of the novel methodology require user interaction. They comprise the circuit selection, the parameters setting and the start of the iterative process for error simulation. First of all, a design to be analyzed must be selected. It should be implemented in a tool like QCADesigner [24]. Once the design is selected, error simulation parameters must be set. The predicted parameters are briefly described in items 4.1.1-4.1.5.

4.1.1 Sample interval

The "Sample Interval" parameter defines the frequency with which the output signals of a QCA circuit should be read. The parameter value is a percentage of the frequency of the clock

signals, *e.g.* a value of 50% means that the sample frequency is half of the frequency of the clock signals.

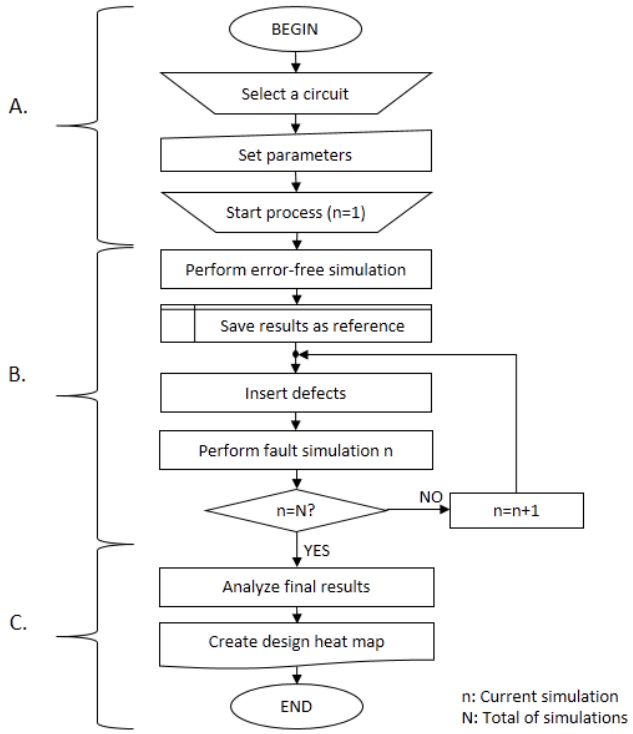

Figure 7. The proposed error simulation flow, where the main steps are identified with letters A-C.

4.1.2 HIGH/ LOW thresholds

"HIGH threshold" parameter determines the percentage of the value of polarization (+1) from which the logic state is interpreted as logic 1. Likewise, "LOW logic level" parameter determines the percentage of the value of polarization (-1) from which the logic state is interpreted as logic 0.

4.1.3 Defect classes

This parameter defines one or more classes of defects that can be inserted into a cell during analysis. Several possibilities were previously detailed in Section 3. The actual insertion of a defect into each cell depends on the probability value assigned to every defined defect class. This assignment may vary according to the probability model chosen. Probability models are explained in the following.

4.1.4 Probability model

Probability model defines the strategy of defect insertion into each cell of a design. There are three possible options for this parameter.

4.1.4.1 Sequential

Defects are inserted into every cell in a design in a sequential manner. That means, a defect is selected out of the defined defect classes and inserted into a single cell at a time. Each defect class has a selection probability equal to the inverse of the total number of classes defined. Next, a simulation is performed. The two processes (defect insertion and simulation) must be run for all cells of the design.

4.1.4.2 Assignable

One or more defects out of the defined defect classes might be inserted into the cells of a design. The probability of a defect insertion into each cell is manually assigned to every defined defect class. Defect insertion process must run repeatedly from the first to last cell in the design. Afterwards, a simulation is performed.

4.1.4.3 Uniform

The defect insertion process for "Uniform" probability model is analogous to "Assignable" probability model. However, the probability value for defect insertion into each cell is now fixed. Its value is given by the inverse of the amount of cells in the design. Hence, it is expected to have an average of one failure per simulation

Probability model selection as well as value assignment for probabilities should consider the device manufacturing process in question. That attribution may not be trivial, especially for emerging nanotechnologies such as QCA, since their manufacturing process is not yet established. Thus, the parameter setting may be based on other mature technologies, whose manufacturing processes are already well consolidated.

4.1.5 Number of iterations

Defines how many times the whole process (defect insertion, simulation and error analysis) is performed. In case of the probability model "Sequential", this value indicates how many times the whole process is executed for each cell of the circuit.

After the design has been selected and all parameters have been successful set, the error simulation process is ready to be started. From this moment on, the methodology does not require any further user interaction.

4.2 Intermediate procedures

The intermediate procedures of the methodology comprise the process of defect insertion, simulation and error detection. First of all, a defect-free simulation is performed. The result of this simulation is saved as reference for determining error events in next simulations. After, defects are inserted into some cells of the design, according to the probability model set. Defect levels, e.g. absolute values of dislocation, interstitial and dopant (dot chosen to be removed), from each cell are randomly chosen. The interstitial displacement and misalignment limits are fractions of the defective cell size (width / length), within the 0 to 100% range. Thus, quantum dots may exceed the limits of a cell and entering neighboring cells. Higher values of the parameter "Number of iterations" lead to more possibilities for error exploration, except when the parameters "Probability model" and "Defect class" are set simultaneously to "Sequential" and "Vacancy". At this specific situation, the concept of defect level may not be applied and the defective cell in each simulation is pre-defined.

After the defect insertion round, a simulation is performed. Output signals obtained from this simulation are then compared to those from the reference. Detected error events as well as the identifications of defective cells in the circuit are registered. The whole process is repeated until the amount of iterations reaches the number specified by the parameter "Number of iterations".

4.3 Final procedures

The final procedures of the methodology regard to the results analysis. Based on the registered information of all simulations, the percentage of error-free simulations is calculated. Further, a cross-reference between error events and defective cells is established, which allows the creation of a heat map.

A heat map is a graphical representation of the cross-reference between error events and defective cells. For each cell in a circuit, a color from a pre-defined range of colors is used in order to indicate how often defects inserted into that cell lead to an error. Figure 8 shows the range of colors applied here.

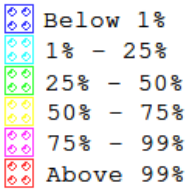

Figure 8. Colors and their respective ranges for heat maps. Defects inserted into dark blue cells led to error events in a circuit in less than 1% of the simulations, i.e., for every 100 defects inserted into the cell, no more than one of them resulted in an error event. Defects inserted into light blue colored cells led in 1-25% of all simulations to an error. Analogous reasoning may be applied to light green, yellow and pink colored cells complying with their respective percentage ranges indicated in the illustration. Defects inserted into red colored cells led in more than 99% of the simulations to an error.

5. RESULTS AND DISCUSSION

The methodology described in Section 4 was implemented as extension to the tool QCADesigner [24]. The software itself, its source code, as well as its full documentation are available over the internet [25].

Two different implementations of three circuits (INVERTER [3][10], MAJORITY [3][11] and FULL ADDER [12] [13]) were subjected to the methodology. Simulations were performed using all four defect classes described in [15] and Section 3.

For all tests, QCADesigner simulation engine was set to "Coherence Vector". Error simulation parameters "Sample Interval" and "LOW/HIGH Threshold" were set to 10%, 80% and 80% respectively. Further, the probability value for individual defect classes was set to 5%. Results can be found in Table 1 and Table 2.

For each test performed, a design heat map was created. Six exemplary heat maps are depicted in Figures 9-11.

Table 1. Error-Free Simulations (%)*

	INVERTER		3-INPUT MAJORITY		FULL ADDER	
	INV1 [3]	INV2 [10]	MJ1 [3]	MJ2 [11]	FA1 [12]	FA2 [13]
Vacancy	74.6	**86.1**	**60.6**	30.3	2.8	**16.2**
Interstit.	97.4	**99.9**	**94.3**	87.9	54.9	**76.0**
Dopant	83.7	**88.6**	**75.8**	31.1	3.7	**26.2**
Dislocat.	88.6	**93.9**	**78.5**	67.2	25.9	**51.0**

*Probability model=Assignable; Number of iterations=1000; Probability value for individual defect classes=5%.

Table 2. Error-Free Simulations (%)*

	INVERTER		3-INPUT MAJORITY		FULL ADDER	
	INV1 [3]	INV2 [11]	MJ1 [3]	MJ2 [10]	FA1 [18]	FA2 [17]
Vacancy	60.0	**83.3**	11.1	**89.9**	**26.6**	0.0
Interstit.	96.0	**100**	87.8	**98.9**	50.9	**83.9**
Dopant	69.0	**80.8**	42.2	**85.2**	0.0	**37.4**
Dislocat.	88.0	**90.8**	61.1	**95.2**	**77.2**	39.0

*Probability model=Sequential; Number of iterations=10 for interstitial, dopant and dislocation defect classes. 1 for vacancy defect class.

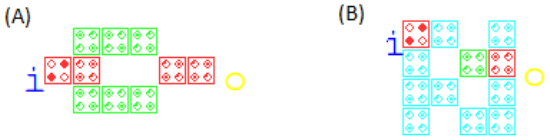

Figure 9. Heat maps of INV1 (A) and INV2 (B) for 1000 tests under vacancy defects where "Assignable" probability model was set.

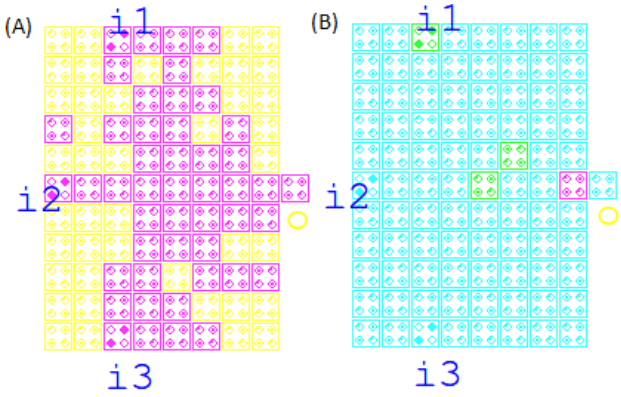

Figure 10. Heat maps of 3-input majority gate MJ2 for 1000 tests under dopant defects (A) and interstitial defects (B). Probability model was "Assignable".

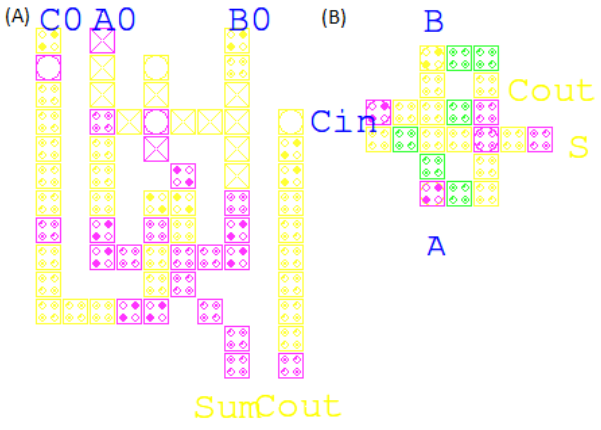

Figure 11. Heat maps of 1-bit full adder FA1 (A) and FA2 (B) for 1000 tests under dislocation defects where "Assignable" probability model was set.

Results indicate that INV2 had a higher percentage of error-free simulations for the probability models "Assignable" and "Sequential". Error-free simulation percentage for INV2 was always above 80 %, and among all the circuits tested, it was the most reliable.

According to [11], majority gate MJ2 is supposed to be more reliable than gate MJ1, but the results of the tests revealed no superiority in terms of robustness for the probability model "Assignable". When the probability model "Sequential" was applied, MJ2 had an absolutely higher performance in all classes of defects. One possible explanation for this is that MJ2 has a large number of critical cells. When several of these cells present defects at the same time, the circuit integrity is affected.

Regarding Full Adders FA1 and FA2, the error-free simulations values found were in most cases very low, surpassing the percentage of 70% in just 18.75% of the simulations. This demonstrates that there is still plenty of room for proposals of more reliable adders. Comparing FA1 and FA2, only the tests that used "Assignable" probability model showed superiority of FA2 compared to FA1.

Figure 9 shows that INV1, less robust than INV2, has in fact a great proportion of high critical cells (identifiable by the amount of red cells). Based on the heat maps in Figure 10, it is interesting to note that tests performed under the same probability model provide distinct results, because different defect classes have been used in both cases. Therefore, it can be concluded that the circuit robustness and cross-reference between defective cells and errors also depends on the defect class that the circuit is subjected to.

Finally, the heat maps in Figure 11 indicate that circuits have critical regions. In those regions, defects will result in errors more easily. Generally, critical regions perform logic operations, as can be observed in FA1: Its critical region comprises mostly the cells that form the 5-input Majority Gate built-in within its structure.

Based on error simulation results, defect classes that cause errors in a circuit more frequently can be identified. Similarly, critical regions of a structure can be mapped, i.e., regions where the presence of defects often leads to error events. Such information may provide support to establish production requirements for different structures. Moreover, results allow identifying the weaknesses of the circuits aiming to propose specific changes in existing structures or design novel structures that are more reliable. In both situations, the use of the methodology described in this work provides support to enhance robustness techniques.

6. CONCLUSION

QCA is a promising technology candidate for CMOS succession. The development of more reliable structures is one important step, though, to enhance the probability that QCA might be applied for future applications. Although there are some researches in the field of defects and error simulation for QCA circuits, there are not many tools available for turn the design of these structures into a less tough task. This paper presents a novel methodology that can be valuable for designers developing new robust QCA structures. The feasibility of the presented methodology could be proven by simulation results. Further, it could be identified initial points for robustness improvements of know QCA structures.

7. ACKNOWLEDGMENTS

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