Pipelined SAR with Comparator-Based Switch-Capacitor Residue Amplification

Frank Sill Torres, *member IEEE,* Pedro Henrique Köhler Marra Pinto
Department of Electronic Engineering / Universidade Federal de Minas Gerais
Av. Antônio Carlos 6627, 31270-901, Belo Horizonte (MG), Brazil
franksill@ufmg.br

***Abstract*— This work presents the implementation of an 11 Bit pipelined successive approximation register ADC (PSAR) in a 65 nm technology. The proposed ADC utilizes comparator-based switch-capacitor circuits and zero-detection in order to enable fast and high linear residue amplification with at reasonable area costs. Simulation results indicate conversion rates of 4.4 MSPS and energy consumption of 48.8 fJ per step.**

Keywords— Switched capacitor circuits, Analog-digital conversion, Analog-digital integrated circuits, Zero-Crossing Detection

I. Introduction

Analog-to-Digital Converters (ADCs) are essential devices in mixed-signal circuits. Its wide field of applications and requirements resulted in various converter types, *e.g.* integrating ADC, successive approximation ADC, flash ADC, pipelined ADC, and sigma-delta ADC [1]. Each of these converters has its preferred tasks. However, for selected applications it is useful to combine different ADC concepts in order to obtain the best trade-off between power dissipation, area, and conversion speed.

A common challenge of pipelined ADC is the realization of high linear and fast residue amplification between each conversion stage. Amongst the several solutions the comparator-based switch-capacitor approach with Zero-Crossing Detection (ZCD) is a promising technique especially for implementation in technologies below 100 nm [2-4].

The ADC presented in this paper combines the concepts of pipelined ADC with successive approximation and applies the comparator-based switch-capacitor for residue amplification. Further, an improved ZCD circuit is proposed in order to enable high linear and fast residue amplification.

The rest of this paper is organized as follows. Section II introduces the general architecture of the implemented ADC. Section III focuses on the circuits for residue amplification and section IV presents simulation results. Finally, section V concludes this work.

II. Pipelined Successive Approximation Register

This section introduces the concept of the implemented Pipelined Successive Approximation Register (PSAR) and details its control.

A. Successive Approximation Register (SAR)

Successive approximation is a popular approach for ADCs which require moderate conversion times at low area and power demands [1]. The main principle bases on successive halving of the intermediate results and comparison with the input value. Thereby, the number of steps determines the resolution of the ADC.

B. Pipelined ADC (PADC)

Converters focusing on high conversion rates are commonly based on the Flash ADC architecture [5, 6] or on the pipelined ADC principle [7, 8]. The latter enables a considerable high conversion rate by dividing the conversion in sub-steps, which raises the throughput by the same amount. The drawback is a longer latency since the conversion result is only available after all sub-units finished its processing.

C. Pipelined SAR (PSAR)

The pipelined ADC principle can be combined with different architectures, like the Flash-ADC [9] or the successive approximation register [10-13]. The former enables high speed at the cost of power and area. In contrast, the pipelined SAR (PSAR) offers a promising compromise between moderate conversion rates as well as power and area demands.

D. PSAR Structure

Fig. 1 depicts the scheme of the implemented PSAR. It consists of two 3 Bit SAR (SAR3) and a 4 Bit SAR (SAR4), which are connected to a residue amplifier (ResAMP). The control of the PSAR is realized by the digital "Control and Time Alignment Logic". Further, each SAR works with charge redistribution whereas the value of the applied capacitances increases by factor two. It should be noted, that the base capacitance value C_b of the SAR4 is only the half of its counterpart in the SAR3. This has no considerable impact on the conversion error, as the final conversion stage has lower requirements on the conversion precision. Additionally, each SAR contains a dynamic comparator.

The implemented unipolar PSAR applies a common-mode voltage V_{CM} which is equal to the half of the reference voltage V_{REF}, *i.e.* $V_{CM} = V_{REF}/2$.

E. PSAR Control Scheme

The SARs presented in Fig. 1 work in different phases controlled by the clock signal. The phases are:

- **LOAD**: Read new input voltage into the SAR
  - Mux M*0* connects net M0OUT with input VIN (voltage level V_{in}), thus the voltage level of M0OUT changes to $V_{M0} = V_{in}$
  - Bits 1 to n and CTRL are set to high (*i.e.*, '1'), thus mux M*1* to M*n+1* connect capacitors with M0OUT
  - Switch S0 connects VINT with VCM

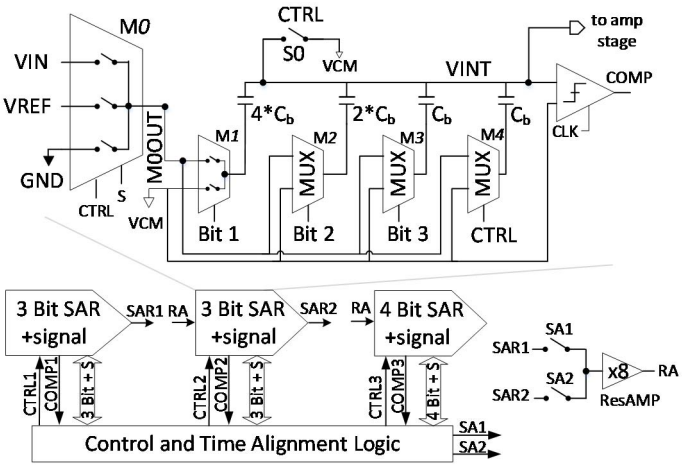

Fig. 1. Structure of the implemented pipelined SAR ADC

- **CHECK S**: Resetting of SAR's output bits and check whether $V_{int} > V_{CM}$ and set B1
  - Switch S0 is disconnected
  - Bits 1 to n and CTRL are unset to low (*i.e.*, '0'), thus M1 to M*n+1* connect the capacitors with VCM
  - Voltage level V_{int} of VINT changes to $V_{int} = V_{CM} - (V_{in} - V_{CM}) = 2 \cdot V_{CM} - V_{in}$
  - Depending on the comparator output COMP it can be determined whether V_{in} is below or above V_{CM}
    - If $V_{in} < V_{CM}$ (i.e. $V_{int} > V_{CM}$, COMP = '1'): mux M*0* connects its output M0OUT with GND (*i.e.*, V_{M0} changes to $V_{GND} = 0V$), unset S (*i.e.*, S = '0')
    - If $V_{in} > V_{CM}$ (i.e. $V_{int} < V_{CM}$, COMP = '0'): mux M*0* connects its output M0OUT with VREF (*i.e.*, $V_{M0} = V_{REF}$), set S (i.e. S = '1')
  - Set Bit 1
  - V_{int} changes to $V_{int} - (V_{CM} - V_{M0})/2$
- **SET Bx**: Successive bit setting and result estimation
  - After Bit x is set V_{int} changes to $V_{int} - (V_{CM} - V_{M0})/2^x$
  - COMP = S indicates that V_{int} crossed V_{CM} and the previous Bit x-1 is unset which changes V_{int} to $V_{int} + (V_{CM} - V_{M0})/2^{x-1}$
- **LAST BIT**: Estimation of result for last Bit (Bit n)
  - Processing of comparator output following scheme of phase SET Bx
- **TRANS**: Generation of input signal for the next stage (only 1st and 2nd SAR)
  - V_{int} is equal to sum of residue and V_{CM}
  - Connect VINT to residue amplifier
  - Set signal SA1 or SA2 depending on the residue to be amplified

Fig. 2 depicts the order of the phases of each SAR. It follows that after seven clock cycles a new result is available at the output of the PSAC.

Based on the control scheme the binary conversion result must be transformed in the following manner:

- **1st SAR3 / SAR4**
  - If S = '0': invert Bx (*i.e.*, Bx = ~Bx)
  - If S = '1': Bx stays (*i.e.*, Bx = Bx)
- **2nd SAR3**
  - If S = '1': invert Bx (*i.e.*, Bx = ~Bx)
  - If S = '0': Bx stays (*i.e.*, Bx = Bx)

Further, the signal S of the first SAR3 indicates the first bit of the final binary results. Thus, the presented PSAR is an 11 Bit ADC.

In order to enable high conversion rates the residue amplifier (ResAMP) separates the sample phase **LOAD** of the input voltage, *i.e.* the sum of residue voltage and V_{CM}, and the amplification phase **AMPL**. However, this configuration creates a conflict with the 2nd SAR3, which enters the phase LOAD (2. CLK) directly after the phase TRANS (1. CLK). Consequently, it must be possible to store a sampled voltage on an additional capacitor, which is realized during phase **STORE**. Before amplification, the stored voltage must be sampled into ResAMP, which is done during phase **LD ST**. Fig. 2 shows the order of the phases of the residue amplifier. It should be noted that during phase STORE (1. CLK) the amplifier holds internally the residue voltage of the 1st SAR3 sampled in the previous phase LOAD (7. CLK).

III. Residue Amplifier

The amplification of the residue is a sensitive step as high linearity is required over a considerable range ($V_{CM} \pm V_{REF}/16$) for a high amplification factor (x8). Common solutions apply closed-loop [12] or open-loop opamp-based circuits [14]. However, in the context of scaled technologies in the nanometer era several challenges complicate the design of operational amplifiers (opamps). This includes, for example, lower supply voltages resulting in lower dynamic ranges, and lower output resistances resulting in lower opamp gains.

A. Comparator-based switched capacitor amplifier

CLK	1st SAR3	2nd SAR3	SAR4	ResAMP
1.	LOAD	TRANS	SET B3	STORE
2.	CHECK S	LOAD	SET B4	AMPL
3.	SET B1	CHECK S	LAST BIT	LD ST
4.	SET B2	SET B1	LOAD	AMPL
5.	SET B3	SET B2	CHECK S	
6.	LAST BIT	SET B3	SET B1	
7.	TRANS	LAST BIT	SET B2	LOAD

Fig. 2. Phases of each SAR and the amplifier (ResAMP)

A promising solution for precise and fast residue amplification is the comparator-based switched capacitor residue amplifier (CBSC-RA) proposed in [2]. Its principal idea is the application of a circuit for Zero-Crossing Detection (ZCD) to detect a virtual ground condition in order to trigger signal amplification.

Fig. 3 depicts the architecture of the implemented residue amplifier, which is an improved modified version of the initial proposal in [2]. Principal differences are an additional voltage follower stage, with bias voltages VB1 and VB2, the removal of the overshoot cancelation, a second current source that is triggered by the output voltage, and a storage capacitor CS. The first change is a consequence of the different virtual grounds of the amplifier and the SAR, which is V_{CM} in case of the amplifier and a combination of V_{GND} and V_{REF} in case of the SAR. The removal of the overshoot cancelation was possible due to the fast response time of the ZCD, which will be detailed below. The second current source (IS' in Fig. 3) compensates the increase of the output resistance of the principal current source (IS in Fig. 3) for high output voltages. The capacitor CS is applied for storage of a sampled voltage (see also section II).

The control scheme of the enhanced CBSC-RA is shown in Fig. 4a. In the initial phase, the voltage V_{in} of input VIN is sampled on the capacitors C1 and C2 with VCM as virtual ground (signal φ1). The following charge transfer phase starts with the preset of the output VOUT to GND (φ3), the connection of bottom plates of C1 and C2 with the ZCD's input (φ2), and the connection of the top plates of C1 and C2 to VCM and VOUT (φ2), respectively. Consequently, the voltage level of VZCD changes to V_{CM}. Next, the charging of VOUT is enabled (φ4), which increases the level of VOUT as well as VZCD. In case of amplified voltages above V_{DD}-V_{th}, with V_{th} is the transistors threshold voltage, the 2nd current source is additionally activated (φ4'). The charging phase is canceled in the moment the voltage of VZCD crosses V_{CM}. Hereby, the response time of the implemented ZCD is sufficient (below 1 ns) to prevent the need of a following correcting, *i.e.* overshoot cancelation, of the output signal. The resulting

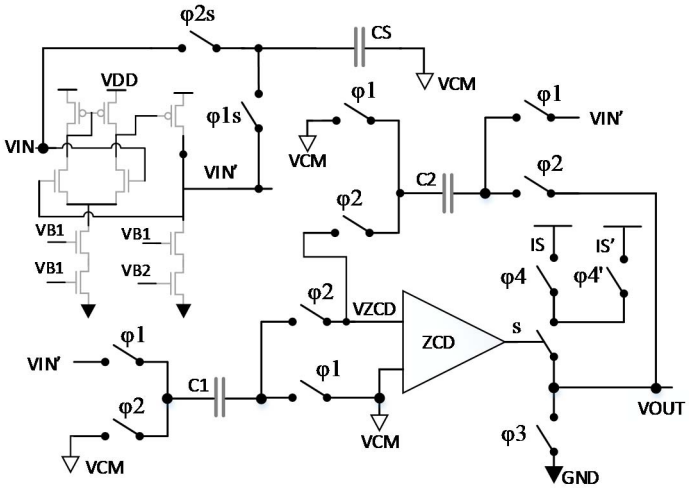

Fig. 3. Architecture of the implemented comparator-based switched capacitor residue amplifier (ResAMP in Fig. 3), *C1 = 7*C2*

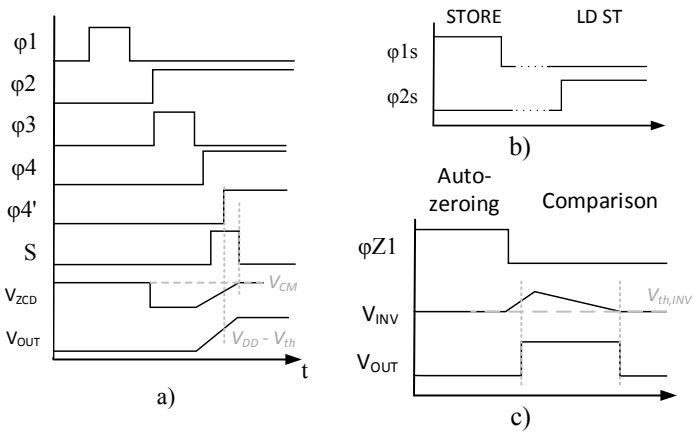

Fig. 4. Control scheme of a) comparator-based switched capacitor residue amplifier, b) Store stage, c) Zero-Crossing Detection

voltage V_{OUT} of the output VOUT follows from:

$$V_{OUT} = V_{CM} + \frac{C1+C2}{C2}(V_{in} - V_{CM}) \quad (1)$$

The control scheme for the STORE and LD ST stages are depicted in Fig. 4b.

B. Zero-Crossing Detection

The circuit for zero-crossing detection is based on the proposal in [4] and depicted in Fig. 5. The advantage of this circuit is low area costs, low power dissipation, and good response times. The control scheme, shown in Fig. 4b, is as follows. During the auto-zeroing phase, *i.e.* φZ1 is '1', inverter INV1 is shortened and the voltage difference between V_{CM} and the switching voltage of the inverter $V_{sw,inv}$ is sampled on the capacitor C1. During the comparison phase, *i.e.* φZ1 is '0', input VIN is connected to C1. This reduces the output voltage V_{INV} of the inverter and, eventually, triggers the inverter chain leading to activation of the current source IS of the ResAMP (see Fig. 3). When the ZCD's input voltage V_{IN} crosses V_{CM}, the input voltage of the inverter is equal to $V_{sw,inv}$ and the chain is triggered again, switching off the current source in ResAMP.

As there is a preferred slope, *i.e.* a change from '1' to '0' of VOUT which indicates the crossing of V_{CM}, the inverter chain can de designed in an appropriate manner. Thus, high V_{th} (HVT) transistors are added and dimensioned with low W/L ratio in order to shift the switching point of the inverters in the

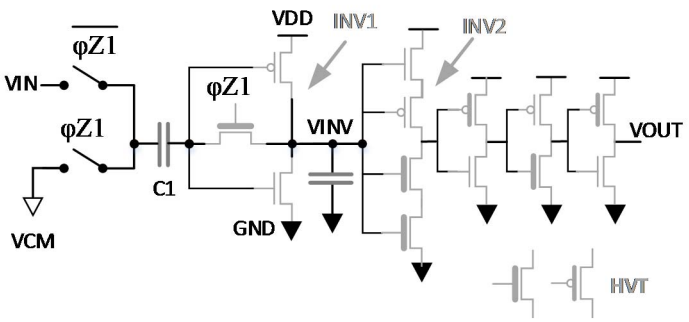

Fig. 5. Archicture of the implemented inverter-based Zero-Crossing detection (ZCD) circuit

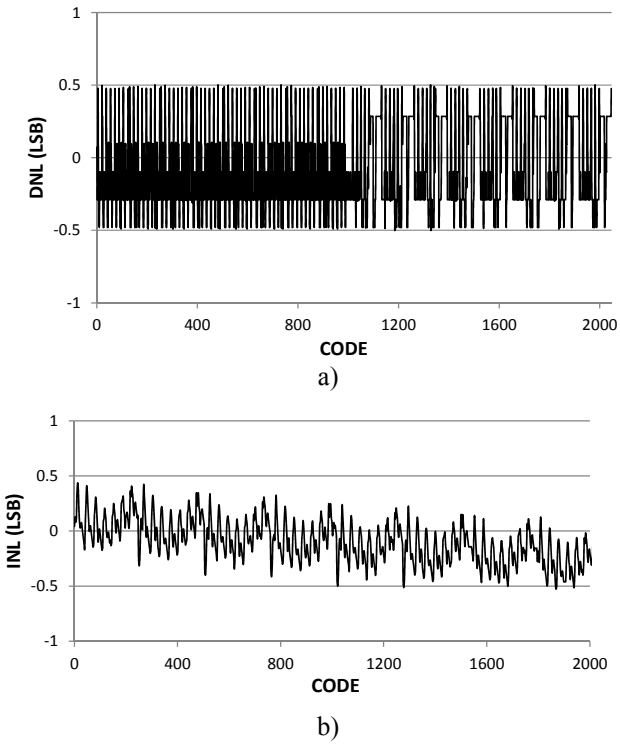

Fig. 6. Estimated DNL (a) and INL (b) curves for typical process conditions (TT) and ambient temperature (27 °C).

chain. Further, inverter INV2 (see Fig. 5) is realized with two transistors in both networks in order to achieve a more defined switching point.

IV. Simulation Results

The proposed pipelined successive approximation register was implemented in a comercial 65 nm technology with a supply voltage of V_{DD} = 1.2 V. The reference voltage was set to V_{REF} = 1 V, resulting in a common mode voltage of V_{CM} = 0.5 V. Simulations were executed with Synopsys HSpice. The maximum clock frequency was estimated with 31 MHz, resulting in a sampling rate of 4.4 MSPS. The power dissipation was estimated with 440 µW leading to an energy consumption of 48.8 fJ per conversion step. The results of DNL and INL estimation are depicted in Fig. 6.

V. Conclusion

This works presents the implementation of an 11 Bit pipelined successive approximation register ADC in a 65 nm technology that applies comparator-based switch-capacitor circuits with zero-detection in order to enable fast and linear residue amplification. Simulation results indicate conversion rates of 4.4 MSPS and energy consumption of 48.8 fJ /step.

Acknowledgements

We gratefully thank CAPES, CNPq, FAPEMIG and PRPq/UFMG for the financial support.

TABLE I. Perfomance Summary of proposed PSAR

f_{sample}	4.4 MSPS
DNL	+0.45 / -0.48 LSB_{11}
INL	+0.43 / -0.53 LSB_{11}
Power	440 µW
E/step [$P/(f_{sample}*2^{11})$]	48.8 fJ/step

References

[1] F. Maloberti, *Data Converters*: Springer Publishing Company, Incorporated, 2010.

[2] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE Journal of Solid-State Circuits,* vol. 41, pp. 2658-2668, Dec. 2006.

[3] S. K. Shin, Y. S. You, S. H. Lee, K. H. Moon, J. W. Kim, L. Brooks, and H. S. Lee, "A fully-differential zero-crossing-based 1.2V 10b 26MS/s pipelined ADC in 65nm CMOS," *2008 IEEE Symposium on Vlsi Circuits,* pp. 171-172, 2008.

[4] C. Chao, T. Zhichao, and M. A. P. Pertijs, "A 1V 14b self-timed zero-crossing-based incremental Sigma-Delta ADC," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 274-275.

[5] Y. S. Xu, L. Belostotski, and J. W. Haslett, "A 65-nm CMOS 10-GS/s 4-bit Background-Calibrated Noninterleaved Flash ADC for Radio Astronomy," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 22, pp. 2316-2325, Nov. 2014.

[6] A. Varzaghani, A. Kasapi, D. N. Loizos, S. H. Paik, S. Verma, S. Zogopoulos, and S. Sidiropoulos, "A 10.3-GS/s, 6-Bit Flash ADC for 10G Ethernet Applications," *IEEE Journal of Solid-State Circuits,* vol. 48, pp. 3038-3048, Dec. 2013.

[7] A. M. A. Ali, H. Dinc, P. Bhoraskar, C. Dillon, S. Puckett, B. Gray, C. Speir, J. Lanford, J. Brunsilius, P. R. Derounian, B. Jeffries, U. Mehta, M. McShea, and R. Stop, "A 14 Bit 1 GS/s RF Sampling Pipelined ADC With Background Calibration," *IEEE Journal of Solid-State Circuits,* vol. 49, pp. 2857-2867, Dec. 2014.

[8] G. G. Oh, C. K. Lee, and S. T. Ryu, "A 10-Bit 40-MS/s Pipelined ADC With a Wide Range Operating Temperature for WAVE Applications," *IEEE Transactions on Circuits and Systems II-Express Briefs,* vol. 61, pp. 6-10, Jan. 2014.

[9] M. Z. Wang and C. I. H. Chen, "Architecture and design synthesis of 2.5 Gsamples/s 4-b pipelined flash ADC in SoC applications," *Iecon 2005: Thirty-First Annual Conference of the IEEE Industrial Electronics Society,* vol. 1-3, pp. 2224-2230, 2005.

[10] F. Sill and D. W. d. L. Monteiro, "Pipelined successive approximation conversion (PSAC) with error correction for a CMOS ophthalmic sensor," presented at the Proceedings of the 22nd Annual Symposium on Integrated Circuits and System Design: Chip on the Dunes, Natal, Brazil, 2009.

[11] F. van der Goes, C. M. Ward, S. Astgimath, H. Yan, J. Riley, Z. Zeng, J. Mulder, S. J. Wang, and K. Bult, "A 1.5 mW 68 dB SNDR 80 Ms/s 2x Interleaved Pipelined SAR ADC in 28 nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 49, pp. 2835-2845, Dec. 2014.

[12] C. C. Lee and M. P. Flynn, "A SAR-Assisted Two-Stage Pipeline ADC," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 859-869, Apr. 2011.

[13] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2-Times Interleaved Fully Dynamic Pipelined SAR ADC in 40 nm Digital CMOS," *IEEE Journal of Solid-State Circuits,* vol. 47, pp. 2880-2887, Dec. 2012.

[14] E. Iroaga and B. Murmann, "A 12-bit 75-MS/s pipelined ADC using incomplete settling," *IEEE Journal of Solid-State Circuits,* vol. 42, pp. 748-756, Apr. 2007.