Pipelined SAR with Comparator-Based Switch-Capacitor Residue Amplification

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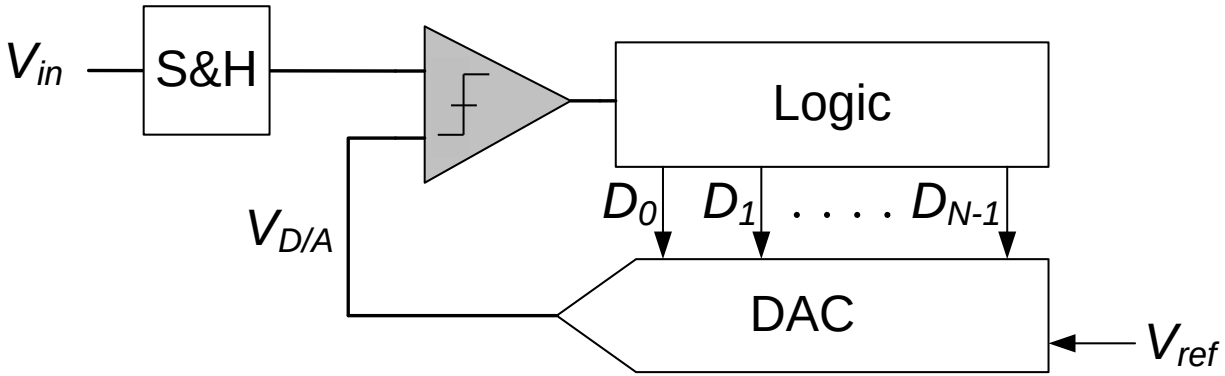
Outline

- Preliminaries
- Pipelined Successive Approximation Register (PSAR)
  - General Architecture
  - Switch-Capacitor Residue Amplification
  - Zero-Crossing Detection
- Results
- Conclusion

Preliminaries

Successive Approximation Register

- Generation of internal analog signal $V_{D/A}$ with Digital Analog Converter (DAC)
- Comparison of $V_{D/A}$ with input signal V_{in}
- Modification of $V_{D/A}$ by bits $D_0D_1..D_{N-1}$ until closest possible value to V_{in}



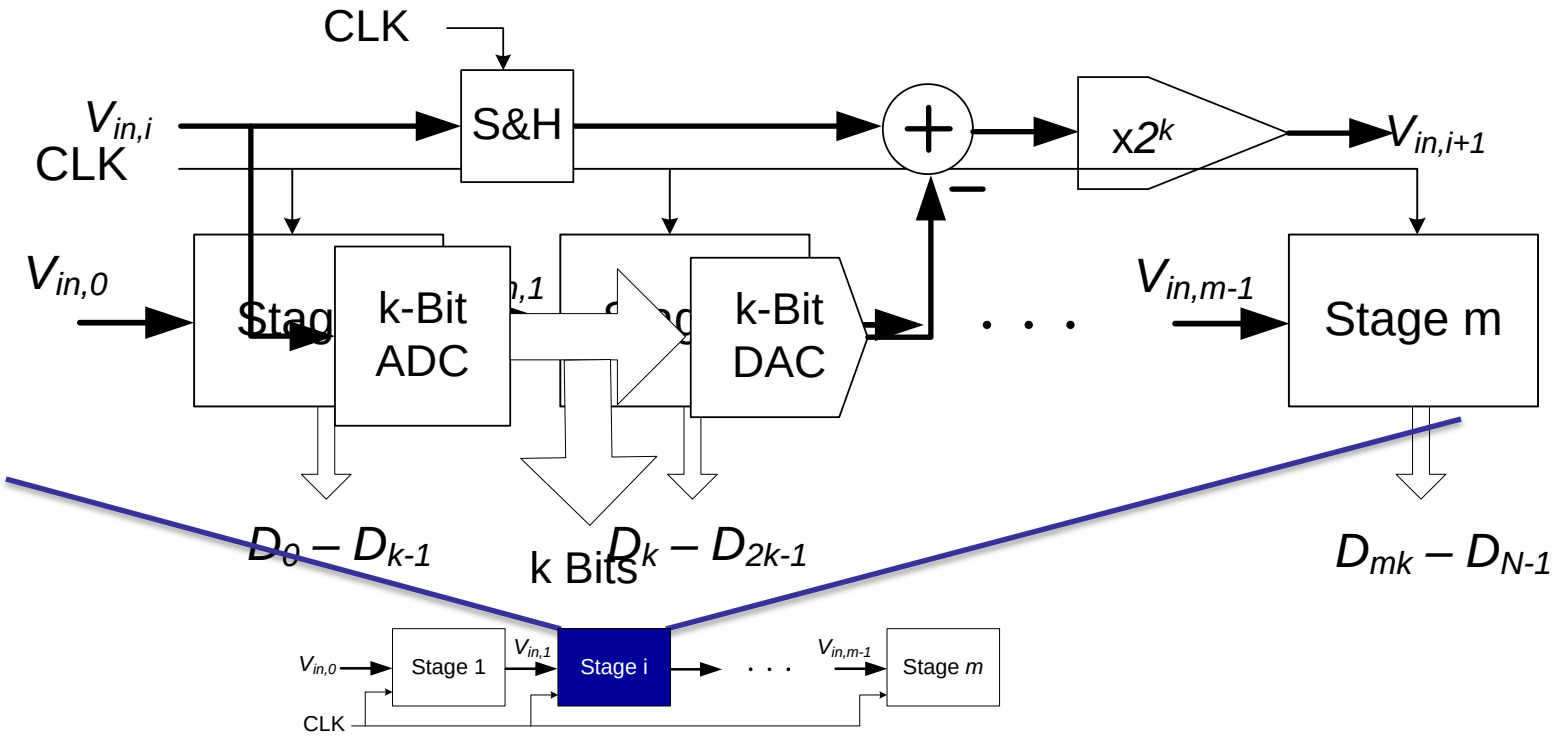
V_{ref} – reference voltage

S&H – Sample and Hold circuit

Preliminaries

Pipelined Converter

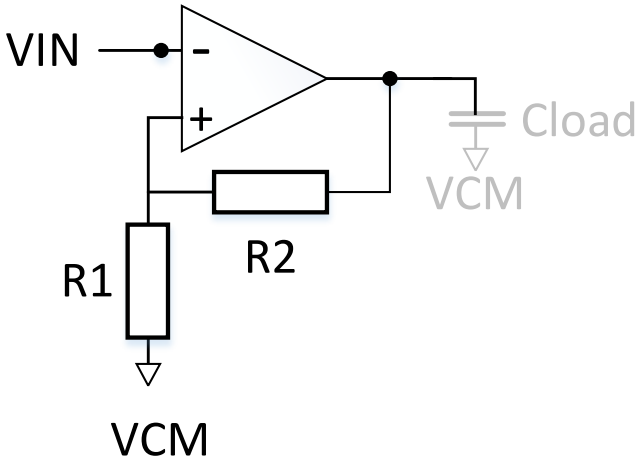
- Conversion separated in clocked stages
- In each stage: subtraction of conversion result from stage input
- Pipelined conversion of subsequent input signals

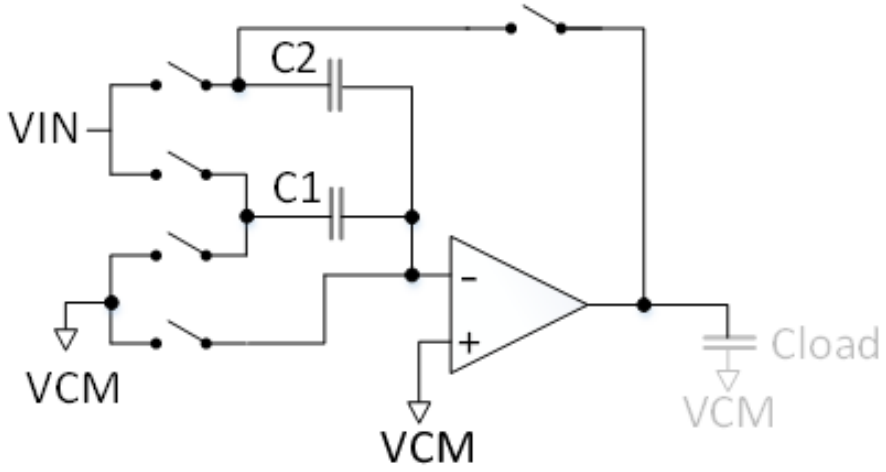


Preliminaries

Pipelined Converter - Residue Amplification

- Usually: OpAmp based
- Common concepts:
  - Resistor network amplifier
  - Switched capacitor amplifier





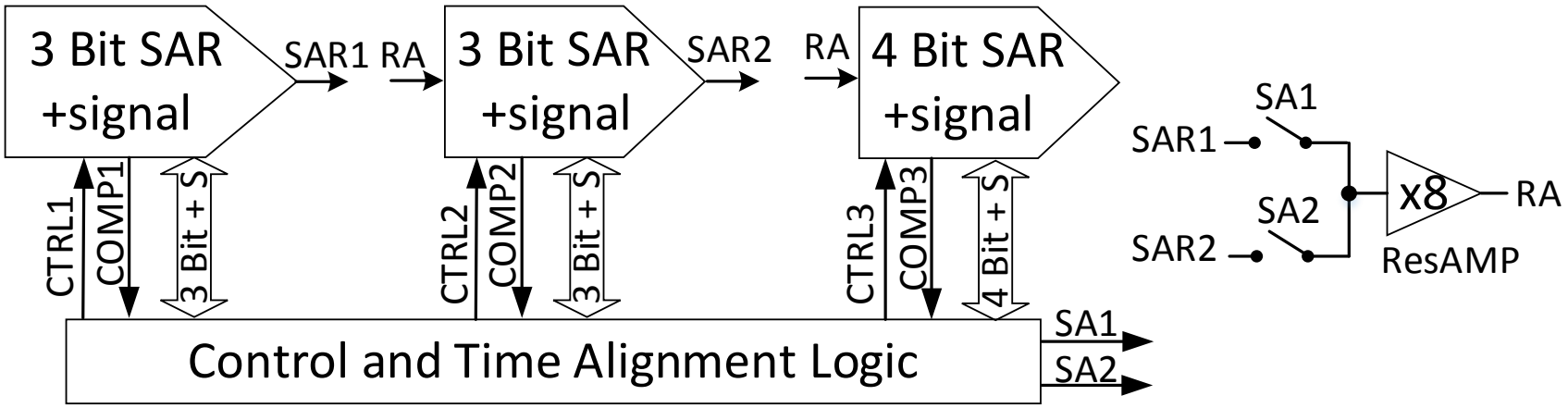
Pipelined Successive Approximation Register

Origin of Approach

- ADC is based on combination of:
  - Successive Approximation Register (SAR)
    - Low power / low area
    - Slow
  - Pipelined Converter
    - Fast
    - High power / high area
- Residue amplification
  - OpAmp => several problems in nanometer technologies (e.g., size, speed, robustness against variations)
  - Proposed solution based on
    - Comparator-based switched capacitor amplifier
    - Inverter-based zero-crossing detection

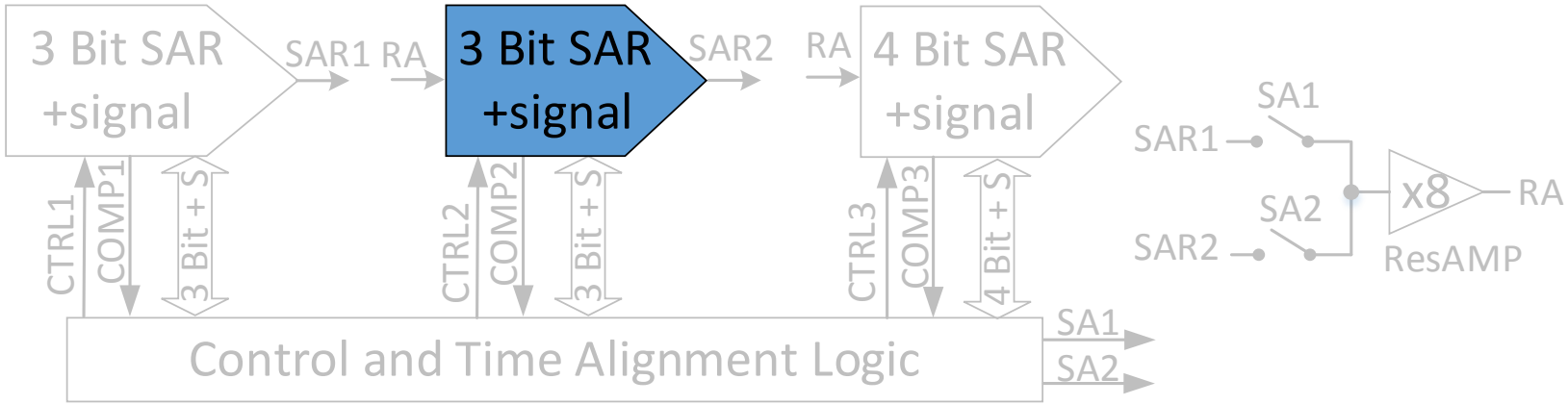
Pipelined Successive Approximation Register

Architecture



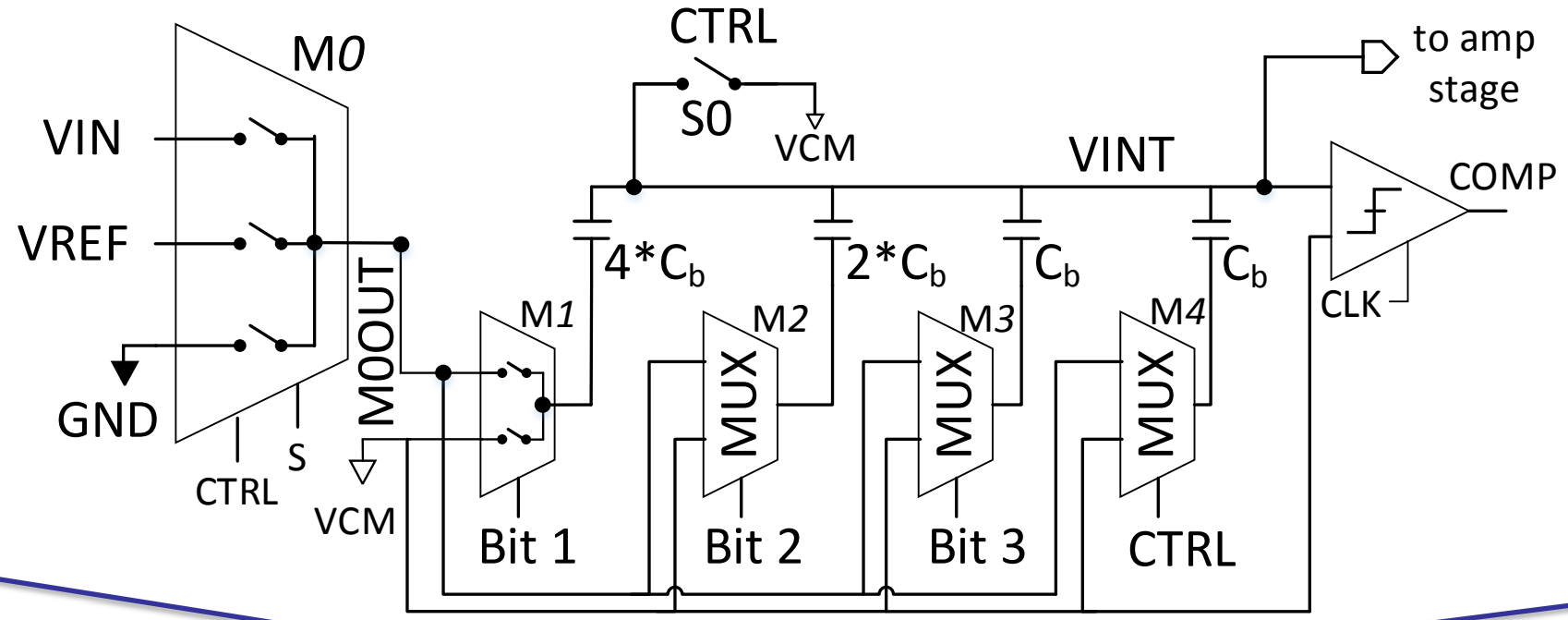
Pipelined Successive Approximation Register

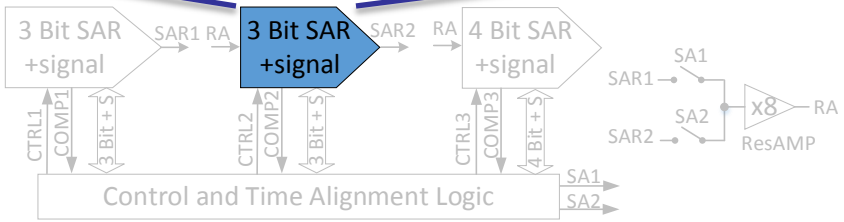
Successive Approximation Converter



Pipelined Successive Approximation Register

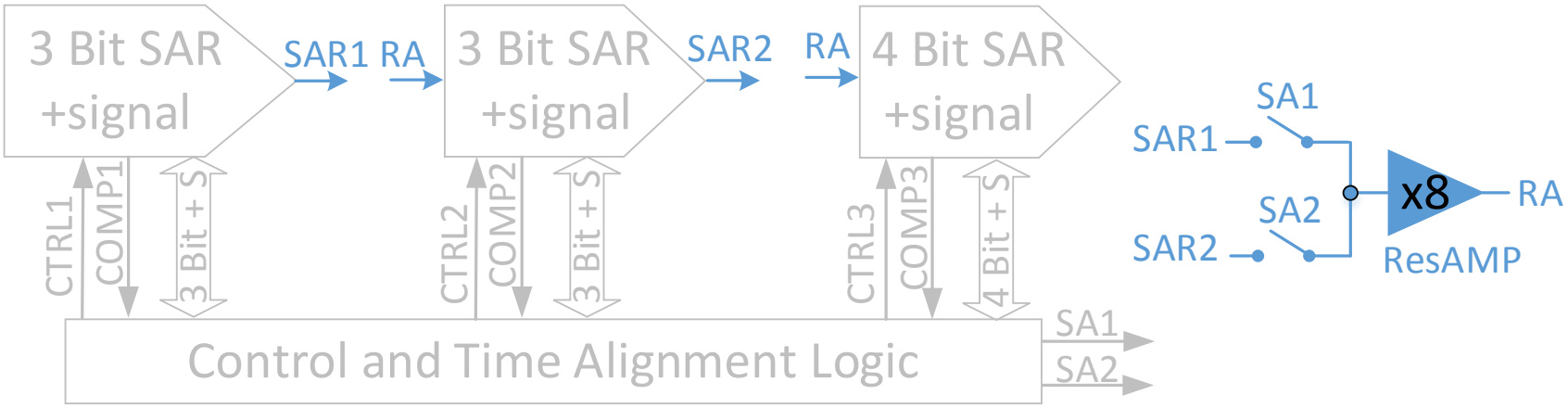
Successive Approximation Converter





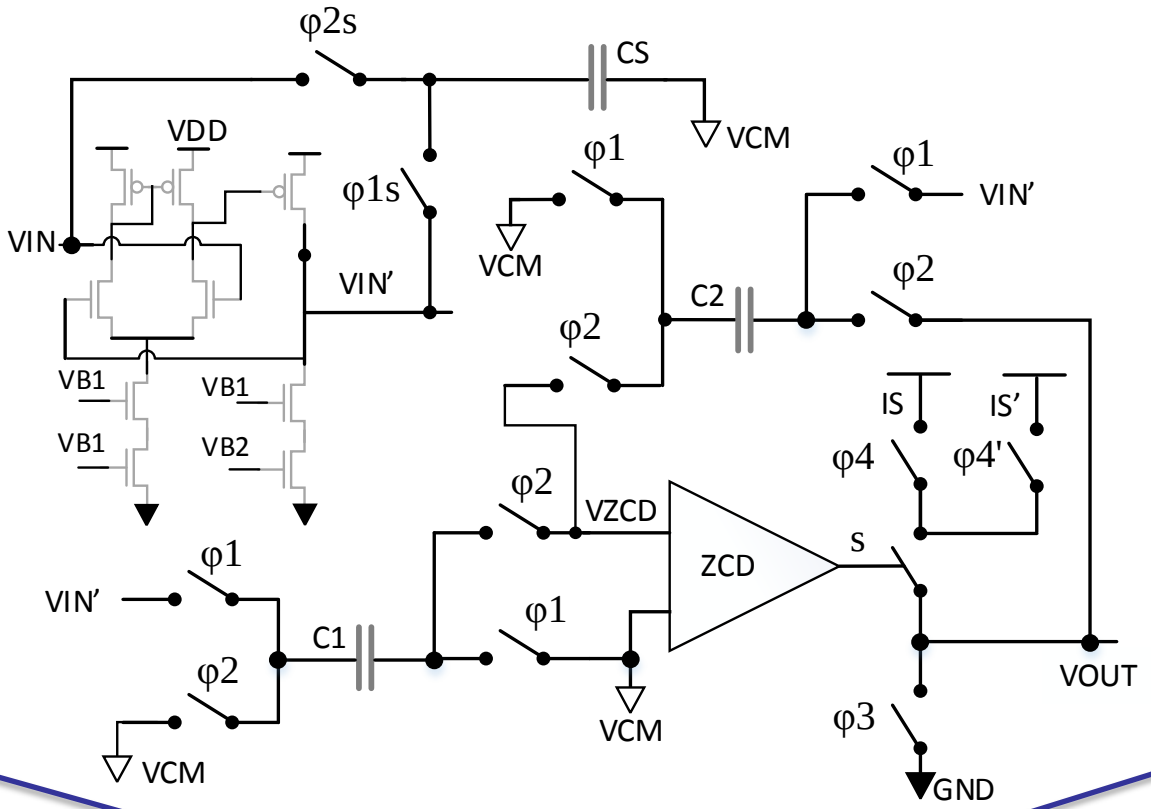
Pipelined Successive Approximation Register

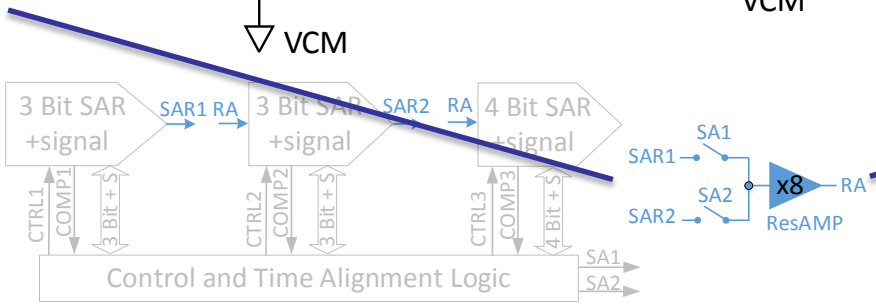
Switch-Capacitor Residue Amplification



Pipelined Successive Approximation Register

Switch-Capacitor Residue Amplification - Architecture

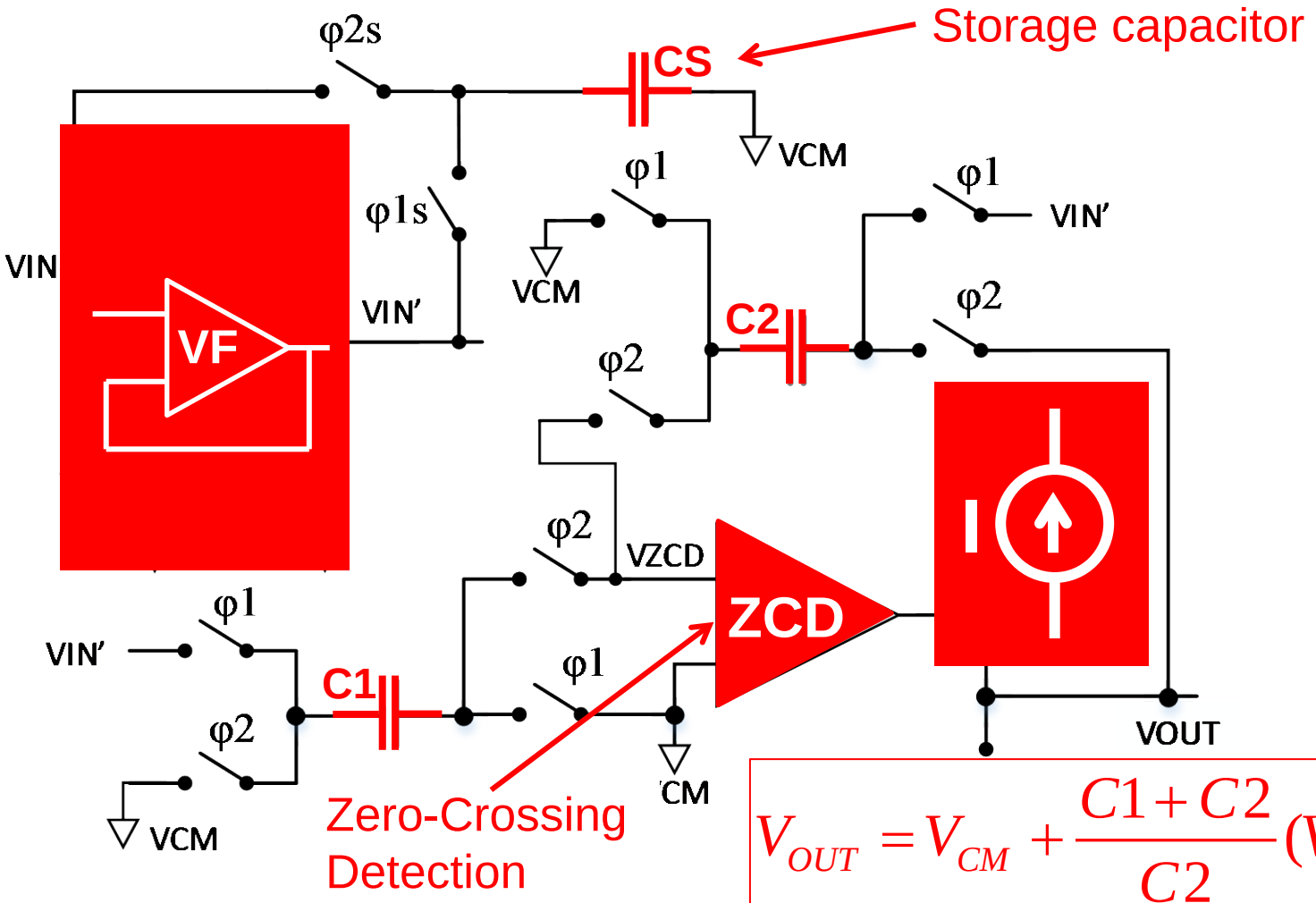




Inspired by
Fiorenza, 2006, IEEE JSSC

Pipelined Successive Approximation Register

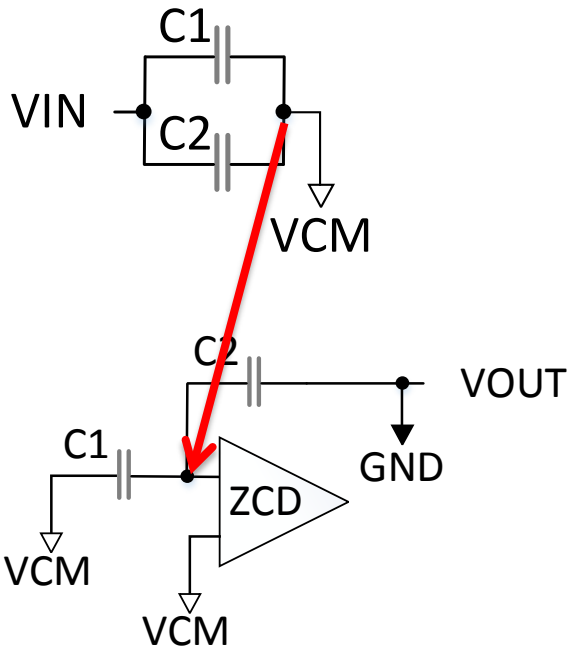
Switch-Capacitor Residue Amplification - Architecture



$$V_{OUT} = V_{CM} + \frac{C1 + C2}{C2}(V_{in} - V_{CM})$$

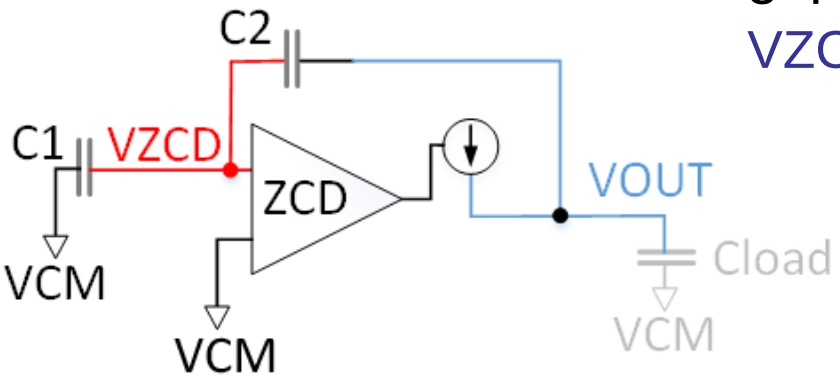
Pipelined Successive Approximation Register

Switch-Capacitor Residue Amplification - Mode of Operation



1st: VIN is sampled on C1 and C2

2nd: Charge transfer phase + VOUT set to GND level



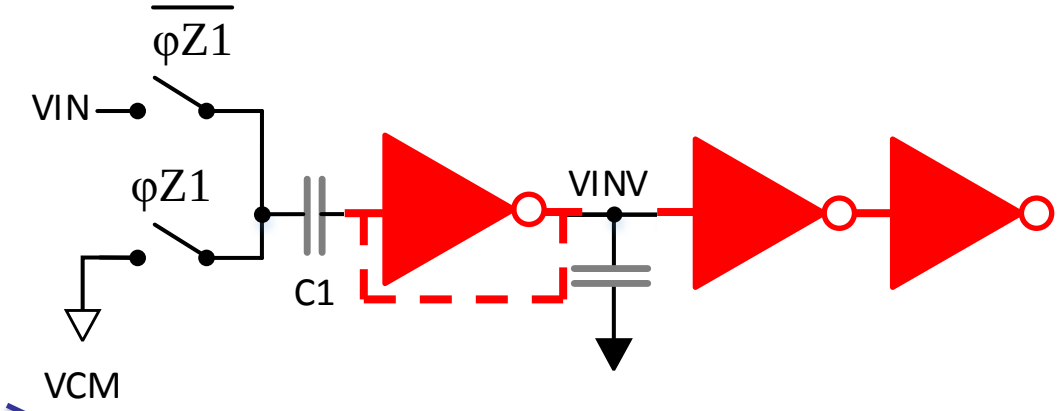
3rd: Current source activated until VZCD crosses VCM

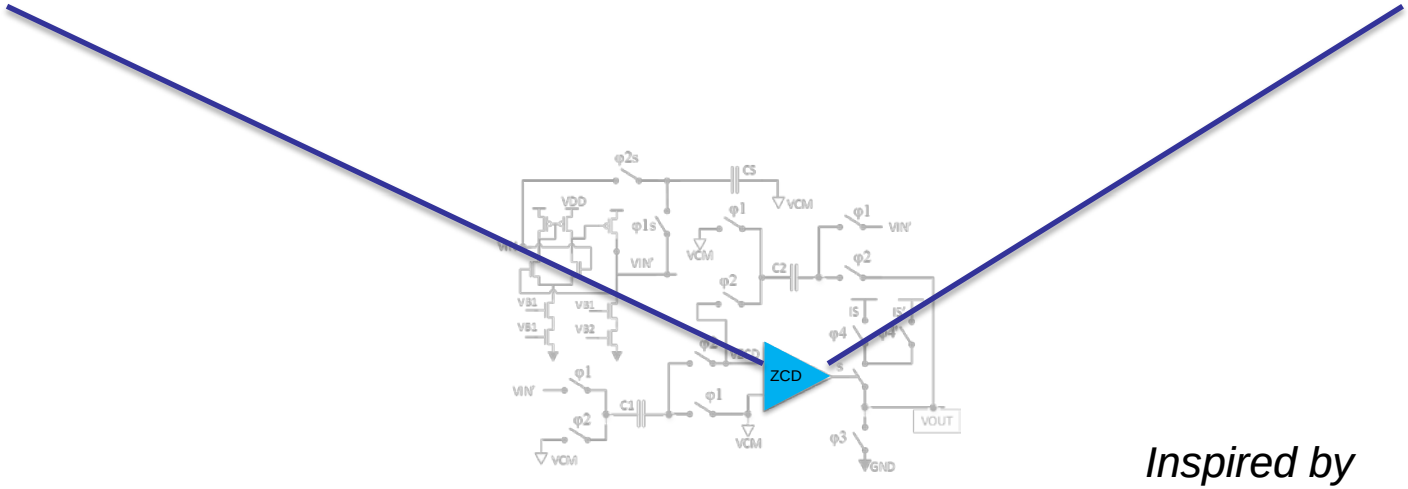
$$V_{OUT} = V_{CM} + \frac{C1+C2}{C2}(V_{in} - V_{CM})$$

$$with \quad C1 = 7 * C2$$

Pipelined Successive Approximation Register

Zero-Crossing Detection - Architecture

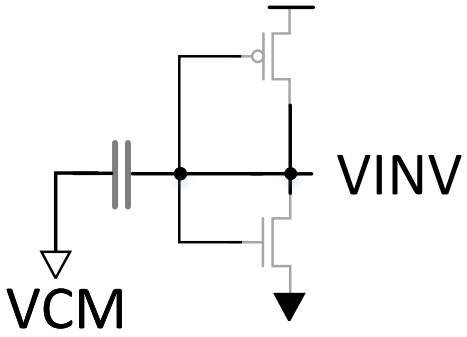




Inspired by
Chao, 2013, ISSCC

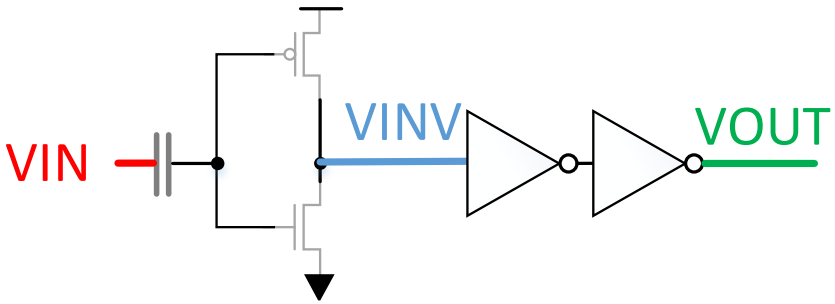
Pipelined Successive Approximation Register

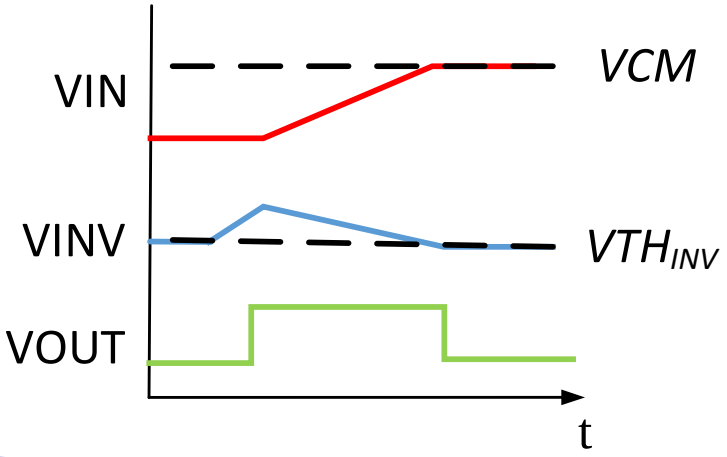
Zero-Crossing Detection – Mode of Operation



1st: Inverter shortened and VINV set to switch voltage of Inverter (VTH_{INV})

2nd: VIN (ramp) connected to inverter, inverter chain amplifies signal

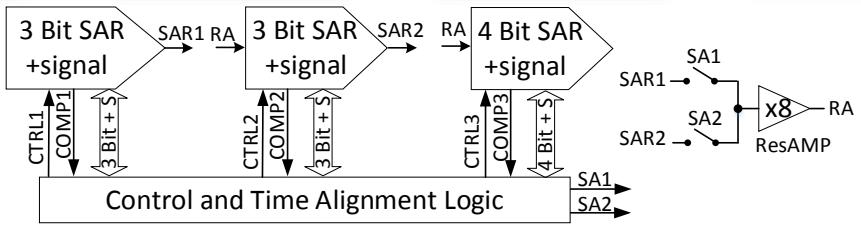




Pipelined Successive Approximation Register

Control Flow

CLK	1st SAR3	2nd SAR3	SAR4	ResAMP
1.	LOAD	TRANS	SET B3	STORE
2.	ZERO	LOAD	SET B4	AMPL
3.	CHECK S	ZERO	LAST BIT	LD ST
4.	SET B2	CHECK S	LOAD	AMPL
5.	SET B3	SET B1	ZERO	
6.	LAST BIT	SET B3	CHECK S	
7.	TRANS	LAST BIT	SET B2	LOAD

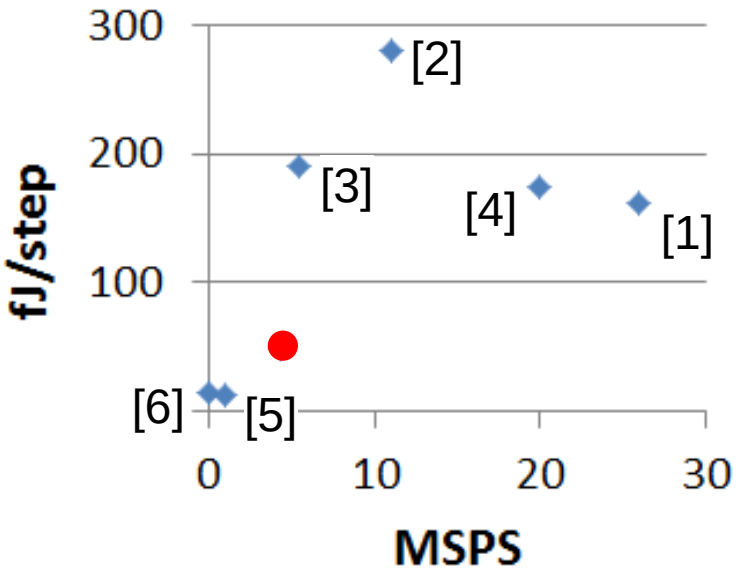


Results

Overview

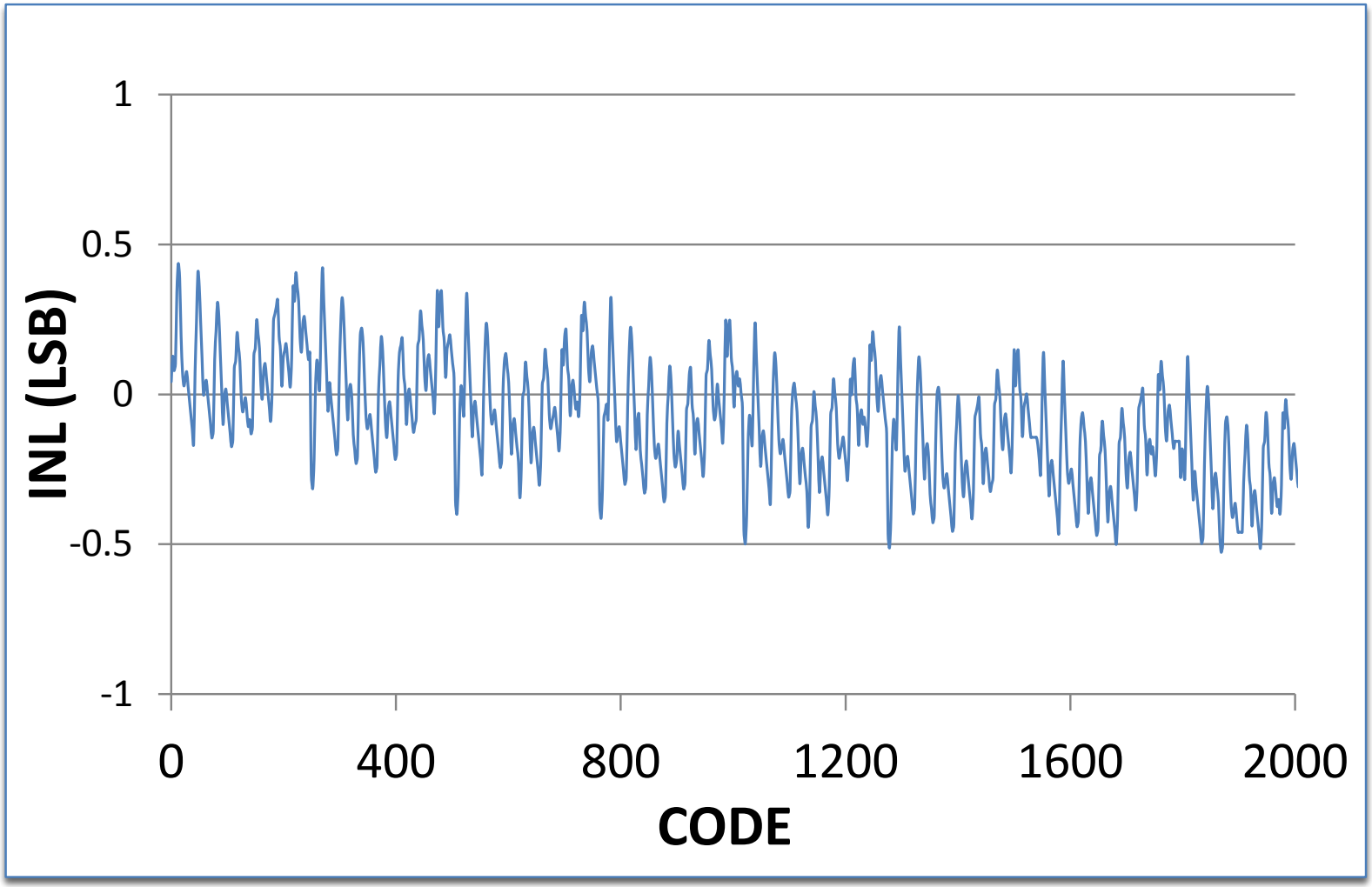
- Realized (on schematic level) in comercial 65nm technology
- VDD = 1.2 V, Vref = 1 V, VCM = 0.5 V

f_{sample}	4.4 MSPS
DNL	+0.45 / -0.48 LSB_{11}
INL	+0.43 / -0.53 LSB_{11}
Power	440 µW
E/step $[P/(f_{sample}*2^{11})]$	48.8 fJ/step



Results

Integral Non-Linearity (INL)



Conclusion

- Combination of two ADC concepts
- Comparator-Based Switch-Capacitor Residue Amplification
- Inverter-based zero-crossing detection
- 11 bit ADC implemented in 65 nm technology with low power and moderate speed

Thank you!

franksill@ufmg.br

OptMA[lab] / ART
www.asic-reliability.com

References

[1] A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS

[2] A 12b 11MS/s successive approximation ADC with two comparators in 0.13µm CMOS

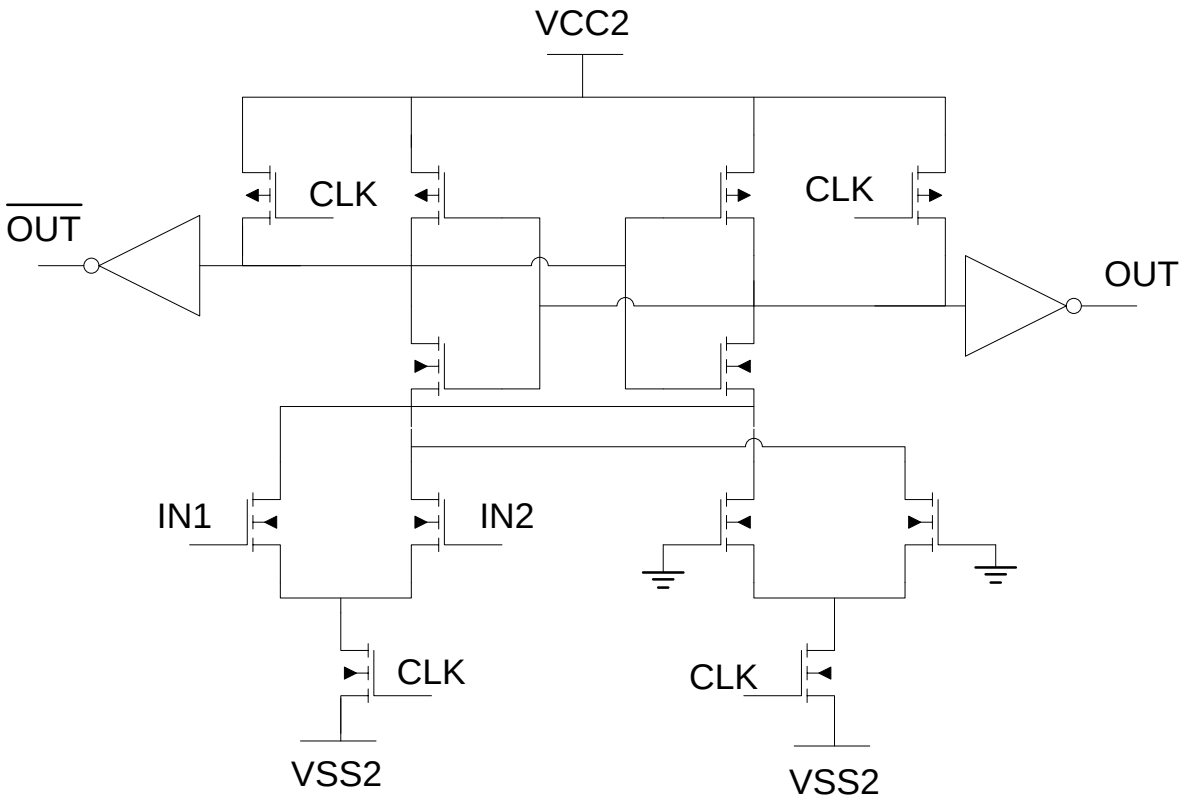
[3] Pipeline of Successive Approximation Converters with Optimum Power Merit Factor

[4] A 2.9-mW 11-b 20-MS/s Pipelined ADC with Dual-Mode-Based Digital Background Calibration

[5] An energy-efficient 1MSps 7µW 11.9fJ/conversion step 7pJ/sample 10-bit SAR ADC in 90nm

[6] ADC Ultra-Low Power for Micro-Sensors

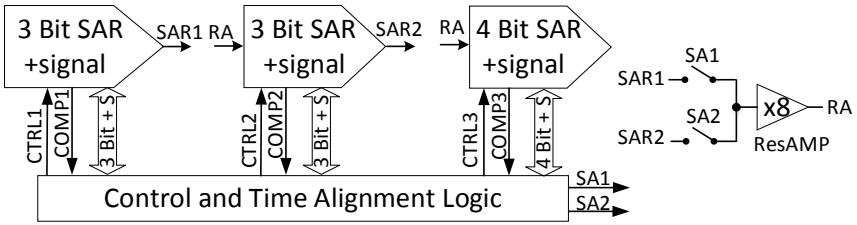
Dynamic Comparator



Pipelined Successive Approximation Converter

Schematic – Flow

CLK	1st SAR3	2nd SAR3	SAR4	ResAMP
1.	LOAD	TRANS	SET B3	STORE
2.	ZERO	LOAD	SET B4	AMPL
3.	CHECK S	ZERO	LAST BIT	LD ST
4.	SET B2	CHECK S	LOAD	AMPL
5.	SET B3	SET B1	ZERO	
6.	LAST BIT	SET B3	CHECK S	
7.	TRANS	LAST BIT	SET B2	LOAD



- **Load** - New analog input into the SAC
- **ZERO** - Resetting of SAC's output bits
- **SET Bx** - Successive bit setting and result estimation
- **LAST-BIT** - Estimation of result for last Bit (Bit n)
- **WAIT** - Generation of input analog signal for the next stage (only 1st and 2nd SAC)