Pipelined Successive Approximation Conversion (PSAC) with Error Correction for a CMOS Ophthalmic Sensor

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ABSTRACT

The purpose of this work is the proposal of a 10-Bit / 1 MSPS Analog to Digital Converter (ADC) with error correction to match the requirements of a CMOS wavefront sensor for ophthalmic applications. The developed ADC is a combination of different techniques for integrated converters. It unifies the advantages of successive approximation converters and pipelined converters. The result of this combination is a very good tradeoff between performance and power dissipation. In a second step, the problem of parameter variations is examined. Therefore, the developed ADC is enhanced by two error correction techniques to improve its reliability. Transistor level simulations indicate that in an environment with varying design parameters the maximum (Differential Non-Linearity) DNL error could be reduced from more than 130 V_{LSB} to 0.7 V_{LSB}. The ADC selection assessment and error correction presented herein can be adopted for other sensors within other signal domains as well.

Categories and Subject Descriptors

B.4.0 [**Input/Output and Data Communications**]: General; B.4.5 [**Input/Output and Data Communications**]: Reliability, Testing, and Fault-Tolerance

General Terms

Design, Reliability

Keywords

ADC, Error Correction, Pipelined SAC

1. INTRODUCTION

Analog-to-Digital Converters (ADCs) are fundamental elements in mixed-signal circuits. The wide field of applications and requirements resulted in various converter types where the most well know kinds are the integrating ADC, the successive approximation ADC (SAC), the flash ADC, the pipelined ADC (PADC), and the sigma-delta ADC (1). Each of these converters has its preferred tasks. However, for some applications it can be useful to combine different ADC concepts to obtain the best trade-off between power dissipation and conversion speed. In this paper such a combined approach is presented.

The target application is a CMOS wavefront sensor to measure complex ocular refractive errors [1]. The sensor to be served consists of 400 active pixels clustered as separate position-sensitive detectors laid in an orthogonal array to detect optical aberrations based on the Hartmann-Shack method [2]. These aberrations are dynamic due to the eye involuntary micro-saccadic movements (~ 90 Hz), which imposes a threshold readout frequency to the system. Safety regulations in ophthalmology demand very low probe-light levels, consequently yielding low signal levels, which cannot be integrated long enough due to the aforementioned constraint, and therefore requires a system with the best possible noise performance in other to increase the signal-to-noise ratio and the measurement accuracy. Also, it is desirable to have a compact and portable system for clinical usage, which requests low-power dissipation. The ultimate goal is to design an ADC in an AMS 0.35 µm technology, integrated with the wavefront sensor elements, that complies with these requirements by meeting a conversion rate of 1 MSPS, for 10-bit resolution, and power dissipation below 10 mW.

A critical problem in analog designs is the variance of technology parameters and variations at runtime which can lead to critical conversion errors. All manufactured samples of an integrated circuit differ in a certain range from each other. Further, variations of temperature and supply voltage have high influence on circuit behavior. Hence, it is necessary to create robust circuits which can handle these variations. This work gives an overview and a comparison of the most reported error correction techniques for ADCs. Further, this paper proposes two error correction techniques for the developed ADC. Finally, the results of transistor-level simulation will be presented.

2. PRELIMINARIES

This section gives a short overview about ADC characteristics and two widely deployed ADC concepts, which, if merged, meet the demands previously described to satisfy the requirements of the proposed CMOS optical sensor. Further, an overview and comparison of the most common error correction techniques for integrated ADCs will be presented.

2.1 Successive Approximation Converter

Successive approximation is a popular approach for ADCs which require moderate conversion times at low area and power demands [3]. The main principle of SAC bases on binary by successive halving of the intermediate results. In a SAC the number of steps determines the resolution of the ADC.

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2.2 Pipelined ADC (PADC)

Beside flash ADCs, Pipelined Analog-to-Digital Converters are common choices for high-speed applications [3]. The frequency can be considerably increased, by means of sub-unit conversion modules, which raises the throughput by the same amount. The drawback is an increased latency since the conversion result is only available after all sub-units finish their processing. However, this is no problem at applications with a continuous input data stream, as is the case for the target CMOS wavefront sensor.

2.3 ADC Error Correction

2.3.1 Redundant Comparators

The idea of redundant comparators follows the consideration that the comparator is the main failure source in Successive Approximation Converters [4]. Hence, the approach proposed by Giannini et al. in [5] applies two parallel fully dynamic regenerative comparators. Both differ in its transistor sizing which leads to a different noise dependency and power dissipation. Further, both comparators share the input connections but they never work at the same time. The strategy behind the correction technique relies on the fact that if the input comparator is properly sized, at most 2 out of N comparisons (with N as ADC resolution) during the SAC operation are likely to be critical because of thermal noise, i.e., the one when the signal is right below the threshold and the one when it is right above. One of those critical decisions will certainly be the last one. However, an error in this decision can be avoided by using the comparator in its low-noise/high-power state. The other decision can be applied for any of the previous (N-1) comparisons.

2.3.2 Foreground Calibration

Foreground calibration is an error correction technique for ADCs where the routine work of ADC is interrupted to apply a calibration signal [6]. As the known calibration signal is converted by the ADC, a set of input and output data is obtained that can be used to find the coefficients of the non ideal model of the ADC or the ADC pipeline stage, respectively. Subsequently, at runtime the code errors are subtracted in the digital domain. Convergence of coefficients is usually very fast and takes few hundred iterations [7]. If this interruption is not desirable queue-based foreground calibration can be used [8]. Thereby, a queue of sample and hold amplifiers stores the input data during the calibration. However, this requires an ADC conversion rate which is larger than the sampling rate of the input signal.

The drawbacks of foreground calibration techniques are the necessity to stop the ADC operation or to increase the conversion rate. In addition, the area demand increases by the need of circuitry for the generation of the calibration voltages. Furthermore, queue-based techniques require more additional blocks which increase area and power, too. Finally, the development of an adequate error model is necessary [9].

2.3.3 Background Calibration

Background calibration techniques determine coefficients of a non ideal model of an ADC similar to foreground calibration approaches. However, in contrast to the latter, background calibration works at runtime of the ADC. This can be done by using a slow-but-accurate ADC converter in parallel with the main converter [10]. Another way is to add a calibration signal to the input signal and process both simultaneously [11]. Thereby, usually the injected calibration signal is modulated with a pseudorandom sequence that is uncorrelated with the input signal. The pseudorandom sequence can be generated by a chopping sample-and-hold amplifier which multiplies the analog input signal by a pseudorandom binary signal. Subsequently, the calibration signal is recovered by correlating the ADC output with the same pseudorandom sequence.

The problems of background calibration are the relatively high effort for the demodulation, or additional hardware which also needs a calibration. Furthermore, similar to foreground calibration techniques an error model has to be designed.

2.3.4 Sub-Ranging

In multistage pipelined ADCs inaccuracies are removed by increasing the number of bits of each stage by one following the first stage and using that bit to determine if the stage conversion was accurate [3][12]. The main idea behind is to use the additional bit for the characterization of the residue of the previous conversion step and to apply this information for error correction procedure [13]. The drawbacks of this approach are the accuracy requirements on the amplifying blocks and on the digital-to-analog conversion blocks. Further, the higher resolution of some stages increases the demands on area and power.

2.3.5 Comparison

Table 1 compares the previously introduced error correction techniques. Thereby, RC means redundant comparators, FC is foreground calibration, BC stands for background calibration, and SR means sub-ranging. The comparison concentrates on the gain in accuracy, the demand in area and power, which is divided in analog and digital parts, and the effort for the design of the approach.

The application of redundant comparators increases the accuracy moderately while the effort in design, area and power is acceptable. Both foreground calibration techniques were valued with a high accuracy as both concern several kinds of errors (e.g. gain, offset) of different blocks (gain stage, comparators, capacitor mismatch). However, both approaches need more attention in the digital domain and both suffer under high effort in design. The background calibration with an additional high accurate ADC has only a moderate increase of accuracy as this ADC is also susceptible to failures (e.g. gain, offset). In contrast, it was shown in the literature that background calibration with signal injection can lead to a remarkable increase of accuracy. However, the effort in design, area, and power is for both techniques a strong drawback. The sub-ranging approach leads to a moderate increase of the accuracy while the design effort for the analog part increases drastically as the resolution of several stages has to be increased.

Table 1. Comparison Of Analyzed Error Correction Techniques.

Technique	Gain in Accuracy	Area / Power		Effort in Design
		Analog	Digital	
RC	+	○	○	○
FC – interrupt	+ +	○	-	-
FC – queue based	+ +	-	- -	- -
BC – red. ADC	+	- -	-	-
BC – injection	+ +	○	- -	- -
SR	+	- -	○	○

3. PIPELINED SAC (PSAC)

3.1 Concept

The drawback of SAC is its performance limitations at higher resolutions as each increase of the resolution requires an additional clock cycle. In contrast, even though the PADC needs less area than a plain flash ADC it still has high demands on area which leads to high power consumption. Hence, the main idea of the implemented Pipelined Successive Approximation Analog-to-Digital Converter (PSAC) is the combination of both concepts' advantages. This idea is similar to the method from Li et al. [14] however both approaches differ strongly in its realization.

The PSAC has lower power consumption as a PADC with flash ADCs since the PSAC uses less comparators which are one of the integrated components with the biggest area [3]. On the other hand a SAC has a good performance at low resolutions while the concept of a PADC allows a high throughput at high resolutions.

3.2 Structure

Figure 1 depicts the scheme of the implemented PSAC which has a resolution of 10 Bit. The PSAC consist of two 3-Bit SAC and a 4-Bit SAC. They are connected by two gain amplifiers which base on the work from Steininger [15]. A digital block (Control and Time Alignment Logic) controls the PSAC. The SACs work with charge redistribution whereas the value of the applied capacitances increases by factor two. Further, each SAC contains a dynamic comparator which bases on the design from Uthaichana et al. ([16]). After the SAC finishes its calculations the input signal V_{comp_in} of the comparator is equal to the residue of the conversion. Therefore, the signal V_{comp_in} of the two 3-Bit SACs is also connected with the gain amplifier stage which amplifies the residue.

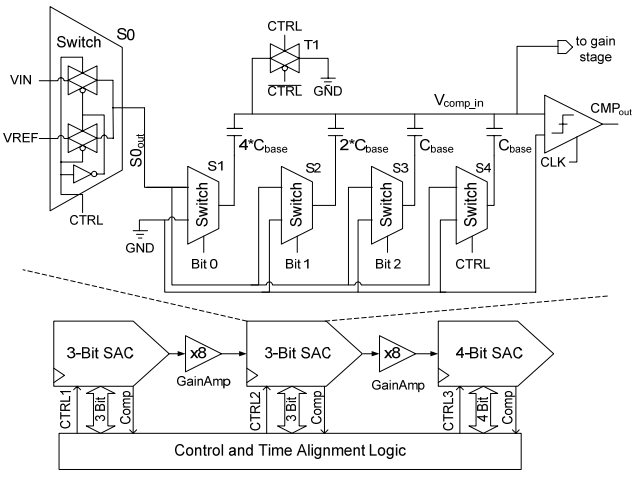

Figure 1. Scheme of the proposed Pipelined Successive Approximation ADC

3.3 Function

The SACs work in different phases controlled by the clock signal. The phases are:

- **LOAD**: Read new analog input into the SAC
  - Switch S0 connects net $S0_{out}$ with voltage V_{in}
  - Bits 0 to n are high (='1'), thus Switches S1-S4 connect capacitors with $S0_{out}$
  - Transmission gate T1 connects V_{comp_in} with GND
- **ZERO**: Resetting of SAC's output bits
  - Bits 0 to n are low (='0'), thus S1-S4 connect capacitors with GND
  - V_{comp_in} changes to $-V_{in}$
- **SET Bx**: Successive bit setting and the result estimation
  - If Bit x is set ('1') V_{comp_in} changes to $V_{comp\_in\_pr} + V_{ref}/2^x$, with $V_{comp\_in\_pr}$ is the previous value of V_{comp_in} and V_{ref} is the reference voltage
  - If $V_{comp\_in} > 0$ then signal CMP_{out} is '1'
  - If CMP_{out} is '1' then Bit (x-1) goes back to '0' (change of V_{comp_in} and comparator operation separated by one clock cycle)
- **LAST-BIT**: Estimation of result for last Bit (Bit n)
  - Processing of comparator output
- **WAIT**: Generation of input analog signal for the next stage (only 1st and 2nd SAC)
  - Value of V_{comp_in} is equal to residue
  - V_{comp_in} connected with 'gain 8' stage

The order of the phases is depicted for each SAC in figure 2a. From this graph follows that after seven clock cycles a new result is available at the output of the PSAC.

The task of the "Control and Time Alignment Logic" block connects the corresponding results of each SAC stage.

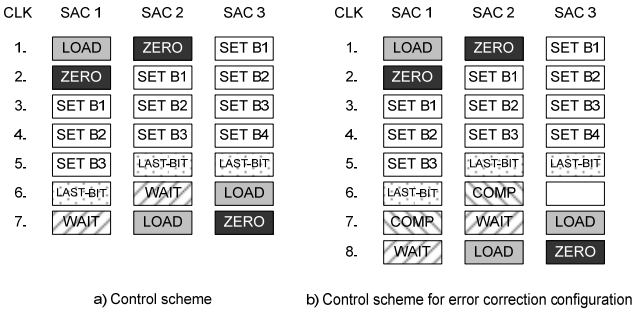

Figure 2. Phase schemes of the PSAC's control algorithm

4. ERROR CORRECTION

4.1 Failure Sources in the PSAC

Before a decision about an error correction approach can be made it is worthy to determine the components which are most susceptible to parameter variations. The required accuracy of the first SAC is 10 Bit, for the second SAC and the first gain stage it is 7 Bit, while the last SAC and the second gain stage require an accuracy of 4 Bit. Monte Carlo simulations with varying parameters (technology parameter, transistor sizes, temperature, and supply voltage) indicated that the comparators in the first and second SAC and the gain amplifiers are the most critical components. Hence, the error correction approaches should concentrate on these components.

4.2 Redundant Comparator

A false decision in the comparator of a SAC leads to a wrong digital result and a wrong residue V_{res} at the end of the conversion. Thereby, the residue error ε_{res} is a multiple of the V_{LSB} of the SAC. This follows from the SAC method of operation as after each comparison a multiple of V_{LSB} is added or removed to or from the internal voltage V_{comp_in} (see figure 1). Hence, if it can be assured that the absolute maximum error of the comparator is smaller than V_{LSB} then $\varepsilon_{res} = [-V_{LSB}, 0, V_{LSB}]$. This error will be multiplied in the following gain amplifier. Thus, after the amplification the input voltage $V_{in,i+1}$ for the next SAC results from:

$$V_{in,i+1} = 8 \cdot \left(V_{res,i} + \varepsilon_{res,i} \right) = 8 \cdot V_{res,i} + 8 \cdot \varepsilon_{res,i} \quad (1)$$

As the maximum residue is equal or smaller than V_{LSB} the input voltage $V_{in,i+1}$ is smaller than 0 (if $\varepsilon_{res} = -V_{ref}/2^N = -V_{LSB}$) or bigger than the reference voltage V_{ref} (if $\varepsilon_{res} = V_{LSB}$). Thus, the idea of the proposed error correction approach is to add after the amplification an additional comparator block which controls whether the input voltage exceeds its theoretical limits. Further, in case of an error the residue error can be fed back to the negative input of the amplifier to correct the residue. The resulting circuit is depicted in figure 3. The block for error detecting consists of two dynamic comparators and logic for the determination of the voltage for the error correction.

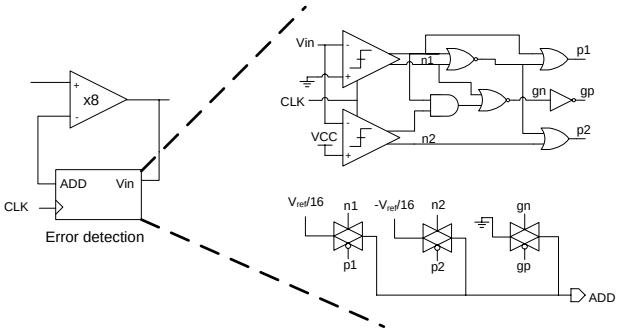

Figure 3. Modified gain amplifier with logic for error detection

Unfortunately, the additional error detection and correction demands an extra clock cycle. The modified PSAC control scheme is shown in figure 2b. The two 3-Bit SAC have the new phase "COMP" in which the error detection logic is active. The new phase follows after the "LAST-BIT" phase. Hence, a new conversion result is available after eight clock cycles.

4.3 Foreground Calibration

The desired application of the ADC, a wavefront sensor for ophthalmic application, allows stopping the conversion for short periods. Hence, it is possible to apply a foreground calibration technique for the adjustment of the gain amplifiers. Therefore, for both amplifiers a voltage ramp circuit based on the work from Zadeh et al. [17] generates an input signal which is converted by the PSAC. Thereupon the amplification error of both amplifiers is determined with a linear regression algorithm. It has to be observed that at first the gain amplifier after the 2nd SAC must be calibrated before the amplifier after the 1st SAC. Thereby, the first calibration requires $2^4 = 16$ steps and an accuracy of the voltage ramp circuit of 8 V_{LSB}. The second calibration requires $2^7 = 128$ steps and an accuracy of 1 V_{LSB}. Further, it is necessary to calibrate the amplifiers for all three possible signals of the negative input. This results in six calibrations with 144 steps each. Together with the implemented first-order algorithm a complete calibration needs around 2 ms which is a reasonable duration for the desired application.

5. SIMULATION RESULTS

The PSAC was modeled in an AMS 0.35 µm CMOS process with a supply voltage of $V_{DD} = 3.3$ V. The sampling rate was set to 1 MSPS at a clock frequency of 8 MHz. The design was analyzed at transistor level by Monte-Carlo simulations with varying parameters (process, voltage, temperature). Without error correction the results indicate a maximum Differential Non-Linearity (DNL) error of more than 130 V_{LSB} and a maximum Integral Non-Linearity (INL) of more than 600 V_{LSB} (see figure 4 and figure 5). These huge errors base mainly on wrong results in the first SAC.

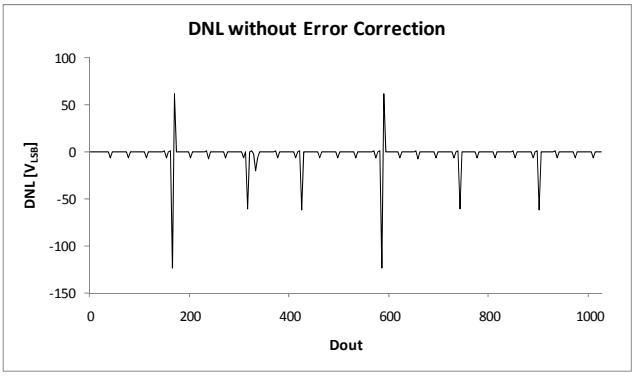

Figure 4. DNL of the PSAC without Error Correction (varying parameters)

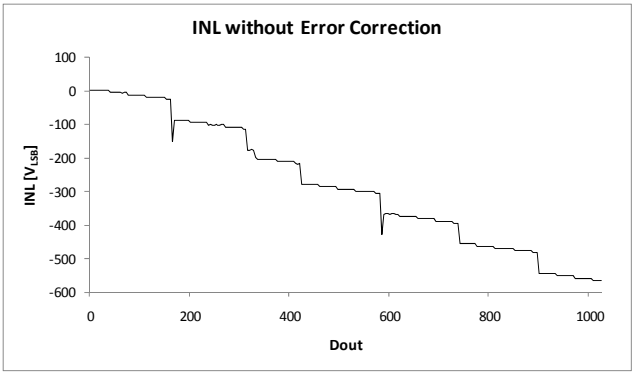

Figure 5. INL of the PSAC without Error Correction (varying parameters)

Through the insertion of the redundant comparator block and the foreground calibration the maximum DNL error could be reduced to 0.7 V_{LSB} while the maximum INL error decreased to 0.9 V_{LSB} (see figure 6 and figure 7). Thus, it could be shown that the proposed error correction for the PSAC leads to correct results.

The average power dissipation for the analog and digital blocks was determined to be 8.2 mW. Table 2 compares the power and current consumption for each main block. There, it can be seen that the gain amplifiers are dominating. Hence, future research should concentrate on these blocks whereby techniques like clock or power gating should be considered.

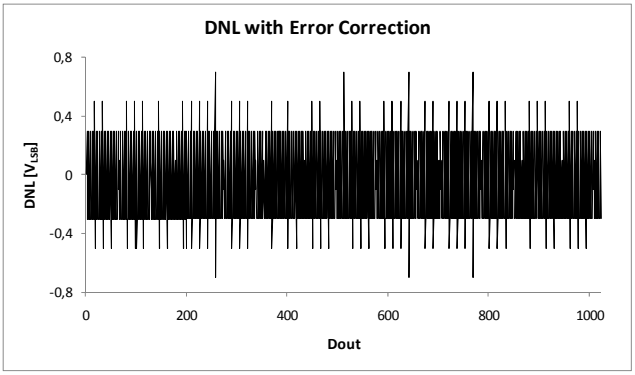

Figure 6. DNL of the PSAC with Error Correction (varying parameters)

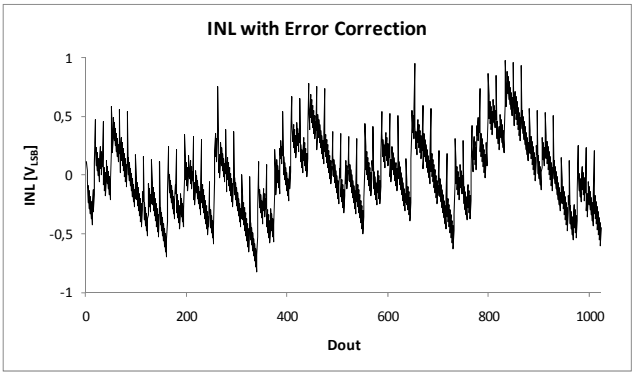

Figure 7. INL of the PSAC with Error Correction (varying parameters)

6. CONCLUSION

This work presents a Pipelined Successive Approximation Converter (PSAC) which will be used for a CMOS wavefront sensor for ophthalmic applications. The proposed converter is a combined approach of two design techniques for Analog-to-Digital Converters (ADCs). Thereby, the advantage of low-power conversions of successive approximation converters and the high speed capability of pipelined converters are coupled. Further, a short overview about error correction techniques in ADCs is given. In addition, this work proposes two error correction techniques for the presented converter. The simulation results for a realistic environment with varying parameters indicate for the design with error correction a maximum DNL error of 0.7 V_{LSB} compared to a DNL error of more than 130 V_{LSB} of the raw PSAC.

Table 2. Current and Power Dissipation (TA – Time alignment, V_{DD} = 3.3 V)

Block	Current	Power
Capacitors	3.2 pF@1 MHz = 3.2 µA	10.5 µW
Comparators	7 * 2.8 µA	64.5 µW
Gain amplifier	2 * 1.1 mA	7.26 mW
Control/TA logic	621 gates	0.9 mW

ACKNOWLEDGMENTS

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