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Design of Mixed Gates for Leakage Reduction

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Focus of this Work

1. Advancement of established Leakage Reduction techniques (DVTCMOS / DTOCMOS)

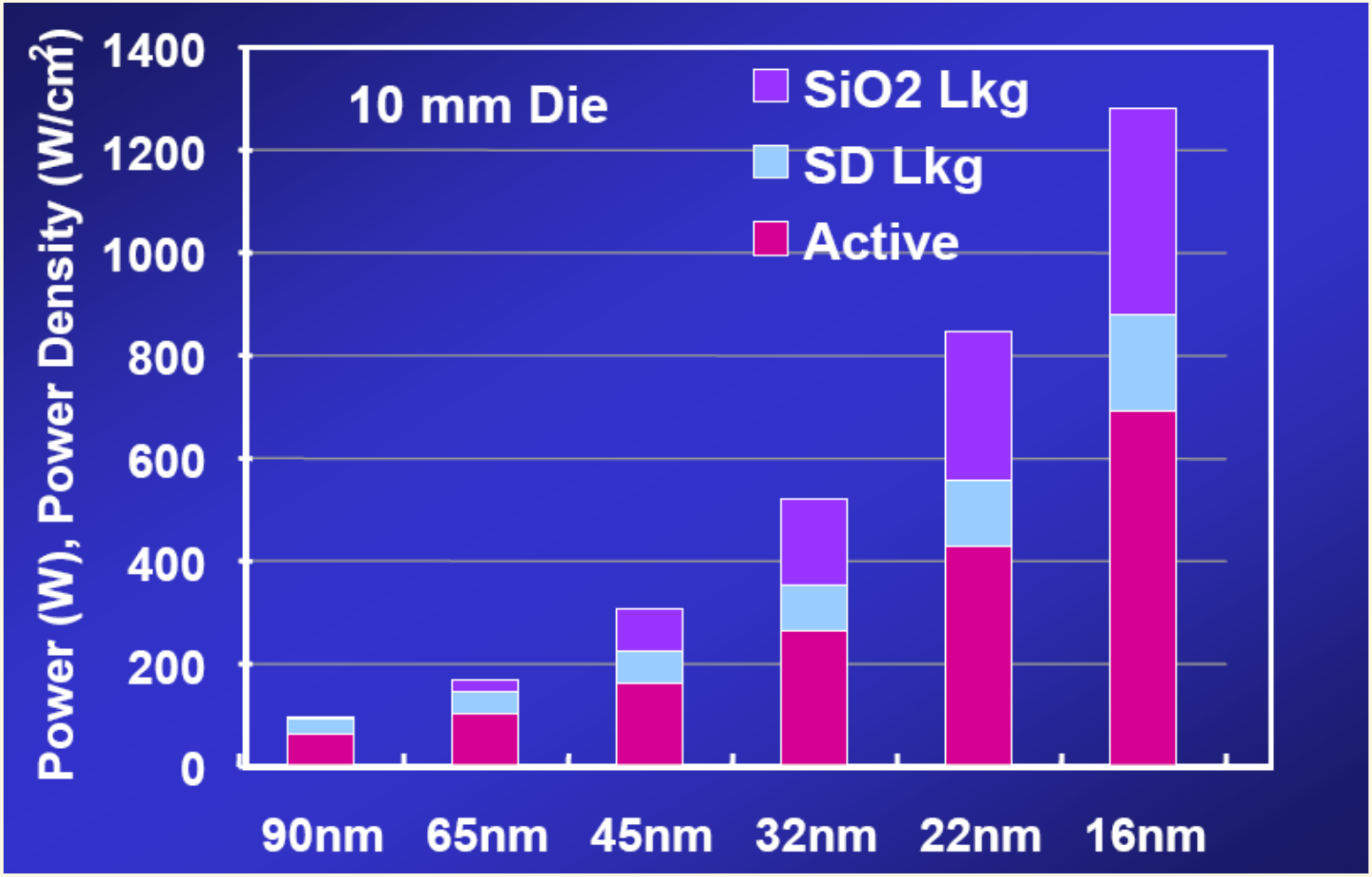
2. Investigations on rules for *Mixed Gates* design

DVTCMOS: Dual V_{th} CMOS
DTOCMOS: Dual T_{ox} CMOS

Outline

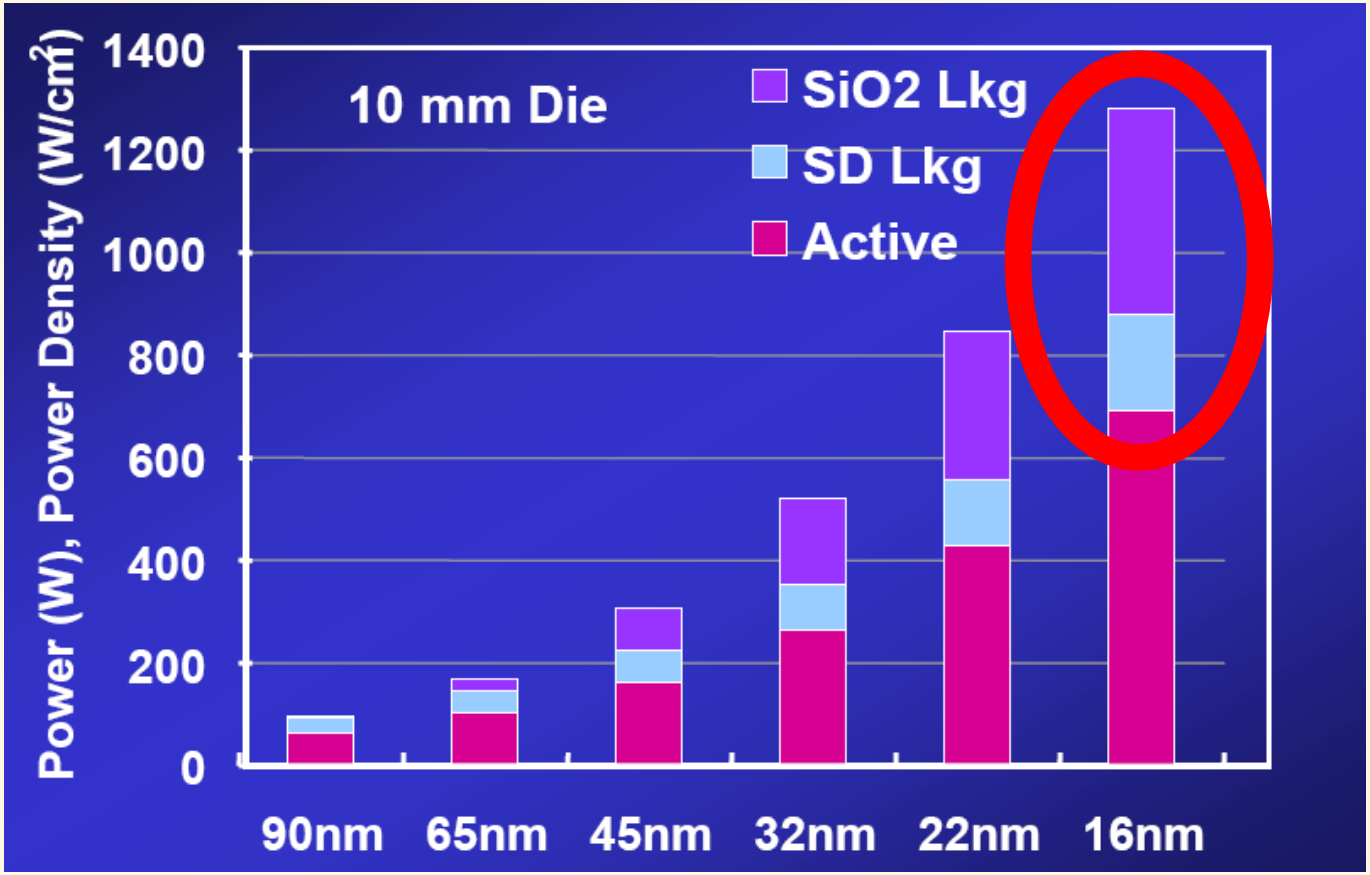
1. Motivation
2. Basics
3. Mixed Gates
4. Design Rules
5. Benchmark results
6. Conclusions

Motivation



S. Borkar, '05

Motivation



Up to 50 % will be (*is !*) leakage!

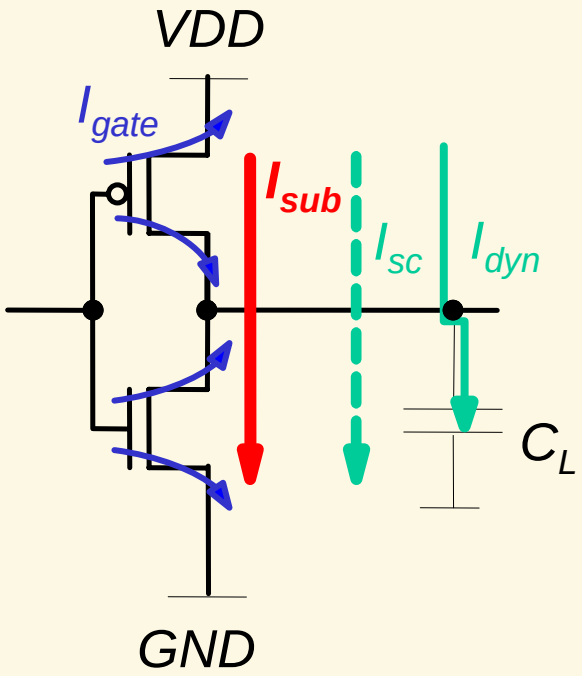
SiO2 Lkg - Gate Oxide Tunneling Leakage (I_{gate})

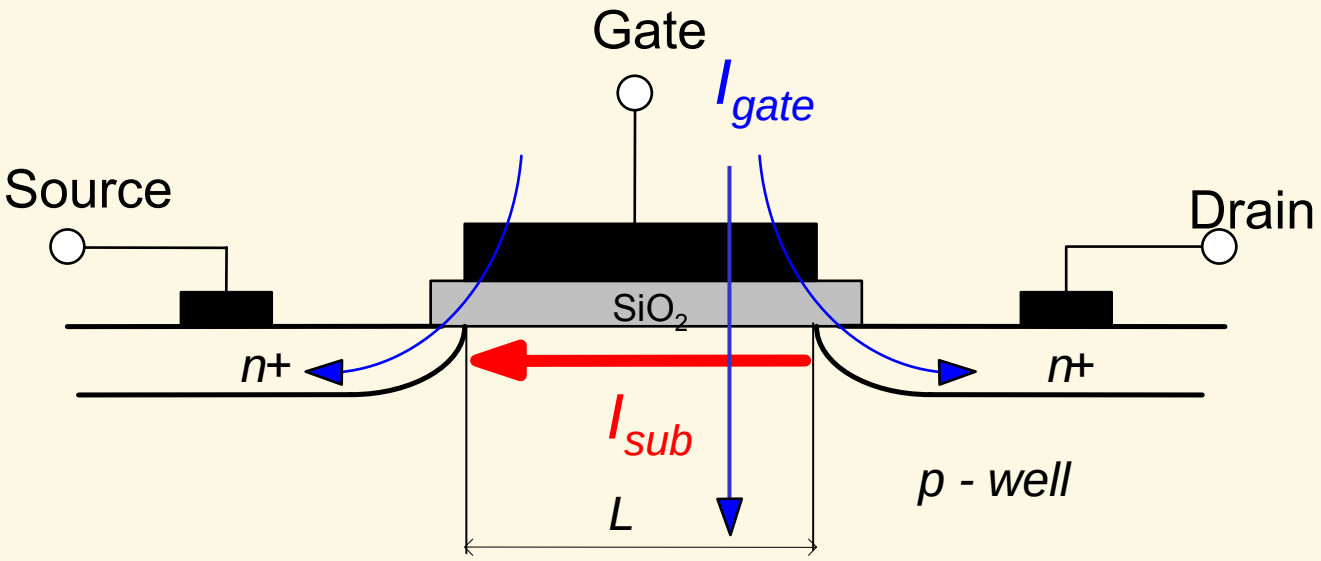
SD Lkg - Subthreshold Leakage (I_{sub})

S. Borkar, '05

2. Basics

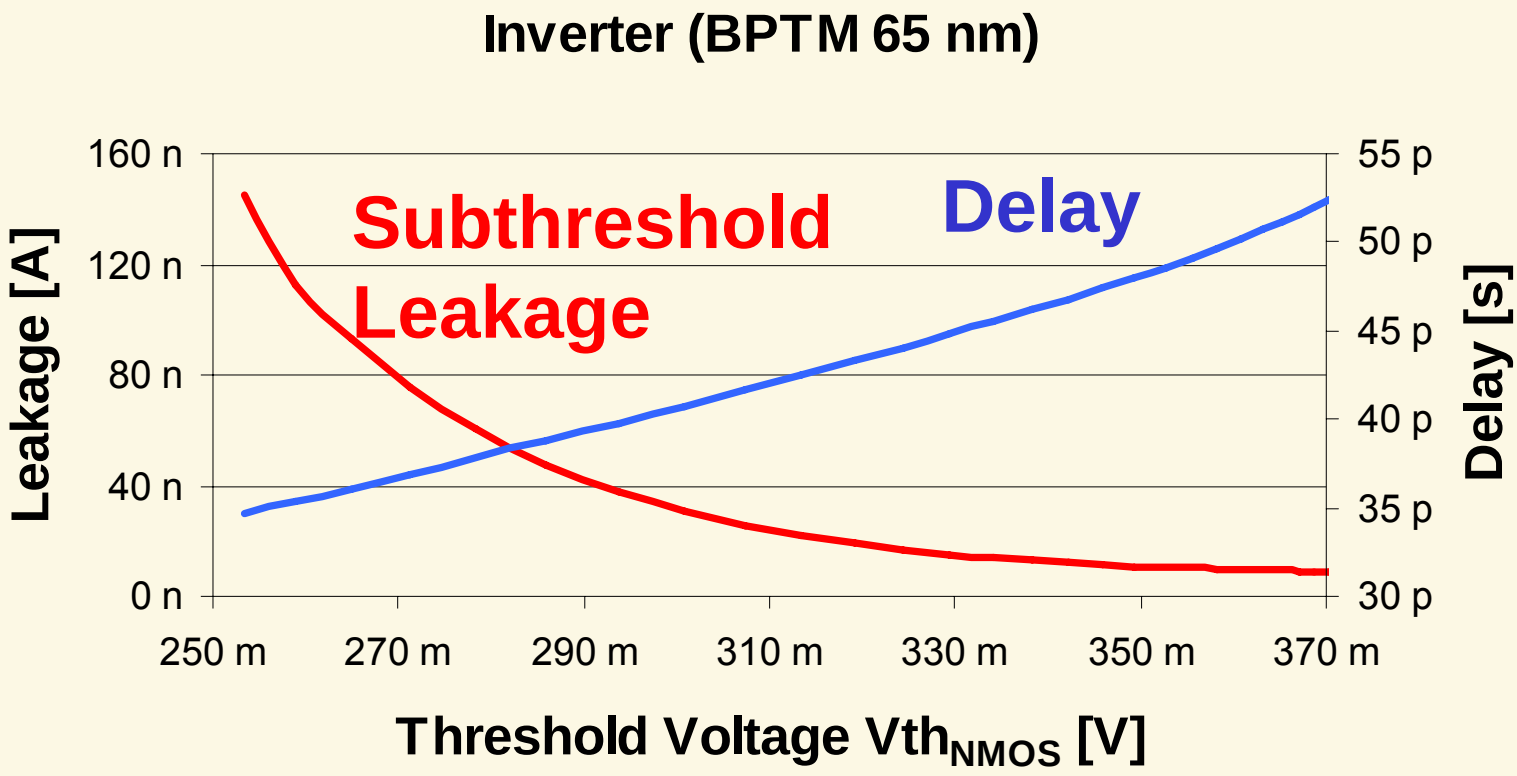
Power Dissipation in CMOS





- I_{sub} occurs if $V_{gs} < V_{th}$
- carriers move by diffusion along surface
- I_{gate} caused by direct tunneling through gate oxide

V_{th} vs. Delay and Leakage



V_{th} vs. Delay and Leakage

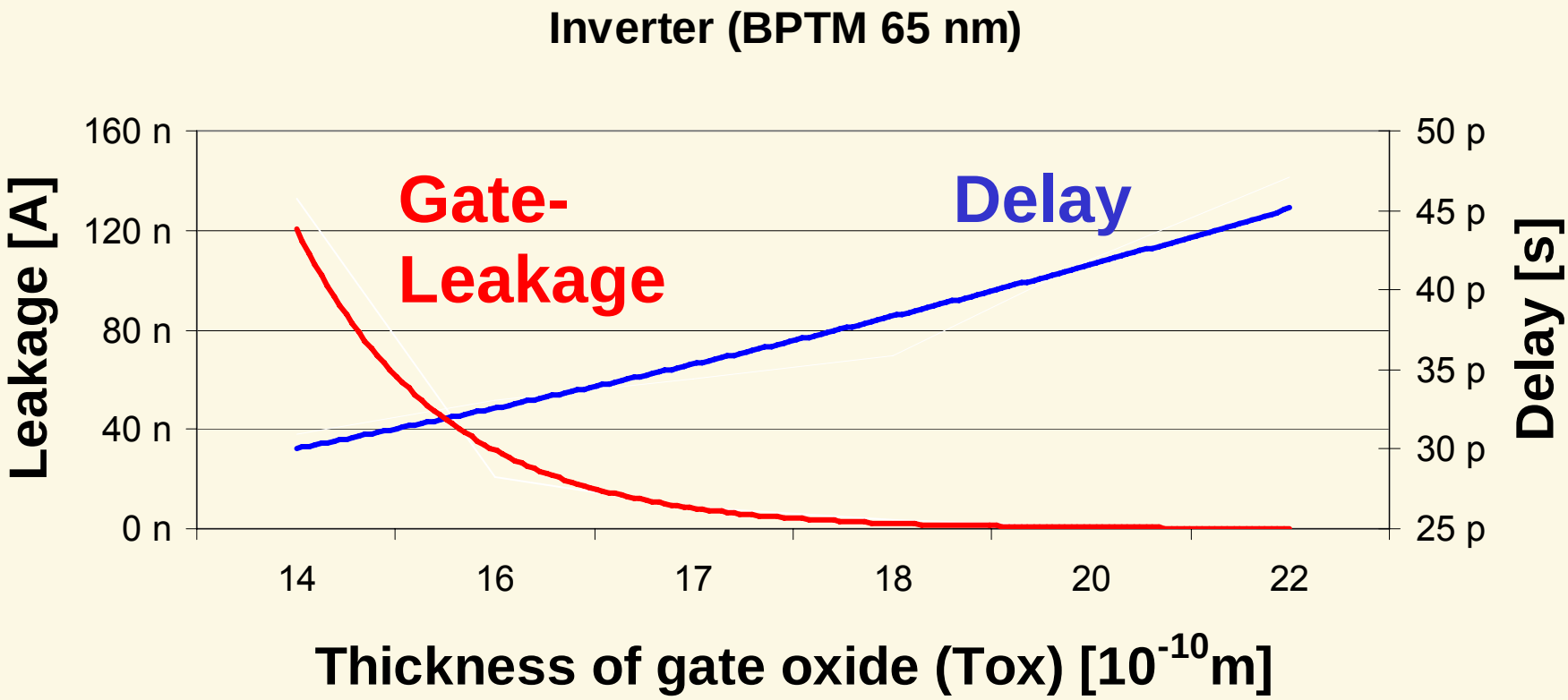
fast devices with high power dissipation (low V_{th})

or

slow devices with low power dissipation (high V_{th})

Threshold Voltage Vth_{NMOS} [V]

T_{ox} vs. Delay and Leakage



T_{ox} vs. Delay and Leakage

fast devices with high power dissipation (low T_{ox})

or

slow devices with low power dissipation (high T_{ox})

Thickness of gate oxide (Tox) [10^{-10}m]

DVTCMOS / DTOCMOS

Dual Threshold Voltages (DVTCMOS)

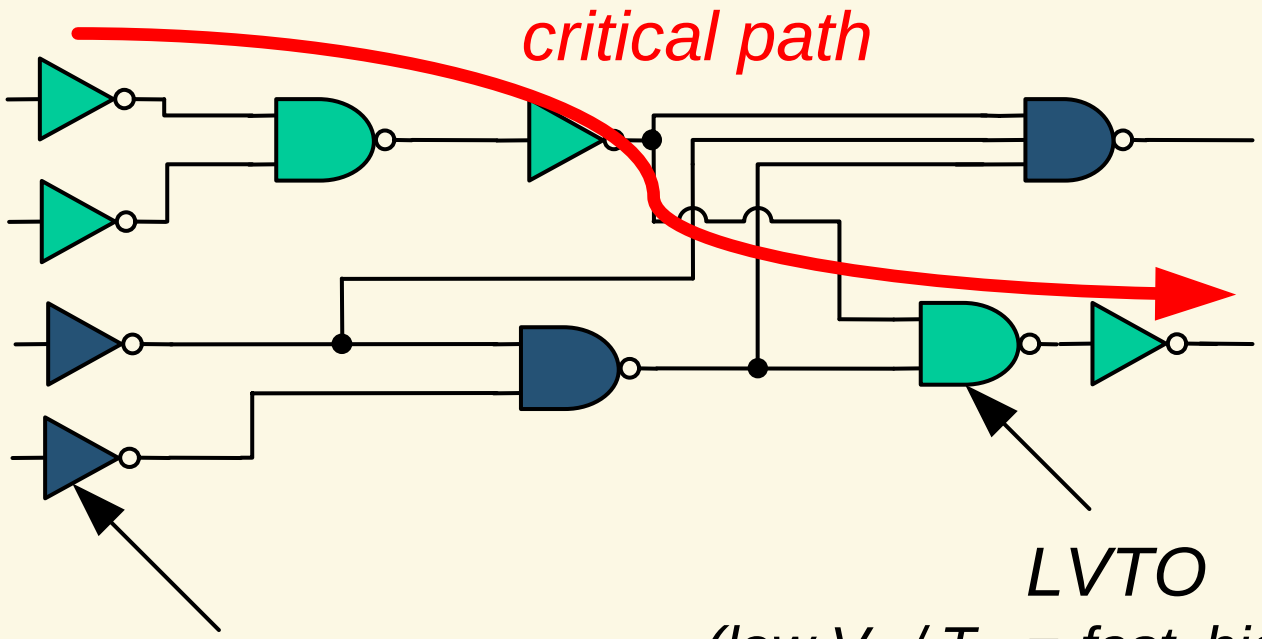
- Use different V_{th}'s
  - use lower threshold for devices within the critical paths
  - use higher threshold for devices outside the critical paths

Dual Tox (DTOCMOS)

- Use different T_{ox}'s
  - use thinner gate oxide for devices within the critical paths
  - use thicker gate oxide for devices outside the critical paths

⇒ Decrease leakage without performance penalty

DVTCMOS / DTOCMOS cont'd



LVTO

(low V_{th} / T_{ox} = fast, high leakage)

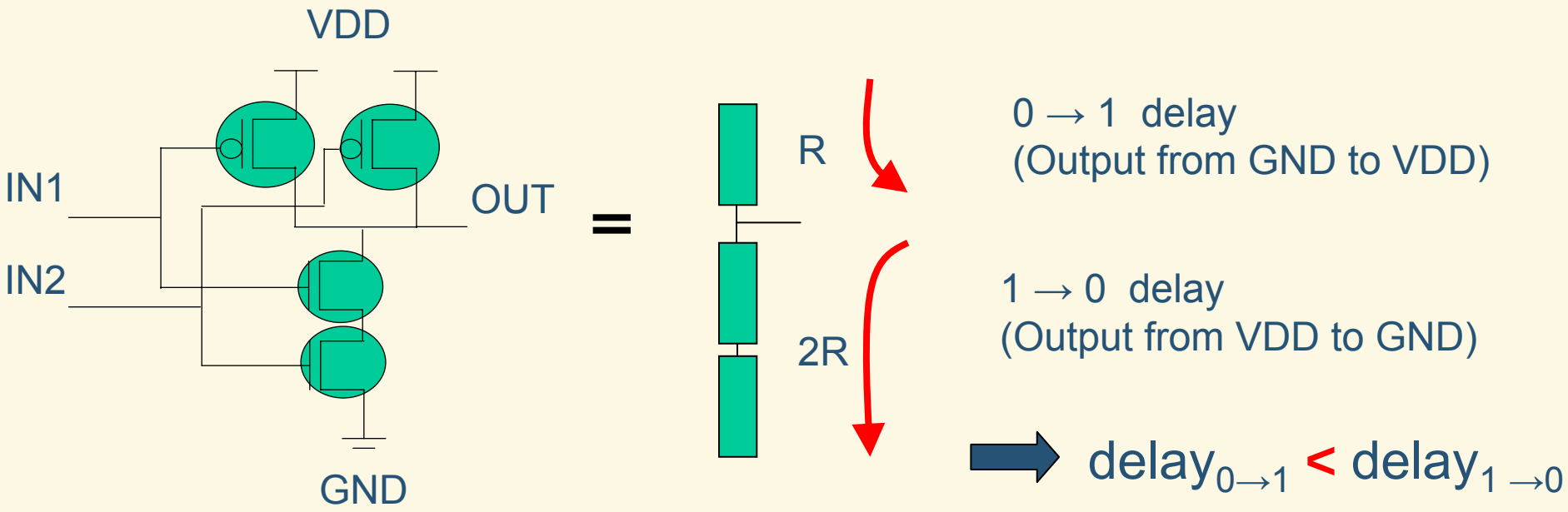
HVTO

(high V_{th} / T_{ox} = slow, low leakage)

3. Mixed Gates

Mixed-V_{th}/T_{ox} Pull-*Down/Up*-Paths

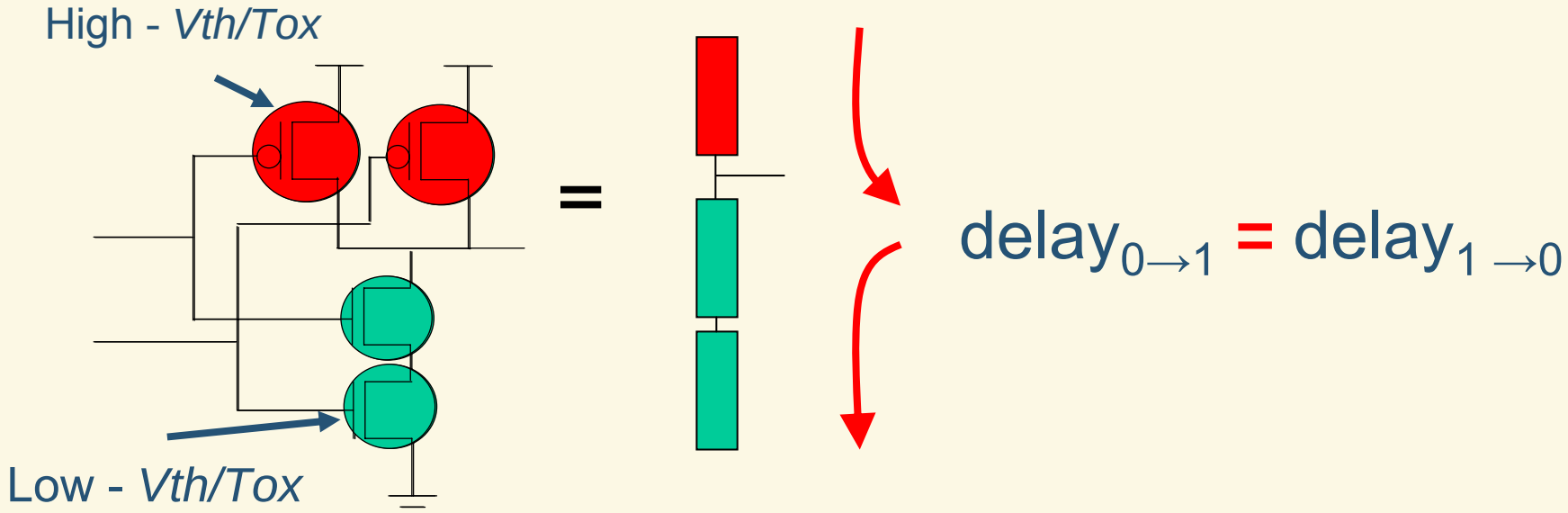
Goal (for fast gates): Preserve the delay while decreasing the leakage



But: At timing analysis → only maximum delay is considered!

Mixed-V_{th}/T_{ox} Pull-*Down/Up*-Paths Cont'd

Idea: Use different V_{th} / T_{ox} devices within a gate to adapt the delays



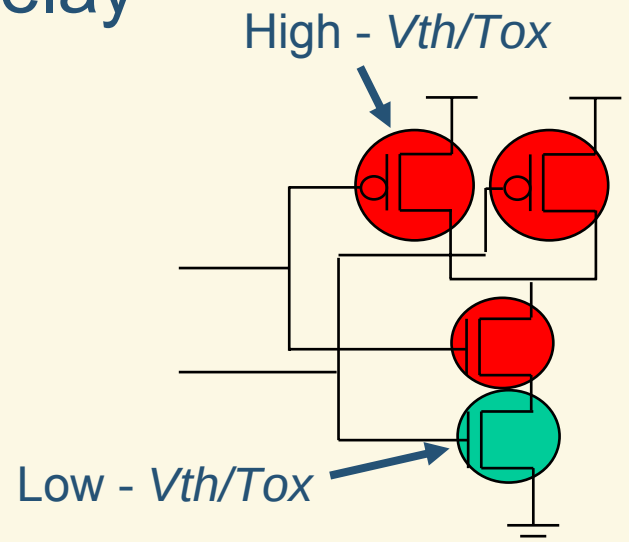
Mixed Gates

Goal: Additional gate types at constant mask count

Only two gate types in DVTCMOS / DTOCMOS

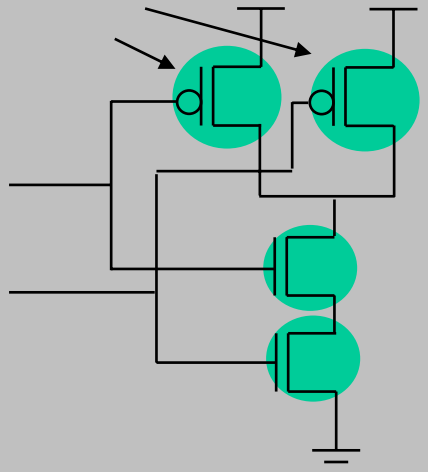
→ Problem: More *high leakage* gates after optimization as needed to keep the delay

→ *Idea:* Mixed V_{th} / T_{ox} gates to increase the amount of possible gate types



Mixed Gates - NAND2

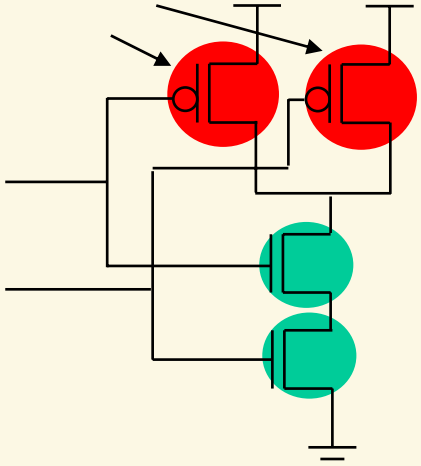
Low - *Vth/Tox*



***LVTO* gate**

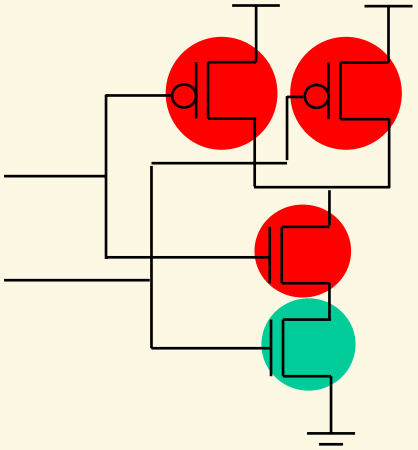
- rise time is shorter than fall time
- ***minimum delay cell***
- ***very high leakage***

High - *Vth/Tox*



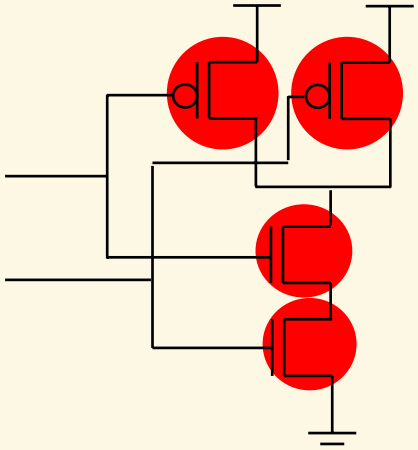
***F - MG* gate**

- rise and fall time are nearly the same
- ***minimum delay cell***
- ***high leakage***



***MG* gate**

- ***middle delay cell***
- ***middle leakage***



***HVTO* gate**

- ***maximum delay cell***
- ***minimum leakage***

4. Design Rules

Design Rules – Why?

- With two different device types:
  - @2 input gate: at least $2^4 = 16$ possibilities
  - @3 input gate: at least $2^6 = 64$ possibilities

⇒ Design rules decrease library design time

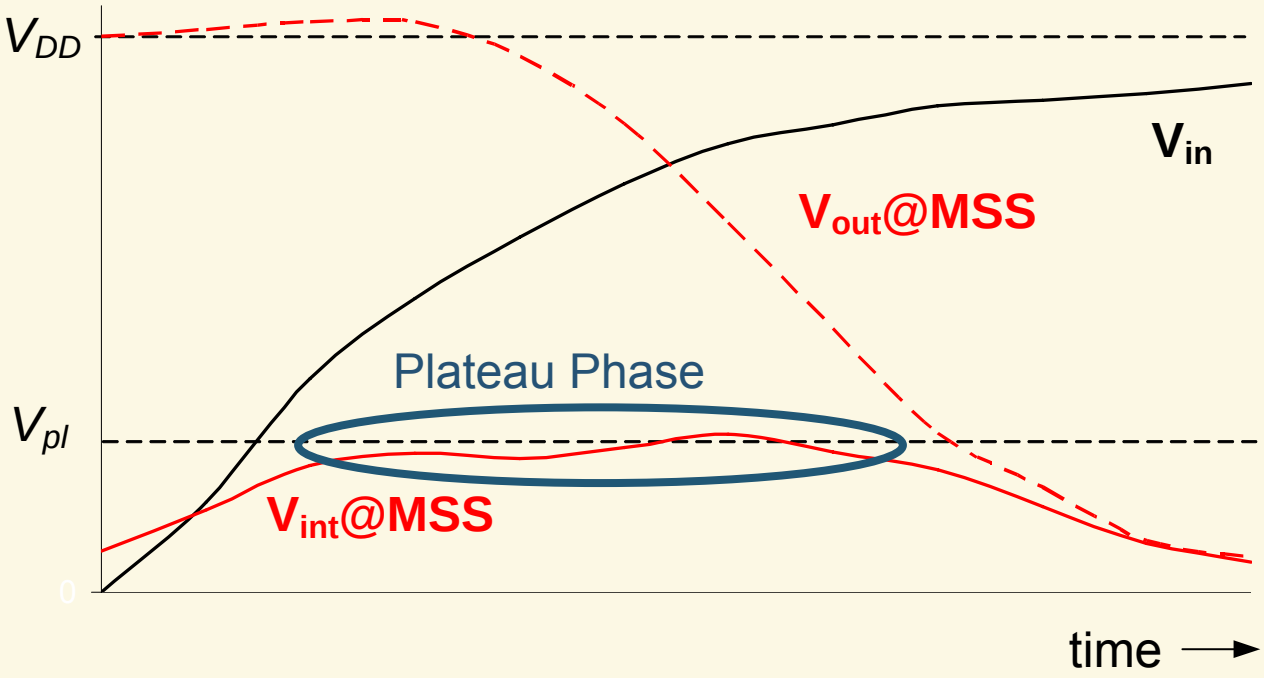
- Behavior of mixed stacks?

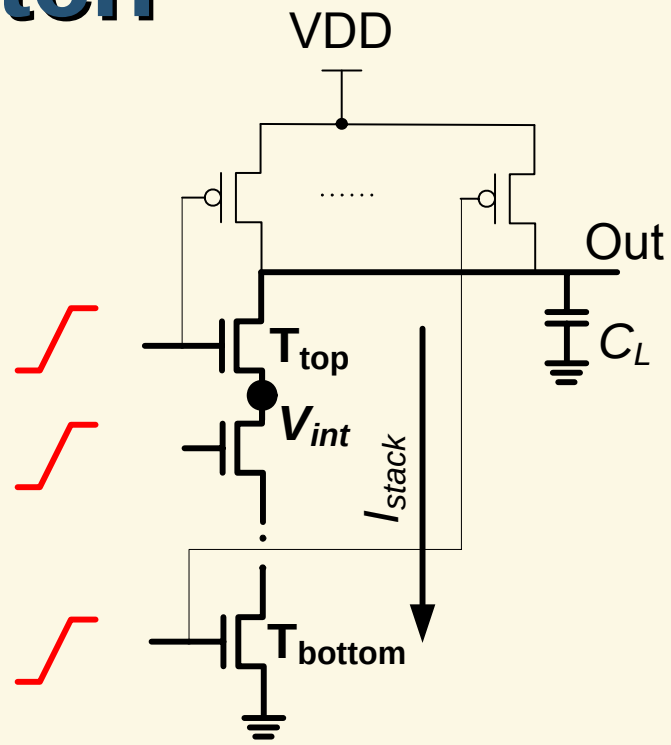
Delay in Mixed Stacks

- Two worst case scenarios:
  - Multi signal switch (MSS): all inputs switch together
  - Single signal switch (SSS): only lowest signal switches
- Plateau-Phase [1]:
  - Internal voltages and current are constant
  - Dominates delay

[1] Bisdounis et al., Analytical Transient Response and Propagation Delay Evaluation of the CMOS Inverter for Short-channel Devices", In *IEEE Journal of Solid-State Circuits,* 33-2, 1998.

Multi Signal Switch

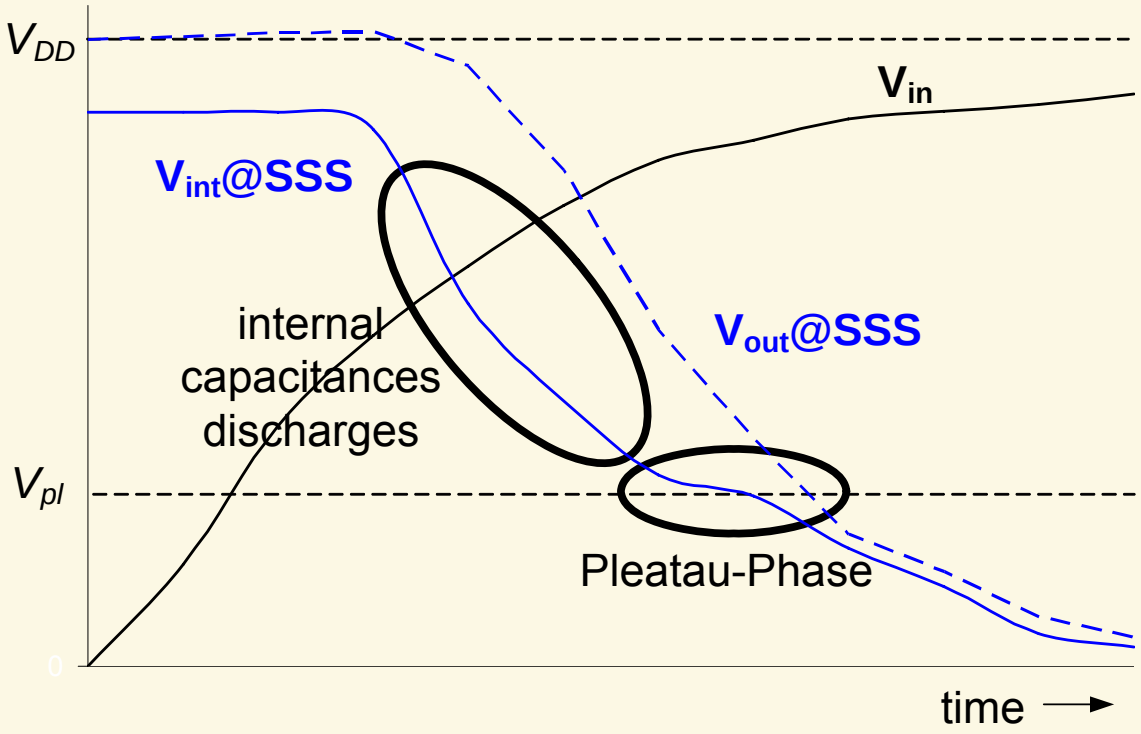


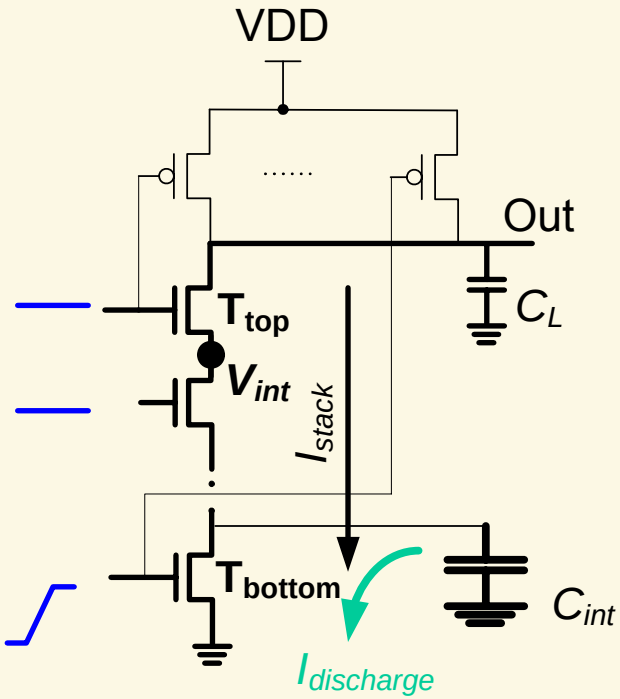


- Plateau voltage V_{pl} depends on top transistor T_{top} in stack (only T_{top} is saturated)
- V_{pl} determines current I_{stack} through stack

T_{top} has highest influence on delay @MMS

Single Signal Switch





- In start phase: internal voltages have to discharged
- T_{bottom} has highest influence on $I_{discarge}$

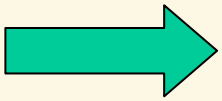
T_{top} and T_{bottom} have highest influence on delay @SSS

Leakage in Mixed Stack

Subthreshold leakage I_{sub}

- I_{sub} depends on input vector (stack effect)

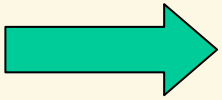
BUT: Positions of off-elements doesn't matter



Average I_{sub} is depends only on amount of high-Vth/Tox elements

Gate oxide leakage I_{gate}

- T_{bottom} connected with GND



T_{bottom} has highest average gate leakage I_{gate}

Design Rules for Mixed Stacks

Delay rule 1: If longest delay at MSS, then **low-Vth/Tox** as high as possible

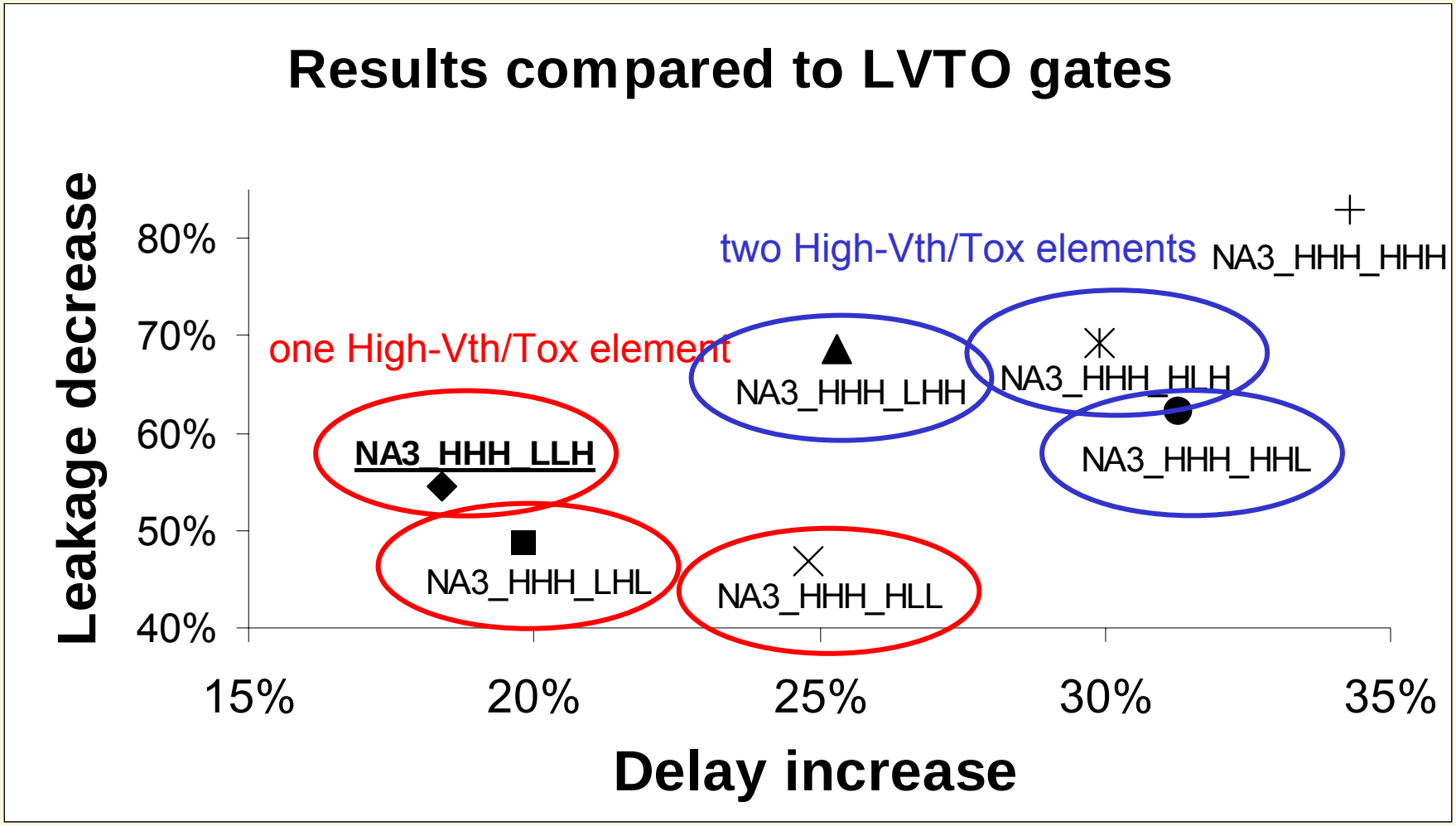
Delay rule 2: If longest delay at SSS, then at first T_{bottom} then T_{top} is **low-Vth/Tox**

Leakage rule: Lowest possible transistor is **high-Vth/Tox**

Rules are applied at design phase, until desired delay is reached.

5. Results

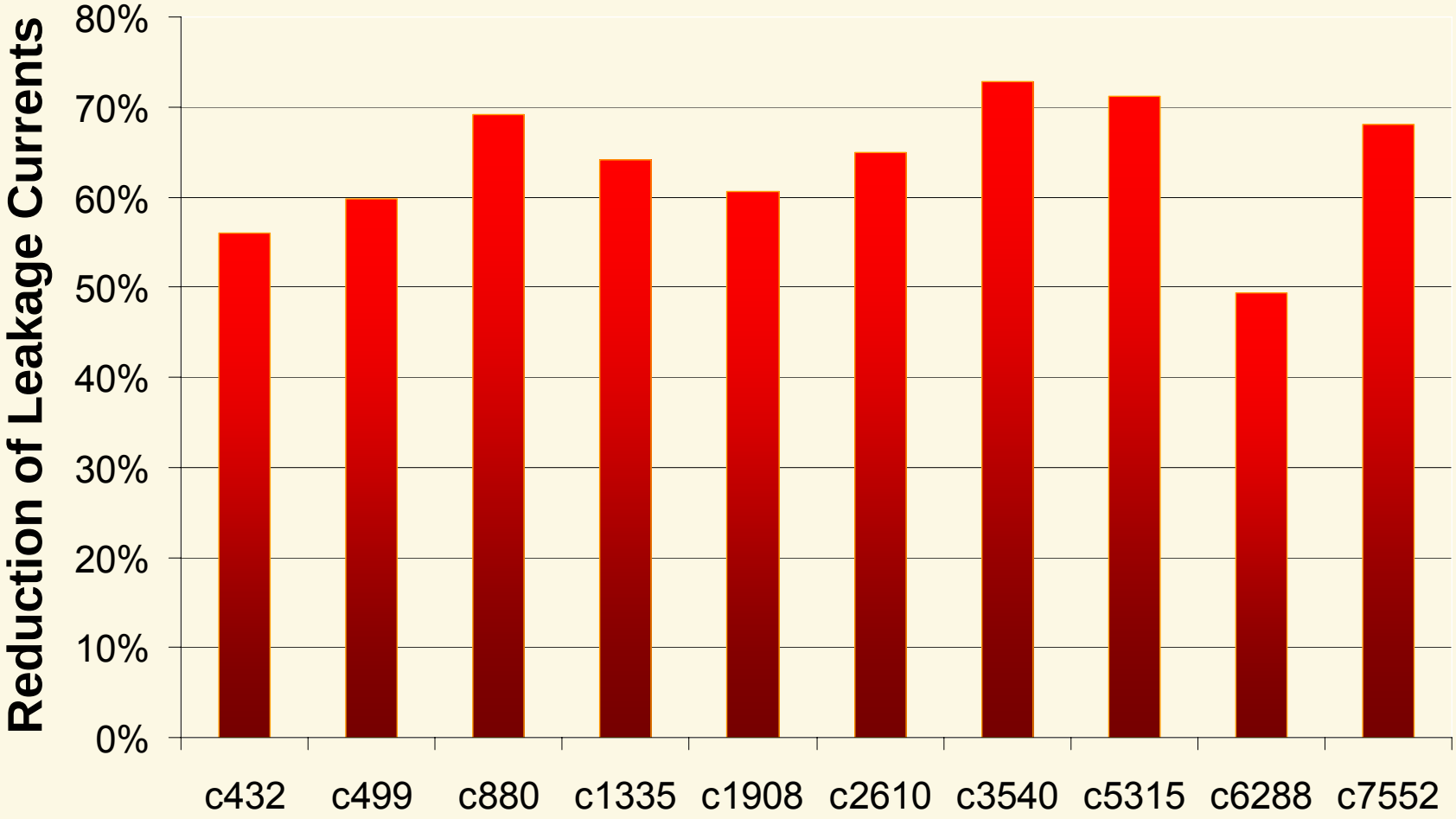
Example: NAND3 – Mixed Stack



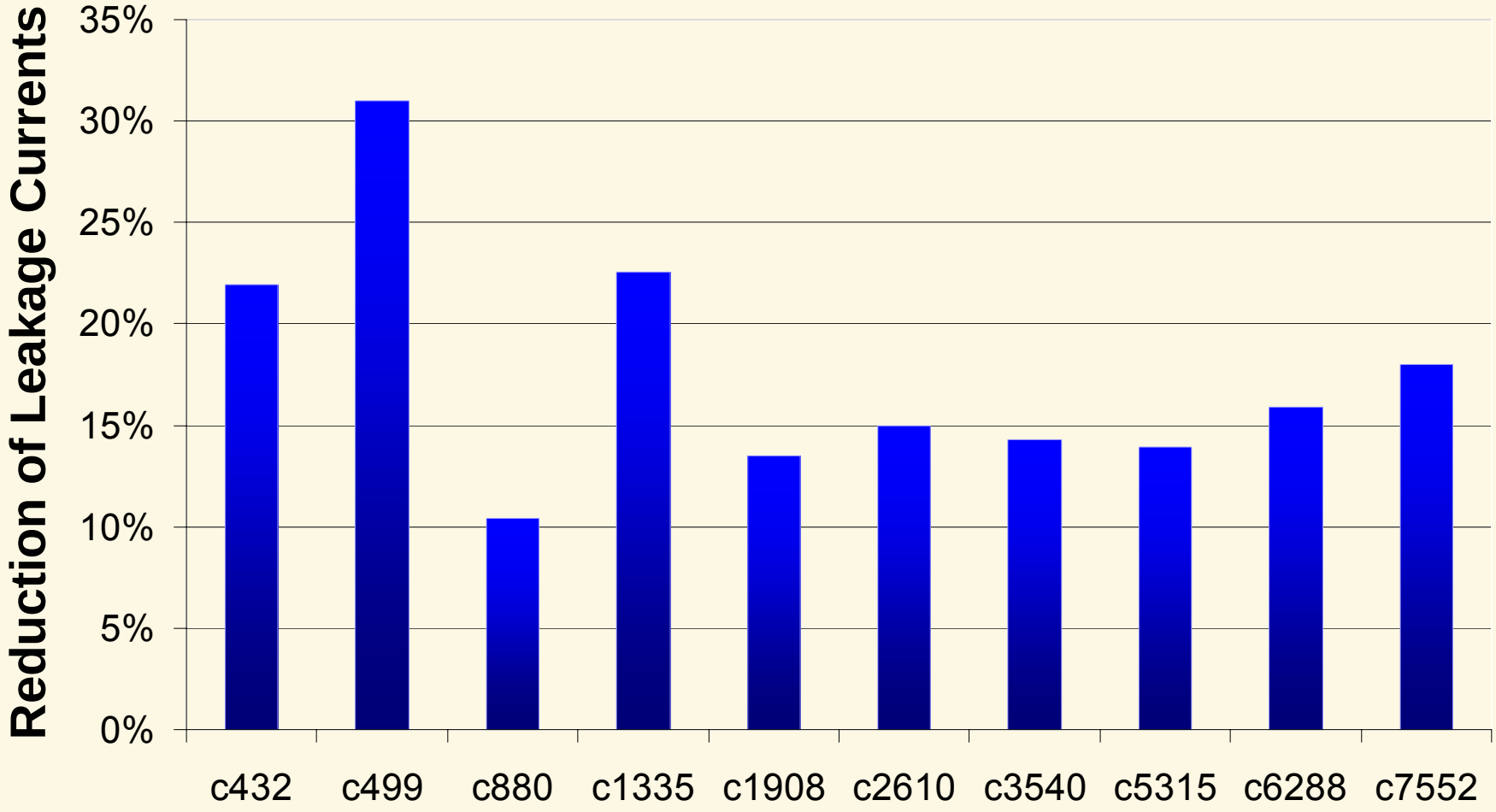
Benchmark results

- Gate library:
  - 65 nm BPTM technology
  - 42 gates
  - for each gate LVTO, HVTO, F-MG, MG type
- ISCAS benchmark designs (200 – 4000 gates)
- Each design implemented with LVTO, DVTCMOS/DTOCMOS, and *Mixed Gates* approach

LVTO vs. Mixed Gates @ ISCAS



DTCMOS vs. Mixed Gates @ ISCAS



5. Conclusions

- *Mixed Gates* approach combines advantages of DVTCMOS and DTOCMOS at transistor and gate level
- Proposed design rules ease library design phase
- Average 65% *(vs. LVTO)* and 18% *(vs. DVTO-CMOS)* leakage reduction at constant delay

Thank you!

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