Total Leakage Power Optimization with Improved Mixed Gates

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ABSTRACT

Gate oxide tunneling current I_{gate} and sub-threshold current I_{sub} dominate the leakage of designs. The latter depends on threshold voltage V_{th} while I_{gate} vary with the thickness of gate oxide layer T_{ox}. In this paper, we propose a new method that combines approaches of Dual Threshold CMOS (DTCMOS), mixed-T_{ox} CMOS, and pin-reordering. As the reduction of leakage leads to an increase of gate delay, our purpose is the reduction of total leakage at constant design performance. We modified a given technology and developed a library with a new mixed gate type. Compared to the case where all devices are set to high performance, our approach achieves an average leakage reduction of 65%, whereas design performance stays constant.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: Integrated Circuits – *design aids*

General Terms

Algorithms, Performance

Keywords

Leakage currents, threshold voltage, MVT

1. INTRODUCTION

Aggressive downscaling of CMOS devices in each technology generation resulted in higher integration density and performance. At the same time, leakage currents increased exponentially and have become a major contributor to total power dissipation on chips. Today, up to 50% of IC power dissipation is based on leakage currents [7]. There are several reasons for this growth. One reason is the lowering of transistor threshold voltage V_{th}. This is necessary to meet the desired performance, because the supply voltage V_{DD} is scaled down. Because V_{th} is not only proportional to delay but also to channel leakage sub-threshold current I_{sub} increases exponentially. As an additional consequence of downscaling, thickness of gate oxide layer decreased drastically. In 65nm technologies the oxide layer has a thickness of less then 20 atom layers. This forces an increase of gate tunneling currents and as a consequence an increase of gate leakage I_{leak}.

Since the last decade, reduction of leakage currents is a main part of low power research, whereas a lot of approaches where developed. Kao proposes in [6] the use of additionally *sleep* transistors which can disconnect supply from design in idle modes. Another approach is the dynamic scaling of supply voltage adjusted to required performance [8]. Furthermore, a very common solution for sub-threshold leakage current and performance tradeoff is the application of two device types which vary in their threshold voltage [13]. Thus, the devices differ in performance and leakage currents. This Dual Threshold CMOS (DTCMOS) design technique applies fast devices in critical paths while slower devices with lower leakage are used in noncritical paths. Wei presents in [15] a transistor level DTCMOS approach. A related design technique is the application of two transistors types, which differ in the thickness of gate oxide layer T_{ox} [12]. This Dual-T_{ox} allows the reduction of gate oxide leakage currents. The problems of common leakage reduction techniques are additional devices (i.e. sleep transistors) or that only one component of leakage is reduced. Moreover, transistor level approaches are not applicable for standard cell design and require long optimization time. Our proposed approach is an improved combination of DTCMOS and Dual-T_{ox} design techniques [10, 11]. We combine reduction techniques on transistor and gate level to reduce total static power dissipation, whereas the delay of designs stays the same. We create a mixed-V_{th} and mixed-T_{ox} gate type and append pin-reordering techniques.

In this paper we introduce basics of leakage power dissipation and DTCMOS design in section 2. We describe a method for selecting appropriate values for transistor technology parameters in section 3. In section 4, the idea of improved mixed gates is proposed. The application of pin-reordering and an optimization algorithm is introduced in section 5. This is followed by simulation results in section 6 and the conclusion in section 7.

2. PRELIMINARIES

2.1 Transistor parameters

The leakage of a transistor is the sum of all currents which are not desired. The biggest influence originates from sub-threshold current I_{sub} and gate oxide current I_{gate}. The sub-threshold current is given by [3]:

$$I_{sub} = I_0' \frac{\sqrt{NDEP}}{L_{eff}} \cdot exp\left(\frac{1}{n\beta}\left(V_{gs} - V_{th0} + \gamma' \cdot \sqrt{NDEP} \cdot T_{ox} V_{bs} + \eta' \frac{T_{ox}}{L_{eff}^2 \cdot \sqrt{NDEP}} V_{ds}\right)\right) \cdot \left(1 - exp\left(-\beta V_{ds}\right)\right)$$

$$\beta = \frac{kT}{q}, I_0' = \mu \cdot W \cdot \sqrt{\frac{q\varepsilon_{Si}}{2\Phi_S}} \cdot \beta^2, \eta' \approx \frac{\left(E_{TA0} + E_{TAB} \cdot V_{bs}\right)\varepsilon_{Si}^{3/2}}{D_{SUB}{}^2 \cdot \varepsilon_{ox}\sqrt{q}}, \gamma' = \frac{\sqrt{2q\varepsilon_{Si}}}{\varepsilon_{ox}}$$

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T is the operating temperature, n is the subthreshold swing coefficient, V_{th0} is the zero-bias threshold voltage, V_{gs} is the gate-source voltage, V_{bs} is the bulk-source voltage, V_{ds} is the drain-source voltage, Φ_S is the surface potential. D_{SUB} and E_{TA0} are technology dependent drain induced barrier lowering (DIBL) coefficients, and E_{TAB} is a body-bias coefficient. The terms q, k, μ, ε_{ox}, and ε_{Si} correspond to physical constants (respectively, charge on an electron, Boltzmann's constant, electron surface mobility, gate dielectric constants of gate oxide and silicon). *NDEP* labels the channel doping concentration, T_{ox} the thickness of the oxide layer, and L_{eff} the effective gate length. Mukhopadhyay and Roy could show in [9] that variations on the latter three technology parameters have the biggest influence on I_{sub}.

Gate oxide current is primarily based on tunneling currents in MOS devices. Physically, these are the direct tunneling (DT) current in the gate-channel region, and the edge direct tunneling current (EDT) in gate-drain/gate-source overlapping regions. The density for direct tunneling current, which is most dominant type, can be described as [4]:

$$J_{DT} = A \cdot \left(1 + B \cdot T_{ox}\right) \cdot exp\left(C \cdot T_{ox}\right)$$

$$A = \frac{4\pi q m_x}{\hbar^3}(kT)^2, B = \frac{4\pi \cdot \sqrt{2M_{ox}} \cdot kT}{2\sqrt{E_B} \cdot \hbar},$$

$$C = \frac{E_{F0,Si/SiO_2} \cdot 4\pi \cdot \sqrt{2M_{ox}}\sqrt{E_B}}{kT \cdot \hbar}$$

$E_{F0,Si/SiO2}$ is the Fermi level at the Si/SiO_2 interface, and E_B is the barrier height. The terms $\hbar$ is the Plank's constant, m_x is $0.19M_{ox}$ for electron tunneling and $0.55M_{ox}$ for hole tunneling, and M_{ox} the effective electron, respectively hole mass in the oxide. In contrast to sub-threshold current, gate oxide leakage is most sensitive to T_{ox} only [9].

2.2 DTCMOS

The Dual Threshold CMOS (DTCMOS) design techniques are based on the dependency of delay and leakage of a gate from threshold voltage V_{th} of its transistors. High V_{th} results in a relative long delay and low leakage currents, while low V_{th} results in a relative short delay and high leakage currents. Thus, known DTCMOS approaches [13] use LVT gates, which consist of low V_{th} transistors, and HVT gates, which consist of high V_{th} transistors. The purpose of DTCMOS optimization algorithms is to increase the number of HVT gates at constant performance. Hence, only gates in noncritical paths will be transformed into HVT gates, while gates in critical paths stay LVT type.

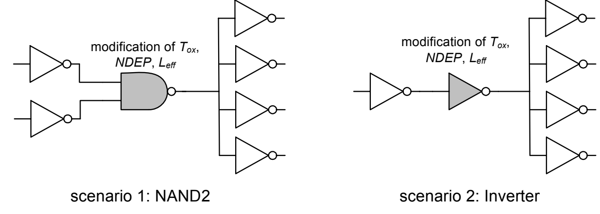

Figure 1: Test environment for determination of transistor parameters

3. MODIFICATION OF L_{eff}, T_{ox}, AND NDEP

The As shown in section 2 and in [9], the most influential technology parameters for sub-threshold and gate leakage current are the effective gate length L_{eff}, the oxide layer thickness T_{ox}, and the channel doping concentration *NDEP*. Thus, we varied these parameters to find the best choice for NMOS and PMOS transistors. Firstly, we searched for fast transistors with an applicable leakage. Secondly, transistors with low leakage were determined working with an applicable delay. In common approaches, T_{ox} is modified at NMOS transistors only, because I_{gate} decreases one decade less on PMOS transistors compared to NMOS. But, as shown in section 2, T_{ox} determines threshold voltage V_{th} as well. Thus, we modify T_{ox} on PMOS transistors as well, intending a decrease of I_{sub}. We choose the predictive 65nm BPTM models [4] as our base technology. We consider two scenarios, the variations at a NAND2 gate as well as at an inverter (see figure 1).

The parameters were varied independently of each other. We measured delay, input capacity, and average leakage current. The latter one is the sum of average sub-threshold and gate leakage current of every input combination divided by count of combinations. The results are depicted in figure 2 and figure 3.

The input capacity C_{in} determines the delay of previous gates as load and is proportional to the dynamic power dissipation. It is only affected by the effective gate length L_{eff}. Thereby, decreasing L_{eff} reduces C_{in} and delay. But even slight variations of L_{eff} can strongly increase the average leakage. As random parameter variability increases radically in upcoming technologies [2], we abandoned modification of L_{eff} for fast transistors. Variation of L_{eff} is not recommended for low leakage transistors as well, because C_{in} rises strongly with increasing L_{eff}. Reduction of gate oxide thickness T_{ox} is not recommended, as a slightly reduced delay yields to drastically increasing leakage. But, increasing T_{ox} is a good tradeoff between delay and leakage in contrast to modifications on *NDEP* and L_{eff}.

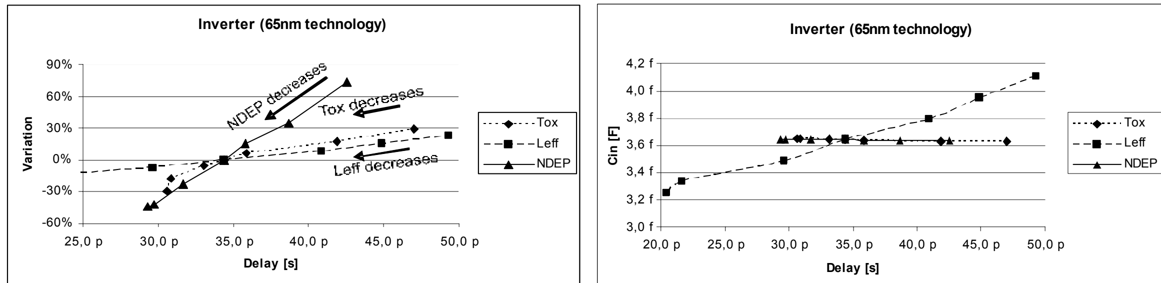

Figure 2: Behavior of delay and input capacity Cin of inverter in a predictive 65nm technology by variation of Tox, NDEP, and Leff

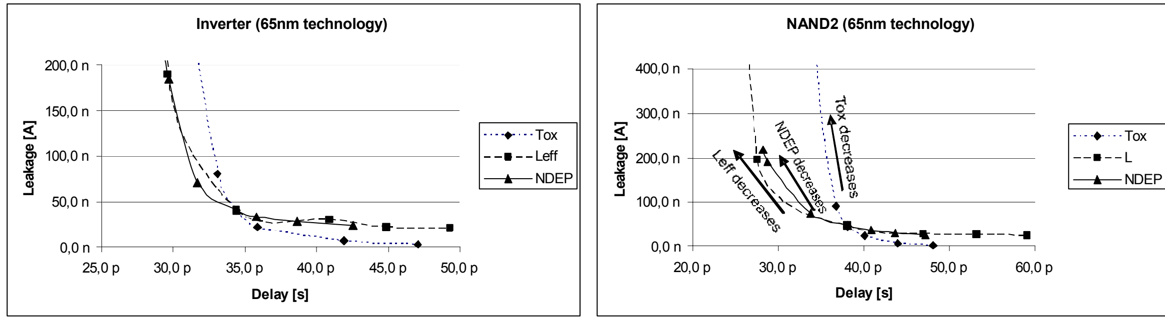

Figure 3: Tradeoff between delay and leakage at inverter and NAND2 in a 65nm technology

Reduction of *NDEP* has the best effect on decreasing delay and leakage. Additionally, *NDEP* is not as strongly affected by random parameter variations as the two other parameters.

As a result of our simulations we decided to choose a *NDEP* which is about 30% lower than the standard technology value for fast transistors. The values of T_{ox} and L_{eff} are not changed. For low leakage transistors we chose a *NDEP* and a T_{ox}, which are approximately 10% higher than standard values. L_{eff} remained constant again.

Certainly, the extracted parameter values only aim at this special technology. But some results can be adapted to related technologies. These are the inadvisable variation of L_{eff}, the good tradeoff between increasing T_{ox} and delay, and the good tradeoff between decreasing *NDEP* and performance.

4. IMPROVED MIXED GATES

4.1 Mixed Threshold Voltages (MVT)

The idea of mixed threshold voltages is based on the Dual Threshold Voltage (DTCMOS). Compared to common leakage reduction methods on gate level, the proposed MVT approach uses transistors with different threshold voltages *within* gates [10, 11]. Hence, we can combine the advantages of transistor and gate level solutions. Optimization algorithms on gate level evaluate relatively fast, but the results are far from an optimum solution. In contrast, algorithms on transistor level are very accurate but the evaluation time increases drastically with increasing design size, because the degrees of freedom rise exponentially with increasing gate count. Additionally, approaches on transistor level rise development costs, because these solutions are not applicable for standard cell design techniques. The gate level MVT approach allows more accurate improvement than common gate level solutions, and requires much less time than solutions on transistor level.

Only the maximum delay of a gate is important for determining design performance. Thus, we slowed down transistors within a gate, which does not determine the maximum delay of a gate. This resulted in enhanced LVT gates, the MLVT gates. For example, maximum delay of NOR gates only depends on its PMOS transistors. Hence, we use slow high V_{th} NMOS transistors (see figure 2b). This decelerates falling slopes, but rising slopes still have higher delay. In common approaches, this slowdown is performed by sizing, which slightly increases dynamic power dissipation.

One problem of standard gate level DTCMOS approaches is the limited amount of gate types. To improve this, we developed MVT gates, which consist of different transistor types. In contrast to MLVT gates, stacks consist of different transistor type as well (see figure 2). It can be shown that mixed stacks have lower leakage than unmixed stacks with the same delay. Hence, compared to DTCMOS design techniques the fabrication costs stays nearly constant, because three different types of gates can be implemented at constant chip mask count.

4.2 Improvement (iMVT)

We improved the mixed threshold voltage approach by adapting transistors with different V_{th} and T_{ox} within gates. Hence, subthreshold and gate leakage current can be concurrently reduced in contrast to common dual-V_{th} and dual-T_{ox} design techniques. The improvements resulted into improved HVT (iHVT), improved MLVT (iMLVT), and improved MVT (iMVT) gates. The new gate types apply iHVT transistors with a V_{th} and T_{ox}, which both are higher than at fast transistors in LVT gates.

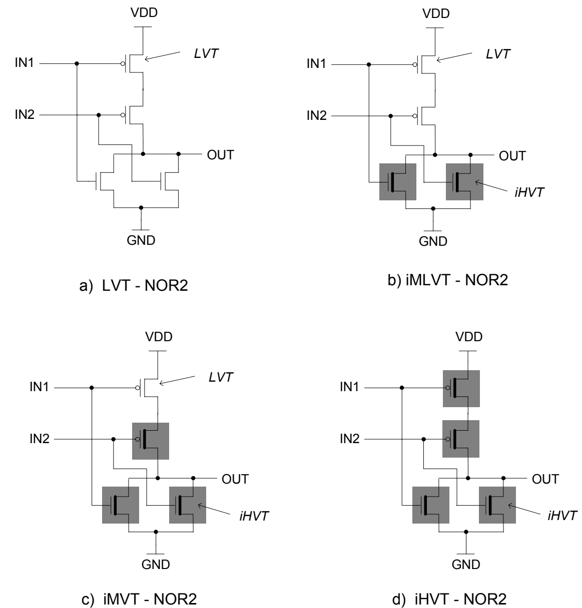

Figure 4: Different implementations of NOR2

Table 1: characteristics for different types of NOR2 gate

	iHVT	LVT	iMLVT	iMVT
PMOS (type, width [m])	iHVT,1µ	LVT, 1µ	LVT, 1µ	HVT, 1µ
	iHVT,1µ	LVT, 1µ	LVT, 1µ	LVT, 0.9µ
NMOS (type, width [m])	iHVT, 0.2µ	LVT, 0.2µ	iHVT, 0.3µ	HVT, 0.2µ
	iHVT, 0.2µ	LVT, 0.2µ	iHVT, 0.3µ	HVT, 0.3µ
T_{max_rise} [s]	88.0 p	**66.0 p**	**66.0 p**	77.0 p
T_{max_fall} [s]	**90.0 p**	65.0 p	65.0 p	**78.0 p**
$I_{sub_average}$ [A]	7.3 n	70.4 n	60.5 n	32.0 n
$I_{gate_average}$ [A]	3.3 n	16.1 n	6.5 n	4.6 n
I_{leak} at "00" [A]	7.5 n	56.6 n	14.3 n	10.3 n
"01" [A]	14.6 n	129.3 n	120.9 n	111.0 n
"10" [A]	12.6 n	113.6 n	105.2 n	14.8 n
"11" [A]	7.6 n	44.5 n	27.8 n	10.3 n
	6.4 f	6.4 f	6.8 f	6.4 f
E_{leak} (t = 1µs) [Ws]	9.5 f	77.4 f	60.3 f	32.9 f

4.3 Library creation

We built up a library with four gate types (LVT, iHVT, IMLVT, iMVT). We sized all gates under the constraints of nearly identical maximum delay of rising and falling slopescal and that equal gates reach the same input capacity except the iMLVT gates. The latter ones have a slightly higher input capacity to fit the same delay as corresponding LVT gates. After sizing, we initially estimated the leakage currents for all input combinations and the sum of input capacities of both inputs. Then, we determined the average leakage energy for 1µs. As an example, gate characteristics for different implementations of a NOR2-gate are shown in table 1. As expected, the input capacity C_{in} of iMLVT type is slightly higher compared to other types. Hence, the dynamic power dissipation, which is directly proportional to C_{in} [14], is increased as well. LVT type compared to iMLVT type has a difference of about 25% and 5% related to leakage energy and dynamic energy dissipation, respectively. Because a ratio of 50% between leakage and dynamic energy dissipation can be assumed [7, 6], the reduction of leakage is higher than the increase in dynamic energy.

5. ALGORITHMS

5.1 Pin-Reordering

The total leakage of a logic gate depends on the input vectors as well. Sub-threshold currents depend on the *stack effect*, which occurs if more than one transistor of a stack is non-conducting [1]. Then, I_{sub} decreases strongly. Unfortunately, the *stack effect* is not applicable if the input vectors cannot be changed.

The dependency of gate leakage currents from input vectors is depicted in NMOS stack in figure 3. In both cases a gate tunneling current I_{gb} occurs from gate to bulk through the channel of the conducting transistor. At case a), the upper transistor of the stack is conducting and the voltage at node n is the difference between V_{DD} and $V_{th,NMOS}$. Hence, there is an additional reverse gate tunneling current $I_{gd,l}$ from drain to gate through the gate-to-drain overlap region of the non-conducting lower transistor. At case b), only the lower transistor is conducting and node n is connected with GND. Hence, there are gate tunneling currents $I_{gb,l}$ and $I_{gs,l}$ in the gate-to-drain and gate-to-source overlap regions of the lower transistor. Furthermore, there is an additionally reverse gate tunneling current $I_{gd,u}$ through gate-to-drain region of upper transistor. Hence, the gate leakage at case a) is lower than gate leakage at case b). At both cases, the whole stack is not conducting. Thus, the position of input pins can be changed, without changes in the function of the stack but with changes in leakage currents.

The dependency of input vectors increases at mixed stacks as in iMVT gates. Here, the gate tunneling current from gate to bulk in the channel region can be reduced additionally at the iHVT transistors. Based of dependency of leakage from the input vectors, we implemented a pin-reordering algorithm. Firstly, we determine the state probability of all signals in the design based on the approach outlined in [5]. Next, we reorder the input pins of every gate so that states with low leakage are forced.

5.2 Gate transfer

The purpose of implemented gate transfer algorithm is reducing leakage at constant design performance. At first, signal probabilities are estimated. Then, for every gate G the expected average leakage $I_{exp,LVT}(G)$ for LVT type is determined. Subsequently, for all gates the weighting factor $\Psi(G)$ is estimated. $\Psi(G)$ is the product of the inverse leakage $I_{exp,LVT}(G)$ and delay $t_{d,HVT}(G)$ of the HVT type of the gate. Next, all gates are set to iHVT type and determination of design timing behavior follows. This step is followed by detection of the critical path. In this path, the gate with highest $\Psi(G)$ will be transferred to iMLVT type and the new critical path will be detected. This step is repeated until all critical paths are completely optimized. Next, for all gates of iMLVT type the determination of slack $t_{slack}(G)$ follows. Slack is the time by which a gate can be slowed down, without impacts on design performance [5]. If $t_{slack}(G)$ is higher than the difference between gate delay of iMLVT and iMVT type, the gate will be transferred to the latter. The proposed pin-reordering is the last part of the algorithm, which is depicted in figure 6.

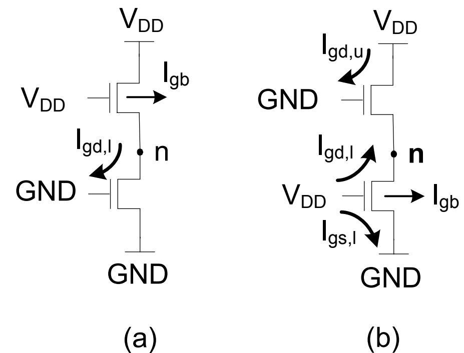

Figure 5: Gate tunneling currents at 2-NMOS-stack

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Determine signal probabilities
For all gates
    Estimate I_exp,LVT(G)
    Estimate Ψ(G)=t_d,iHVT(G)*(I_exp,LVT(G))-1
Initialize all gates as iHVT gates
Determine design timing behavior
While critical path can be optimized
    transfer gate with Ψ_max(G) to iMLVT type
    search for critical path
For all iMLVT gates
    Estimate t_slack
    if t_slack > t_LVT(G)-t_iMVT(G)
    then transfer gate to iMVT type
For all gates
    if high probability of high leakage state
    then reorder inputs
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Figure 6: Optimization algorithm

6. EXPERIMENTAL RESULTS AND DISCUSSION

We implemented three versions of ISCAS designs. At first, all designs were built-up of LVT gates, which consist of transistors with low T_{ox} and low V_{th}. Next, we implemented a DTCMOS version of the designs, which consists of LVT and iHVT gates. The last design type, which was improved by pin-reordering, consists of iMLVT, iHVT, and iMVT gates. We assumed a signal probability of 0.5 for every input. With HSpice simulation we determined the average leakage and the total energy dissipation for frequency $f=1GHz$ and activity $\alpha=1\%$. The wire loads were ignored. The results are shown in figure 7 and table 2.

The average leakage reduction for raw LVT designs is ca. 65% and at previously optimized DTCMOS designs ca. 18%. The average total power reduction is 45% for raw LVT designs and about 10% for previously optimized DTCMOS designs.

7. CONCLUSION

In this paper we proposed a new approach to reduce the total leakage currents within designs. We varied the transistor parameters *NDEP*, L_{eff}, and T_{ox} to get applicable fast transistors and transistors with low leakage. Thereby, we could show that variation of L_{eff} is not recommended. We used those transistors to build up gates with equal and with mixed transistor types. These improved gates yield significant reduction of sub-threshold and gate oxide leakage keeping constant delay. We implemented an algorithm, which transfer all gates in non-critical paths of designs in slower gates. These slower gates have the advantage of lower leakage currents. Additionally, we implemented a pin-reordering algorithm to further reduce the leakage. We verified our proposed approach at ISCAS'85 designs. The optimized designs have the same performance than raw designs. We could reduce the leakage at raw designs by average 65%. The average leakage of previously optimized DTCMOS designs could be reduced by average 18%.

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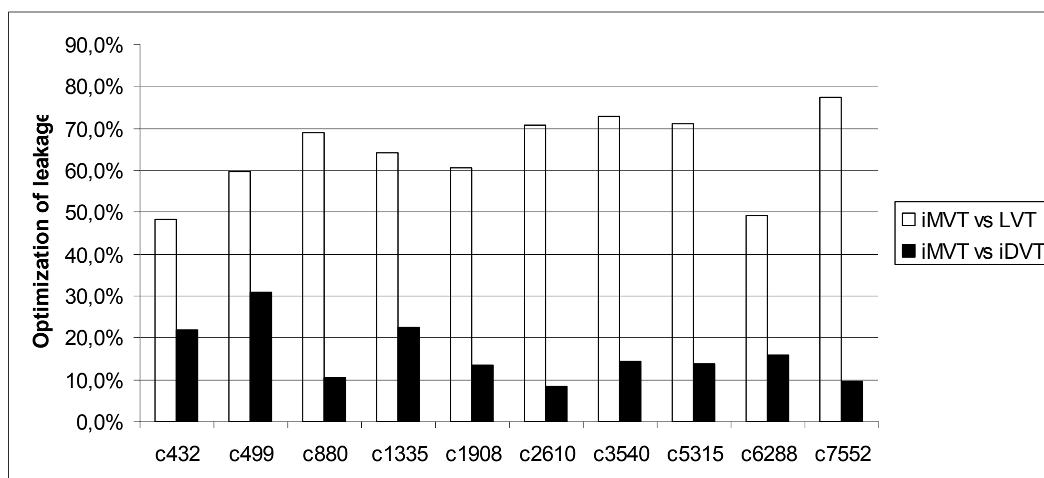

Figure 7: Optimization of total leakage at ISCAS'85 circuits in LVT, iDVT, and iMVT implementation in 65nm technology

Table 2: Simulation results for ISCAS'85 circuits in 65nm technology

		iDVT	iMVT		Leakage			Total energy at f=1GHz, α=1%		
Name	#all gates	#iHVT	#iMLVT	#iMVT	LVT [A]	iDVT [A]	iMVT [A]	LVT [Ws]	iDVT [Ws]	iMVT [Ws]
c432	155	79	58	18	23.7 µ	15.7 µ	12.3 µ	30.9 µ	22.6 µ	19.9 µ
c499	474	279	150	45	75.2 µ	43.8 µ	30.2 µ	106.7 µ	70.4 µ	58.0 µ
c880	393	330	60	3	60.9 µ	21.0 µ	18.8 µ	93.2 µ	49.9 µ	47.7 µ
c1335	738	501	195	42	114.9 µ	53.2 µ	41.2 µ	144.0 µ	80.4 µ	68.6 µ
c1908	453	305	134	14	76.7 µ	34.9 µ	30.2 µ	109.8 µ	67.4 µ	62.2 µ
c2610	663	604	50	9	108.3 µ	34.4 µ	31.6 µ	178.9 µ	95.5 µ	93.3 µ
c3540	1093	938	138	17	161.0 µ	51.1 µ	43.8 µ	234.5 µ	114.8 µ	108.5 µ
c5315	1781	1544	171	66	279.2 µ	93.4 µ	80.4 µ	436.9 µ	235.9 µ	225.3 µ
c6288	2701	1422	1223	56	416.5 µ	250.9 µ	211.0 µ	792.9 µ	610.3 µ	568.2 µ
c7552	1874	1783	85	6	310.6 µ	77.4 µ	70.0 µ	545.3 µ	285.1 µ	278.2 µ

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