Automatic Layout Integration of Bulk Built-In Current Sensors for Detection of Soft Errors

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***Abstract*— Soft error resilience is of rising importance for the design of integrated circuits realized in CMOS nanometer technologies. Therefore, Bulk Built-In Current Sensors (BBICS) have been proposed as a fast and efficient technique for detecting transient faults that might lead to soft errors. An important requirement for application of these sensors in common designs is the automatic integration. The aim of this work is to present a methodology for automatic insertion of BBICS in common standard cell designs. Further, two different placement strategies are introduced and compared. Experiments demonstrate the feasibility of the approach and indicate requirements for future BBICS developments in order to reduce area offset.**

Keywords—Soft error, transient fault, EDA, Bulk Built-in Current Sensors

I. INTRODUCTION

Current nanometer scale CMOS technologies are facing an increasing amount of fault sources that can lead to serious reliability problems. Examples are effects like parameter variations [1], oxide breakdown [2], and radiation [3]. In case of the latter, high energetic particles inject electrical charge into sensitive regions of the semiconductor devices that can result in transient faults and soft errors [4]. For long time, researches on soft errors due to radiation focused mainly on memories and avionics and aerospace applications. However, with the uprising of nanometer scale technologies, soft error resilience is also a concern for applications on ground level. Several concurrent error detection and/or correction techniques have been presented to avoid the effects of radiation. This includes multiple clocking schemes [5], checker based arithmetic units [6], and selective redundancy [7]. In contrast to these gate and system level techniques, Bulk Built-In Current Sensors (BBICS) are an approach on transistor level, which enables the detection of radiation induced particle strikes immediately after its occurrence [8]. The advantages of these sensors are fast error detection and low power penalty with moderate costs in terms of area [9-11].

However, to the best of our knowledge, there is still no solution for automatic integration of BBICS in random designs published. Thus, this work presents a modified standard cell design flow that enables the automatic insertion of modular BBICS [9, 12]. Further, requirements for layout and placing algorithms will be introduced. It can be said that the results of this work are an essential step towards the consolidation of the BBICS approach for application in common designs.

The rest of the paper is organized as follows. Section 2 gives preliminary information, while section 3 details the proposed flow. Section 4 discusses the layout design of the standard cells and Section 5 presents experimental results. Finally, section 6 concludes this work.

II. BASICS

This section presents fundamental information that support the understanding of the paper.

A. Standard Cell Design

Standard cell design is a CMOS design methodology that applies cells, which are pre-designed and pre-verified on logic, schematic, and layout level. This enables the separation of design tasks into different abstraction layers, *e.g.*, logic synthesis, placement, and routing [13].

The layout of each standard cell has same height but different widths. Further, cells are designed such that they can be placed horizontally next to each other. This also includes the adequate positioning of supply wires as well as N- and P-wells. Thus, cells can be organized in rows during placement.

B. Transient Faults and Soft Errors

Strikes of high energetic ion particles, like alpha particles or neutrons, into a sensitive region of an integrated device can cause transient faults that might turn into soft errors [4].

The most susceptible regions to ionizing radiation events are reverse biased junctions, as for instance the drain of a transistor in off-state. In the event of a hit, the particle's path forms an electron-hole pair track. When this track traverses a depletion region, carriers are rapidly collected by the electric field creating a distortion of the potential into a funnel shape [14]. This carrier collection can be observed as a current and voltage transient on the affected node. The following phase is dominated by diffusion, in which additional charge diffuses into the depletion region over a longer period of time [4].

The described effect can be modeled by double exponential current pulse I_{strike} by following equation [4]:

$$I_{strike}(t) = \frac{Q_{coll}}{t_f - t_r}\left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right) \quad (1)$$

with Q_{coll} is the total collected charge, t_r indicates the time constant for the funnel collection and t_f represents the second phase of carrier collection.

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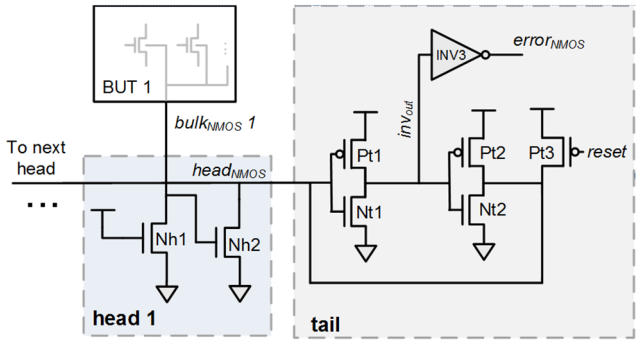

Fig. 1. Principal architecture of modular BBICS (mBBICS)

C. Modular Bulk Built-In Current Sensors

The principal idea of a Bulk Built-In Current Sensors (BBICS) is to measure the anomalous current in the transistor bulk in case of an ionizing particle strike [8, 15]. Thus, BBICS enable the detection of transient faults that might lead to soft errors. Amongst the several BBICS architectures, the modular BBICS (mBBICS) represents a promising trade-off between response time, robustness and costs in terms of area [9].

The mBBICS consists of two functional blocks: the head and the tail (see Fig. 1). The head circuits are connected to the bulk of the monitored transistors (BUT in Fig. 1) while the outputs of several heads are latched by the tail circuit. NMOS devices are monitored by the NMOS type mBBICS, while the bulks of the PMOS counterparts are connected to the PMOS type mBBICS

Considering the NMOS version of the mBBICS, the gate of transistor Nh1 is connected to VDD and its drain to the bulk of the monitored transistors (see Fig. 1). In normal operation, the drain of Nh1 acts as a virtual GND while the signal $head_{NMOS}$ is at V_{DD} level. In case of a particle strike, the fault current is conducted through Nh1 resulting in a voltage drop over Nh1 which increases the gate-source voltage of Nh2. If this voltage exceeds the threshold voltage $v_{th,Nh2}$ of Nh2 the signal $head_{NMOS}$ is pull-down. Consequently, the connected tail circuit latches this signal and triggers the error flag. The circuit remains in this state until the reset transistor Pt3 is activated, causing the circuit to returning to its initial state [9].

The processing of a detection of a particle strike is realized on higher processing layers and not considered in this work. Further information can be found in [16-18].

III. Flow for BBICS Insertion

This section presents the proposed flow for automatic insertion of BBICS in a random design.

A. Flow

The proposed flow applies the modular BBICS presented in section II [9]. It should be noted, though, that the flow can be adapted with low effort for any other BBICS architecture. The purposed flow is also resilient to changes in the netlist during the place and route phase, since it uses relative cell position.

Each mBBICS head monitors a certain amount of transistors. These transistors can be placed in different or same N- or P-wells. However, devices that are monitored by different sensors must be placed in different wells. In this case, wells have to be separated by a minimum distance, which easily can be as wide as a standard cell [19]. Consequently, it is desired to place all standard cells, whose transistors are monitored by the same mBBICS, in the same N- or P-well.

The insertion of mBBICS heads and tails on logic level is not recommended as there is still no information about the design layout available. Thus, we propose to include the mBBICS only after initial placement. This solution permits less control over which cells are monitored with same mBBICS, but it considerably reduces the area penalty.

Fig. 2 depicts the simplified version of the proposed flow for mBBICS insertion. After initial synthesis and floorplanning, the standard cells are placed by an automatic placement tool. During the next step, the cells of each row are clustered to be monitored by same heads. Then, cells are shifted in order to create space, the wells are separated, and NMOS and PMOS type heads are added to the row. In the final steps, tail circuits are added at the end and beginning of each row and the routing is executed by an automatic tool.

B. Clustering and head insertion strategies

The amount of transistors an mBBICS head can monitor is limited by the capacitive load due to the bulks of the monitored devices [20-22]. If this load is higher than the sensor's capability, the sensibility of the mBBICS will not be sufficient to detect all particle strikes that can lead to a soft error.

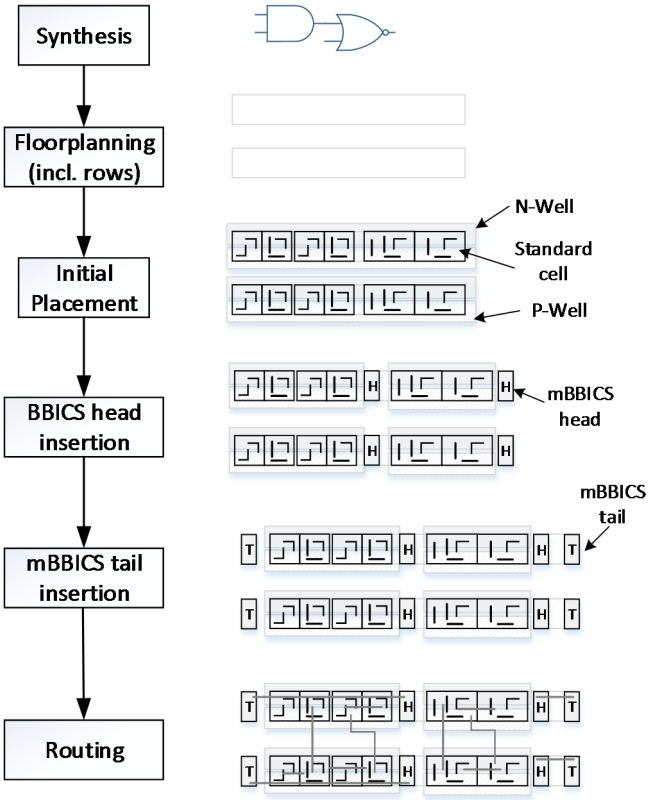

Fig. 2. Proposed flow for mBBICS insertion (simplified)

Hence, we propose to define for each cell *i* the two weight values $\gamma_n(i)$ and $\gamma_p(i)$, which are related to the bulk capacitances of its NMOS and PMOS devices. During clustering, the total weights $\gamma_{cl,n}$ and $\gamma_{cl,p}$ of the cluster are incremented when a standard cell is added to the cluster. Further, for both mBBICS head types are estimated the maximum capacitive loads $\beta_{max,n}$ and $\beta_{max,p}$ for which they have still sufficient sensibility.

The proposed methodology offers two kinds of mBBICS head cells, which are detailed in the following.

1) Double head

A *Double head* mBBICS cell consists of a NMOS and a PMOS type head. The resulting insertion algorithm is listed in Fig. 3. The processing of each row of the design starts with the initialization of the cluster weights (line 3). Next, cells are added successively to the cluster starting from left side (lines 5 and 6). This is done until the value of at least one of the total cluster weights $\gamma_{cl,n}$ and $\gamma_{cl,p}$ would cross the corresponding maximum capacitive load (line 7). Then, a *Doubled head* is inserted (line 10) and a new cluster is formed (lines 8 and 9). In case of an insertion in the layout, the current row is extended and all right-hand cells are shifted rightwards by the width of the *Doubled head*, which is then added. It should be noted that a *Doubled head* realizes the separation of the wells. Further, the netlist is updated in order to enable the later routing of the mBBICS head cell.

2) Single head

The disadvantage of the *Double head* cells is its incapability to handle unbalanced cell weights, *i.e.*, clusters in which $\gamma_{cl,n}$ and $\gamma_{cl,p}$ strongly differ. In these cases, one of the mBBICS heads in the *Double head* cell monitors less devices than it could. Hence, we propose the additional use of *Single head* cells, which consist of a single NMOS or PMOS type mBBICS head.

The modified algorithm is listed in Fig. 4. Similar to the previous algorithm it starts with an initialization of the cluster weights (line 3). This is followed again by successive addition of cells to the cluster (lines 5 and 6). In contrast to the algorithm presented in Fig. 3, a *Double head* is only inserted if at least one of the cluster weights is higher than the corresponding maximum load, while the opposite cluster weights crosses a predefined fraction α of the corresponding

```
 1:  Do for all rows {
 2:    Get n, row[1], …, row[n]  // array with all cells of the row
 3:    γcl,n = γcl,p = 0
 4:    Do for i = 1 to n {
 5:      γcl,n = γcl,n + γn(row[i])
 6:      γcl,p = γcl,p + γp(row[i])
 7:      if (γcl,n > βmax,n) or (γcl,p > βmax,p) {
 8:        γcl,n = γn(row[i])
 9:        γcl,p = γp(row[i])
10:        insert Double head before row[i]
11:      }
12:    }
13:    Insert Double head
14:  }
15:  End
```

Fig. 3. Algorithm for insertion of mBBICS *Double head* cells

```
 1:  Do for all rows {
 2:    Get n, row[1], …, row[n]   // array with all cells of the row
 3:    γcl,n = γcl,p = 0
 4:    Do for i = 1 to n {
 5:      γcl,n = γcl,n + γn(row[i])
 6:      γcl,p = γcl,p + γp(row[i])
 7:      // 0 ≤ α ≤ 1
 8:      if [(γcl,n > βmax,n) and (γcl,p > α *βmax,p)]
           or [(γcl,n > α * βmax,n) and (γcl,p > βmax,p)] {
 9:        γcl,n = γn(row[i])
10:        γcl,p = γp(row[i])
11:        insert Double head before row[i]
12:      } else if (γcl,n > βmax,n) {
13:        γcl,n = γn(row[i])
14:        insert Single head NMOS before row[i]
15:      } else if (γcl,p > βmax,p) {
16:        γcl,p = γp(row[i])
17:        insert Single head PMOS before row[i]
18:      }
19:    }
20:    Insert Double head
21:  }
22:  End
```

Fig. 4. Algorithm for insertion of mBBICS *Double* and *Single head* cells

maximum load (line 8). The value of α should be determined in empiric studies.

If only one of the cluster weights reaches the maximum load while the opposite weight is lower than the predefined fraction, a corresponding *Single head* is inserted (lines 14 and 17) and only the related cluster is reformed (lines 13 and 16). The addition of a *Single head* is realized in the same way as for the *Double head* described above.

C. Final Steps

After the head cells have been inserted in all rows, tail cells are added. Thereby, PMOS type tail cells are added on the right side of a row and NMOS type ones on the left side. The number of tail cells in each row depends on the amount of heads each mBBICS tail can monitor [9]. However, each row has at least one tail of each type. Additionally, the netlist of the design is updated.

Finally, the whole design is routed by an automatic routing tool. Thereby, also the bulk connections of each standard cell are routed with its corresponding head cell.

IV. Cell Implementation

This section presents the applied technology and the implemented cells.

A. Technology

All designs have been realized in a commercial 180 nm technology with Triple-well option. The nominal voltage is 1.8 V, the minimum transistor length is 180 nm and the minimum width is 220 nm.

B. Standard cells

The BBICS approach requires that all monitored transistors are located in a P- or N-well. Hence, it was necessary to create

a standard cell library that complies with this requirement. Fig. 5 depicts the layout of a NAND2 and an INV standard cell which are realized in a Triple-well process. The standard cell height was defined with 16.5 µm.

As can be identified in Fig. 5, the Triple-well structure of the NMOS devices as well as the N-well of the PMOS devices are not closed within the cell. Hence, this closing has to be realized by filler cells or mBBICS head cells. Further, the bulk contacts are pins that can be connected during the routing process.

All cells have been characterized by the tool Synopsys SiliconSmart [23].

C. Layout of mBBICS head cells

This subsection presents the layouts of the head cells of the mBBICS.

1) Double head

The *Double Head*, introduced in section III, contains both PMOS and NMOS heads in the very same cell. Fig. 5 depicts the layout of this cell. The size of the cell is dominated by the required minimum distances between wells of same ($MinD_{eq}$) and different potential ($MinD_{dif}$). Further, its NMOS devices are not realized in Triple-well. The connections (pink wires) between the input pins $bulk_{NMOS}$ and $bulk_{PMOS}$ and the corresponding bulk connections of the monitored cells NAND2 and INV had been added only during routing. The width of the cell is 12.6 µm.

As mentioned in the previous subsection, the *Double head* also contains structures to close the N-wells and Triple-wells of the neighbor standard cells (see left and right corners of the *Double head* cell in Fig. 5).

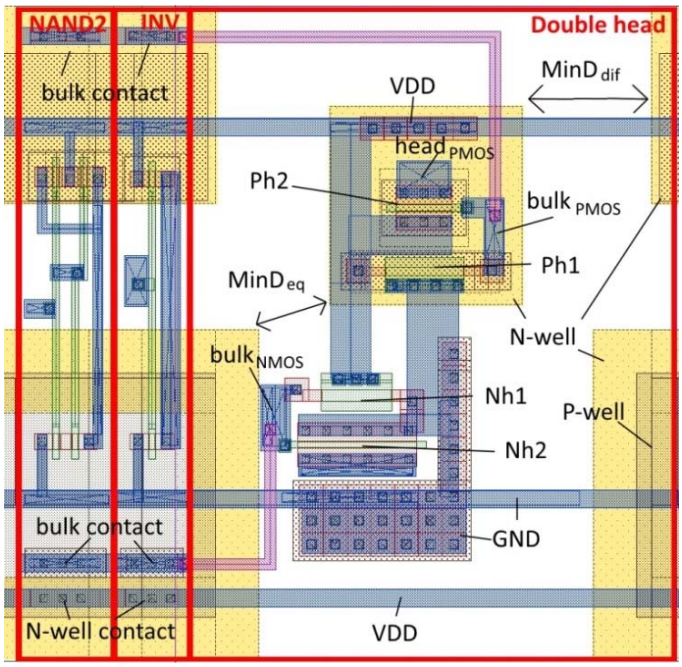

Fig. 5. Layout of *Double head* cell and NAND2 and INV standard cells. The bulk connections (pink wires) had been added during routing. $MinD_{dif}$ and $MinD_{eq}$ indicate minimum distances between wells with same and different potential.

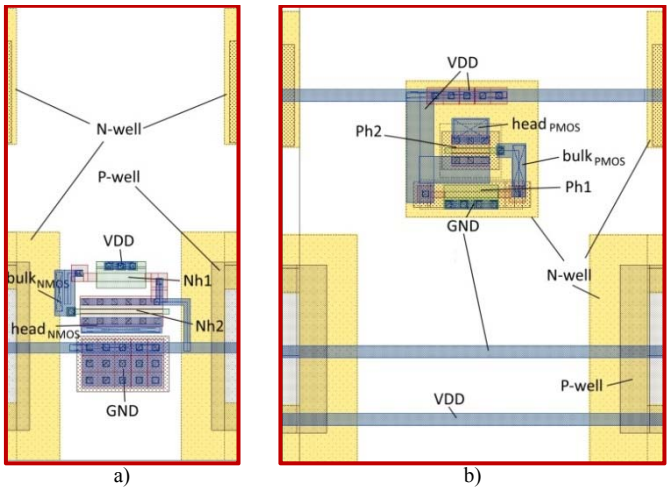

Fig. 6. Layout of a) NMOS *Single head* cell, b) PMOS *Single head* cell

2) Single head

Fig. 6 depicts the NMOS and PMOS *Single head* cells. The width of the NMOS version is 8.2 µm, while its PMOS counterpart has the same width as a Double head, *i.e.*, 12.6 µm. This difference in size follows from the required minimum distances of N-wells with same and different potential, as mentioned in the previous subsection. Given that the NMOS head applies no PMOS devices and no Triple-well, it can be realized with smaller area.

Further, both cells contain again structures to close the N-wells and Triple-wells of neighbor cells.

D. mBBICS Sensibility estimation

The sensibility of the BBICS was estimated by using inverters. Initially, a chain of two inverters was created and a double exponential current pulse with t_r = 1ps and t_f = 20 ps (see equation 1) was added to the drain of the 1st inverter in order to simulate the effects of a particle strike. Next, the value for the collected charge Q_{coll} was increased until an error occurred at the output of the 2nd inverter. Thus, the critical collected charge for particle strikes in NMOS and PMOS devices could be determined.

In the following step, the NMOS and PMOS mBBICS cells were connected with the bulks of the corresponding inverter's transistor and the estimated values for the critical charge were applied. Then, the amount of monitored inverters was increased in order to determine the maximum amount of device and thus, the maximum capacitive load the mBBICS can monitor.

The weight of each standard cell (see also section III) was directly related to the gate-bulk capacitances of its devices.

V. Analysis

This section presents and discusses the results for the exploration of the proposed flow.

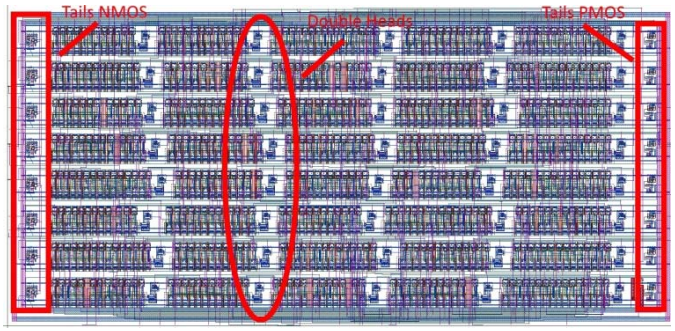

Fig. 7. Exemplary layout of the circuit c499 with *Double head* mBBICS

A. Environment

Automatic placing and routing was realized by the tool Cadence Encounter [24]. All scripts have been implemented in TCL. The designs are taken from the ISCAS benchmark suite [25] and were verified after application of the proposed flow. Fig. 7 depicts an exemplary result for the circuit c499 with inserted *Double head* and tail mBBICS cells.

B. Comparison of head insertion strategies

In a first attempt, the application of solely *Double heads* and mixed *Single* and *Double heads* was compared. Therefore, the maximum load was set to β_{max} = 40 minimum sized transistors for both mBBICS types and a layout aspect ratio of AR = 0.5 was chosen. During this analysis, the algorithm for mixed application of *Single* and *Double heads* was applied, whereas α varied between 0 and 1 (see algorithm in Fig. 4). It should be noted that the results for α = 0 are identical to an application of solely *Double heads*.

The results shown in Fig. 8 indicate that the area offset improves for decreasing α, with achieving lowest offset for α < 0.8. Further, for α values below 0.8 only *Double head* cells have been applied. This can be explained by the rather balanced NMOS and PMOS weights of the applied standard cells. Consequently, the number of required mBBICS for NMOS and PMOS devices is very uniform in each row. Thus, there is no gain in using cells with only one head. It should be noted, that these results might differ for other standard cell libraries.

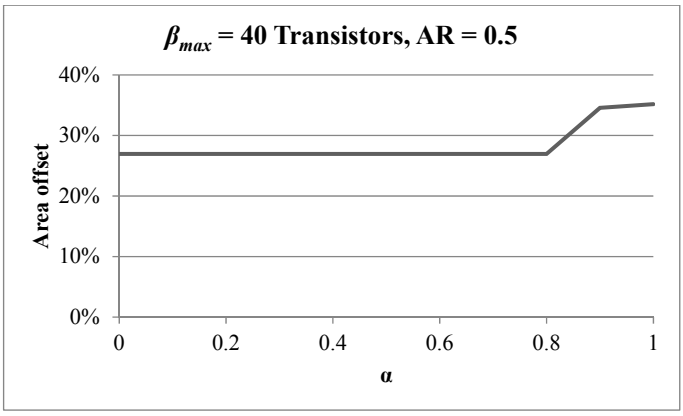

Fig. 8. Average increase of area for varying α, max. load of β_{max} = 40 (in terms of min. sized transistors), layout aspect ratio AR = 0.5 and mixed application of *Single* and *Double heads*.

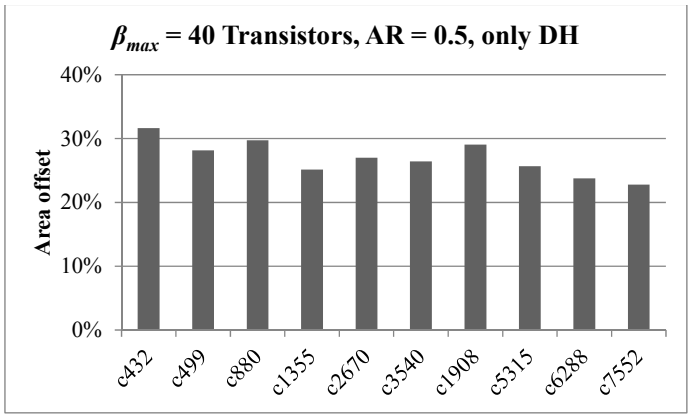

Fig. 9. Area increase for layout aspect ratio AR = 0.5, solely application of *Double heads*, and max. load β_{max} of 40 min. sized transistors.

Following from the observed results, all further experiments were based on the solely application of *Double head* cells.

C. Impact of design

In the following analysis, the variation of the area offset for different designs was compared. The aspect ratio was set to AR = 0.5, β_{max} was defined with 40 minimum transistors, and only *Double heads* were inserted. The results are shown in Fig. 9.

The average area increase is 26.9 %, while the results vary between 22.8 % (c7552) and 31.7 % (c432). It follows that, as expected, the design has average impact on the area offset.

D. Maximum load

The next analysis focused on the reduction of the area offset if the maximum load of the mBBICS could be improved. The results might indicate guidelines for further optimizations of the mBBICS.

Fig. 10 shows that the area offset saturates for maximum

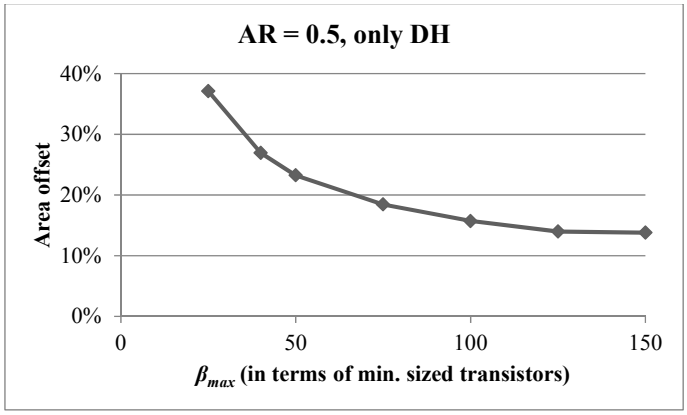

Fig. 10. Average increase of area for aspect ratio AR = 0.5, solely application of *Double heads*, and varying max. load β_{max} of the mBBICS heads.

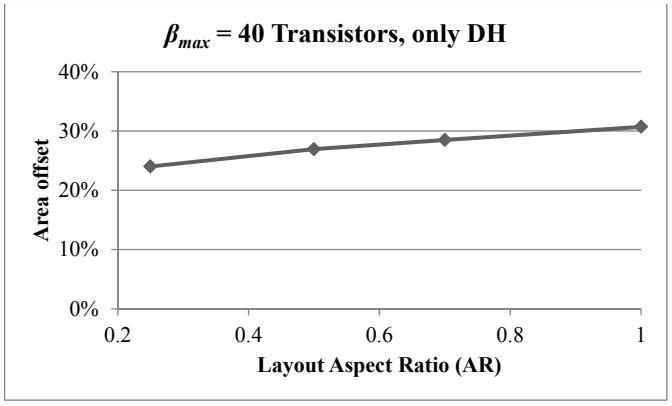

Fig. 11. Average increase of area for different Aspect Ratio (AR) with max. load of β_{max} = 40 (in terms of min. sized transistors) and only DH cells.

loads above 100 minimum sized transistors at around 13 %. This is expected as each row applies at least 2 tail circuits, resulting in a minimum area offset. Even though the minimal achievable area offset differs amongst the designs, *e.g.* 9.0 % for c6288 and 18.7 % for c432, the observed tendency is the same for all analyzed circuits.

Hence, it is recommended to develop mBBICS that can monitor at least 100 minimum sized transistors.

E. Aspect Ratio

The final analysis concentrated on the impact of the aspect ratio on the results. Therefore, each design was implemented with solely *Double head* mBBICS and a maximum load of β_{max} = 40 minimum sized transistors.

The results depicted in Fig. 11 show that the area offset varied from 24.0 % for AR = 0.25 to 30.7 % for AR = 1. Thus, there is only a low impact of the AR value on the results.

VI. CONCLUSION

Radiation-induced soft errors are a rising concern in designs realized in current nanometer CMOS technologies. mBBICS are a promising approach to circumvent these problems. This work proposes a flow that enables the automatic integration of the sensors into common designs, which is a mandatory step towards the application of this approach. It could be shown, that it is recommendable to use of cells that combine NMOS and PMOS head sensors. Further results indicate that mBBICS heads should be able to monitor at least 100 min. sized inverters in order to achieve an area increase of 13 % or lower.

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