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Enhancement of System-Lifetime by Alternating Module Activation

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Focus / Main ideas

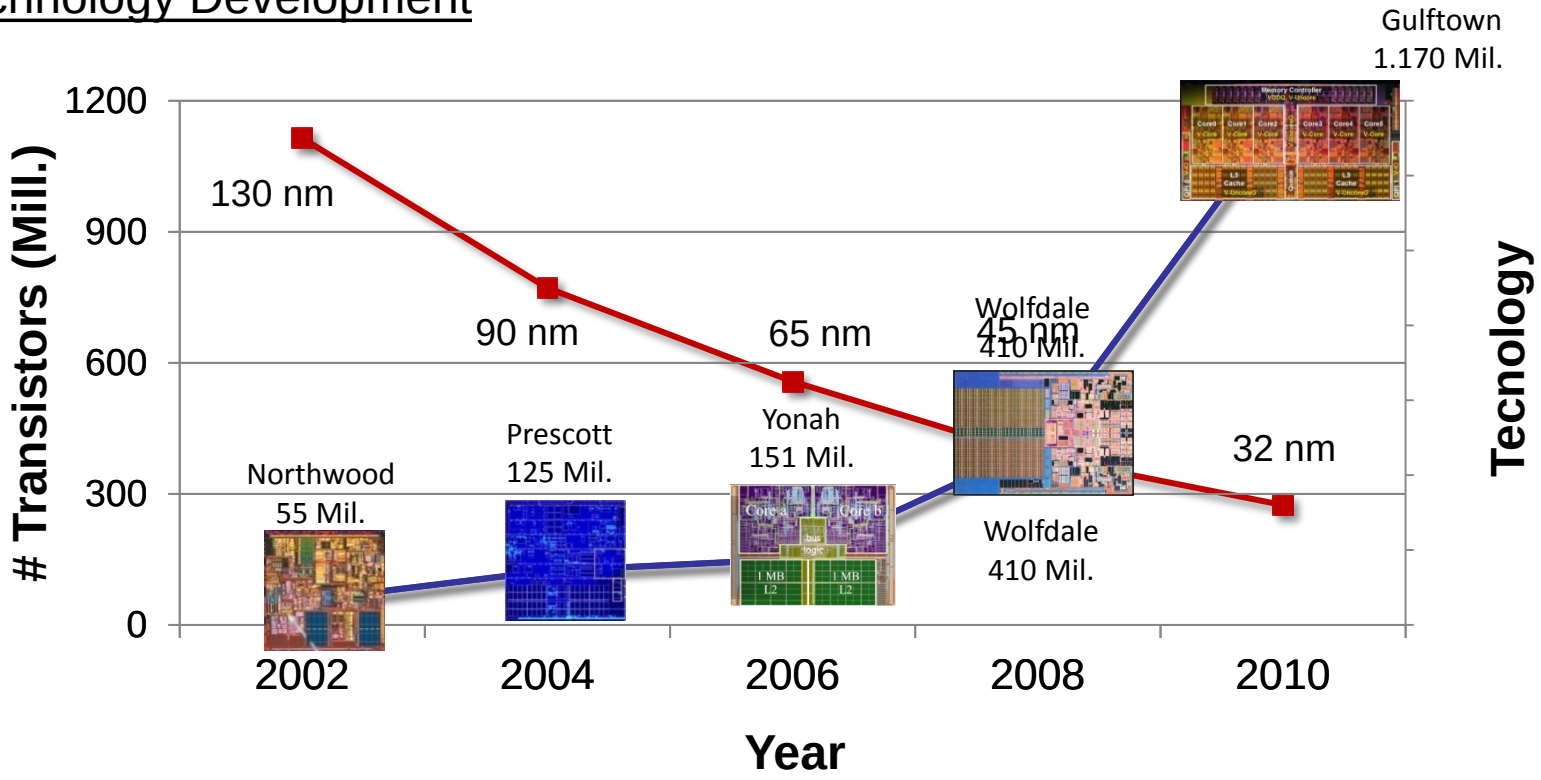
1. Approach aiming at extension of expected lifetime
2. Enabling of detection of faulty design blocks

Outline

- Motivation
- Alternating Module Activation
- **Extended** Alternating Module Activation
- Results
- Conclusion

Motivation

Technology Development



Probability for failures increases due to:

- Increasing transistor count
- Shrinking technology

Motivation

Time Dependent Failure Mechanisms

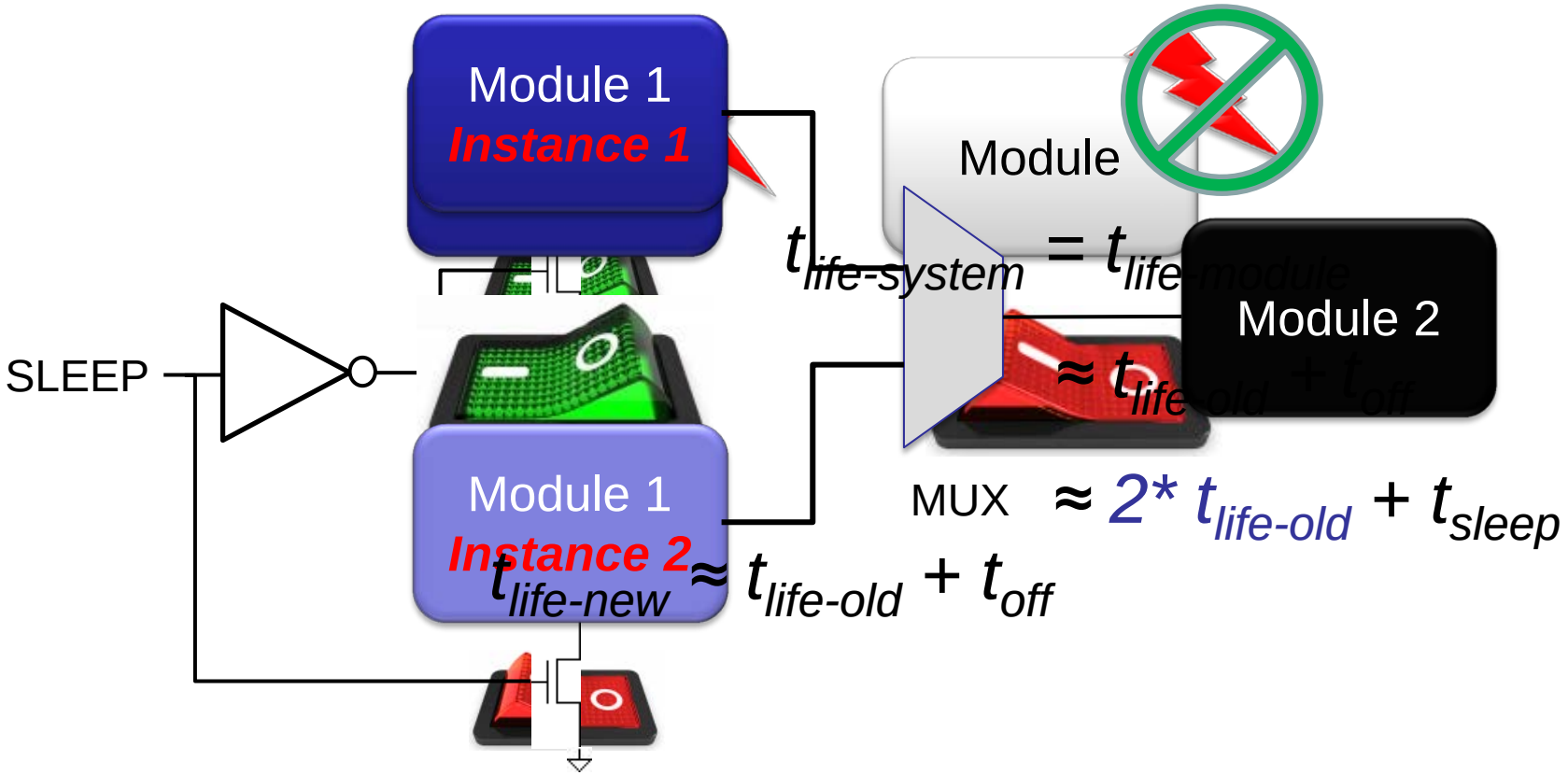
- Electromigration (EM)
  - Performance reduction and errors
  - Depending on **currents** and **temperature**
- Negative Bias Temperature Instability (NBTI)
  - Performance reduction
  - Depending on **voltage level** and **temperature**
- Time Dependent Dielectric Breakdown (TDDB)
  - Performance reduction and errors
  - Depending on **voltage level** and **temperature**

→ Increase of lifetime through reduction of supply voltage and activity

Alternating Module Activation

Concept and Realization

- Basic idea: Reduction of degradation via module **deactivation**
- Problem: What to do at **run-time**?



Alternating Module Activation

Previous Results (*Cornelius, Sill Torres;JOLPE;2011*)

- Test Environment
  - BPTM 22nm, Monte-Carlo simulations
  - Modeling of TDDB and EM (w/o consideration of temperature)
  - Estimation of expected life time via Mean Time To Failure (MTTF)
- Results
  - **Lifetime** increase by factor **2.2** (*aver.*)
  - **Delay** increase by **7 %** (*aver.*)
  - **Power** increase (dynamic and leakage) by **5 %** (*aver.*)
  - **Area** increase by **110 %** (*aver.*)

Extended Alternating Module Activation

Discussion

Advantages

- Considerably extension of expected lifetime
- Moderate increase of delay and power

Disadvantages

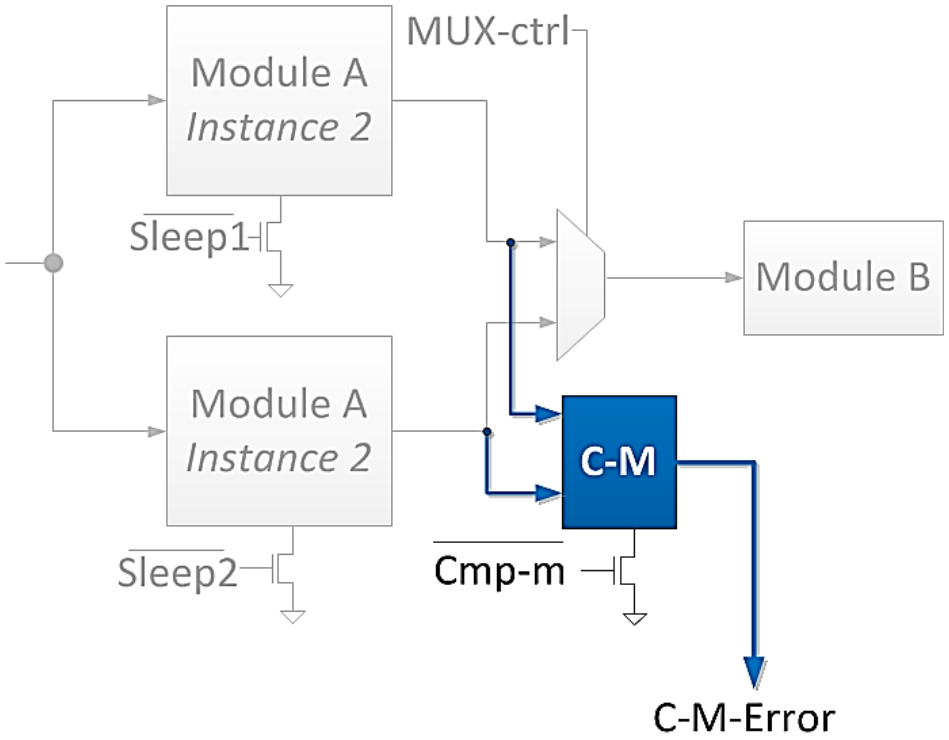
- Strong increase of area
- **No detection of faulty elements**

Proposed Improvements

- Utilization of overlapping activity phases
- Additional comparators and BIST mode
- **Identification and deactivation of faulty elements**

Extended Alternating Module Activation

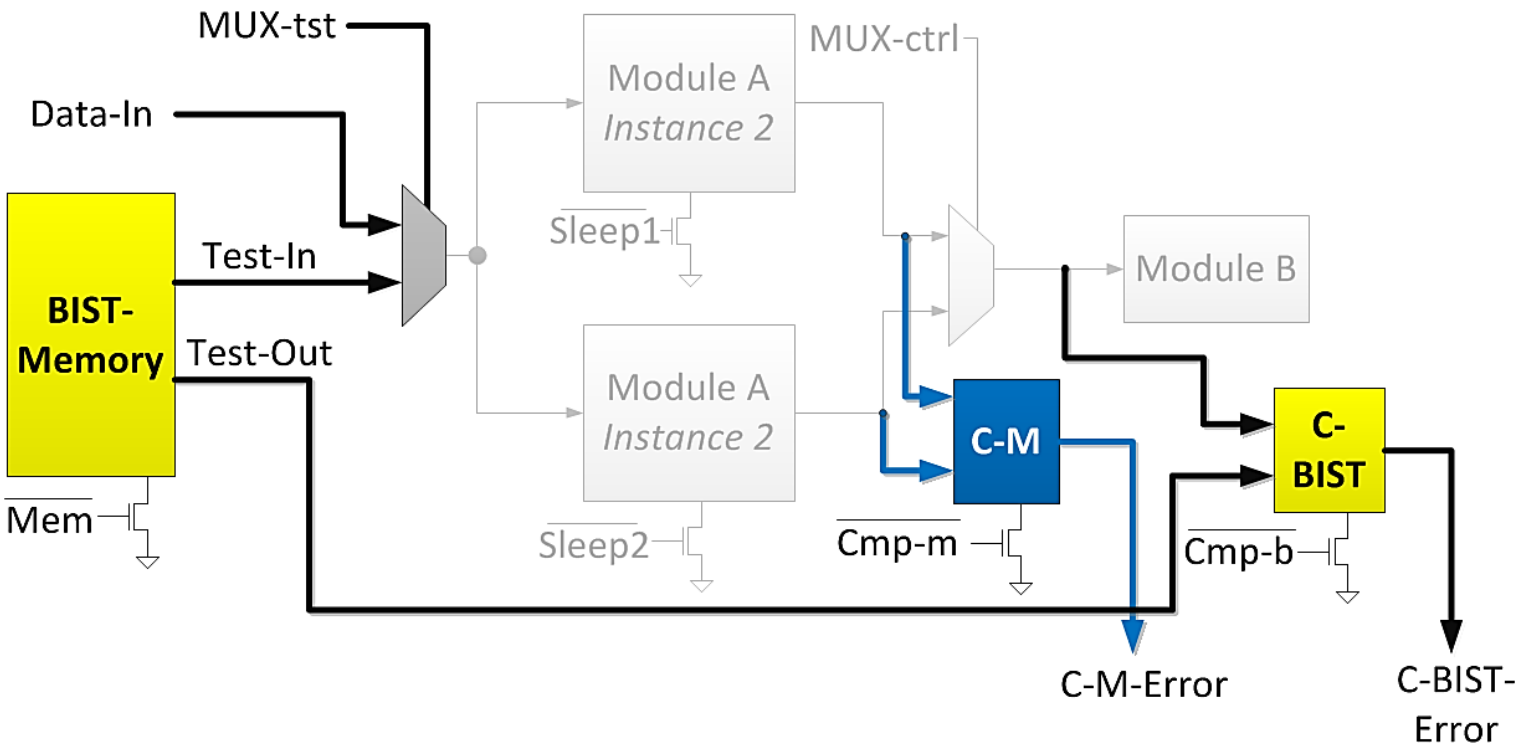
Comparator



- Additional **Comparator** → enabling detection of inconsistent results of all module's instances for same inputs
- Deactivation via Sleep Transistor

Extended Alternating Module Activation

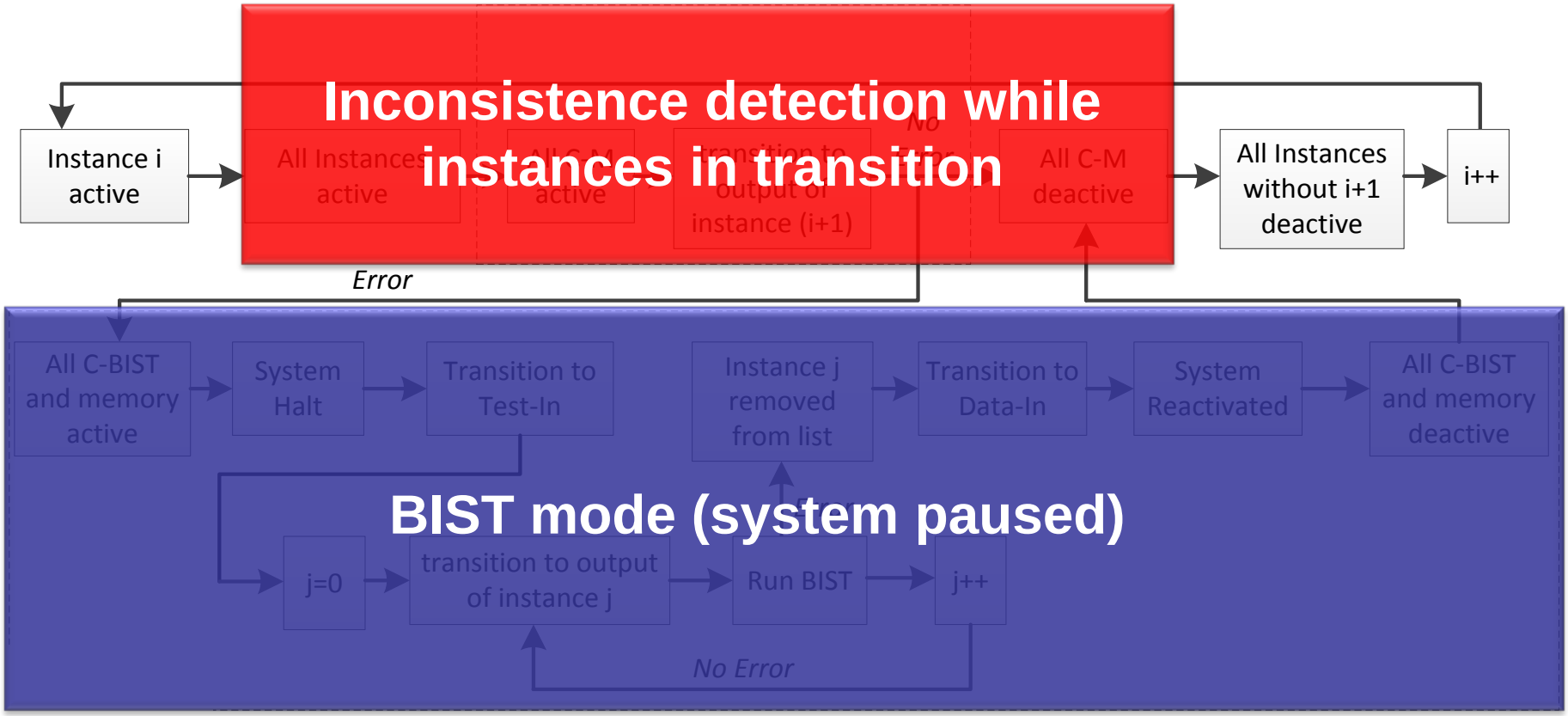
Built-In Self Test (BIST) - Mode



- Additional **BIST Mode** → Enabling identification of faulty instances
- Deactivation via Sleep Transistor

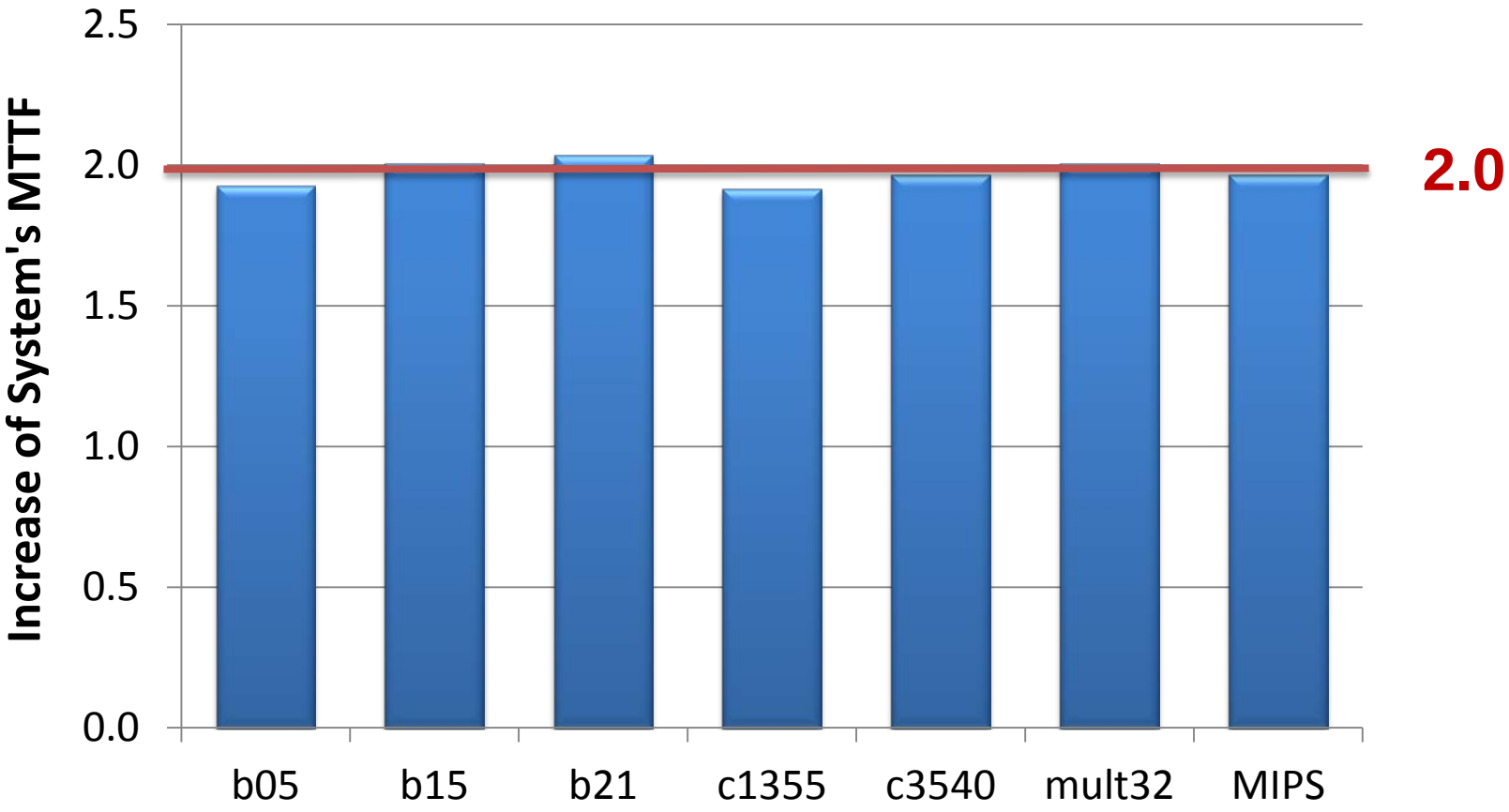
Extended Alternating Module Activation

Control Flow



Results

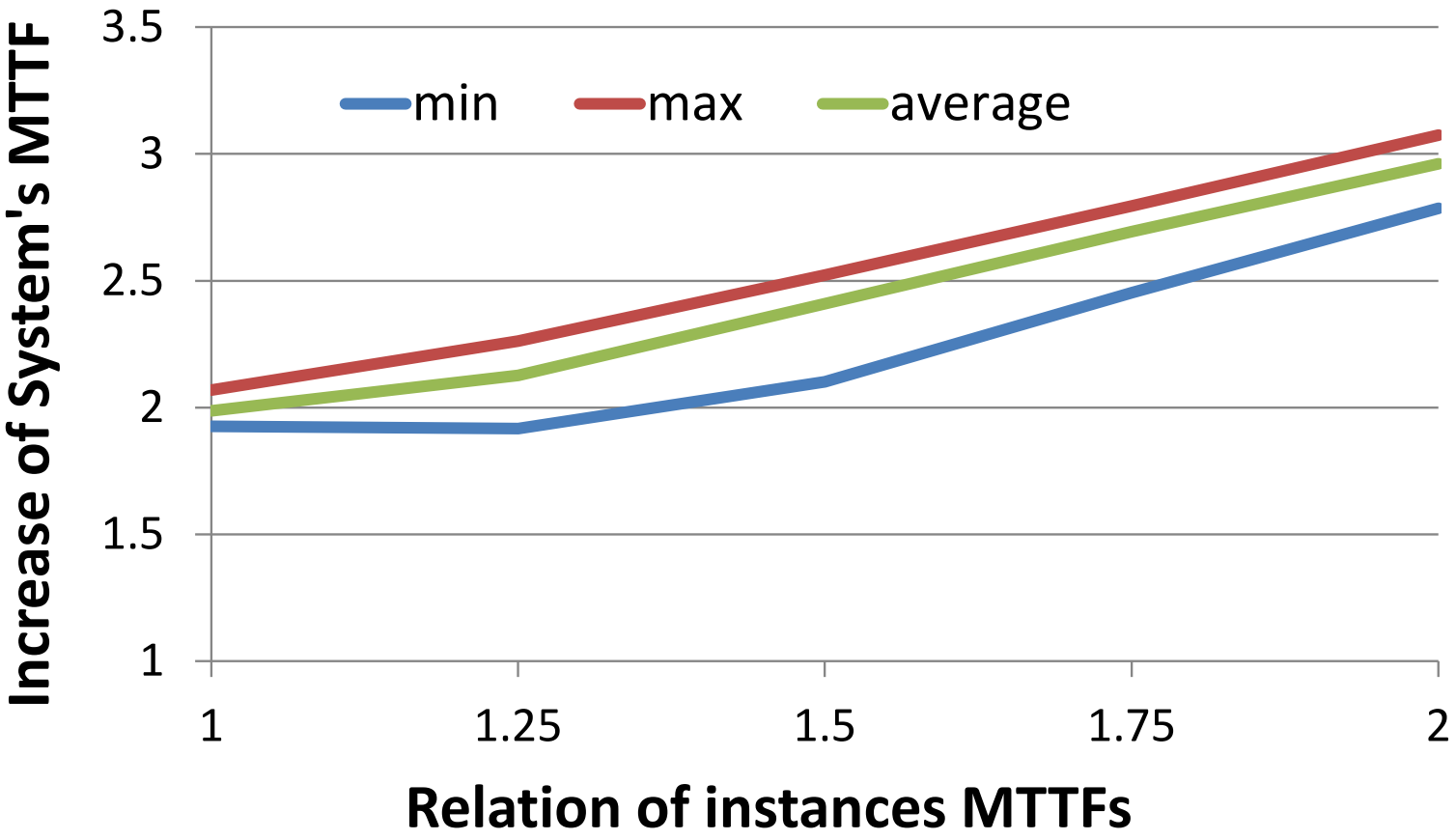
Mean Time To Failure (vs. raw designs)



(Verilog cell models, technology and error data based on BPTM 22nm, 100 simulations, error free control circuitry)

Results

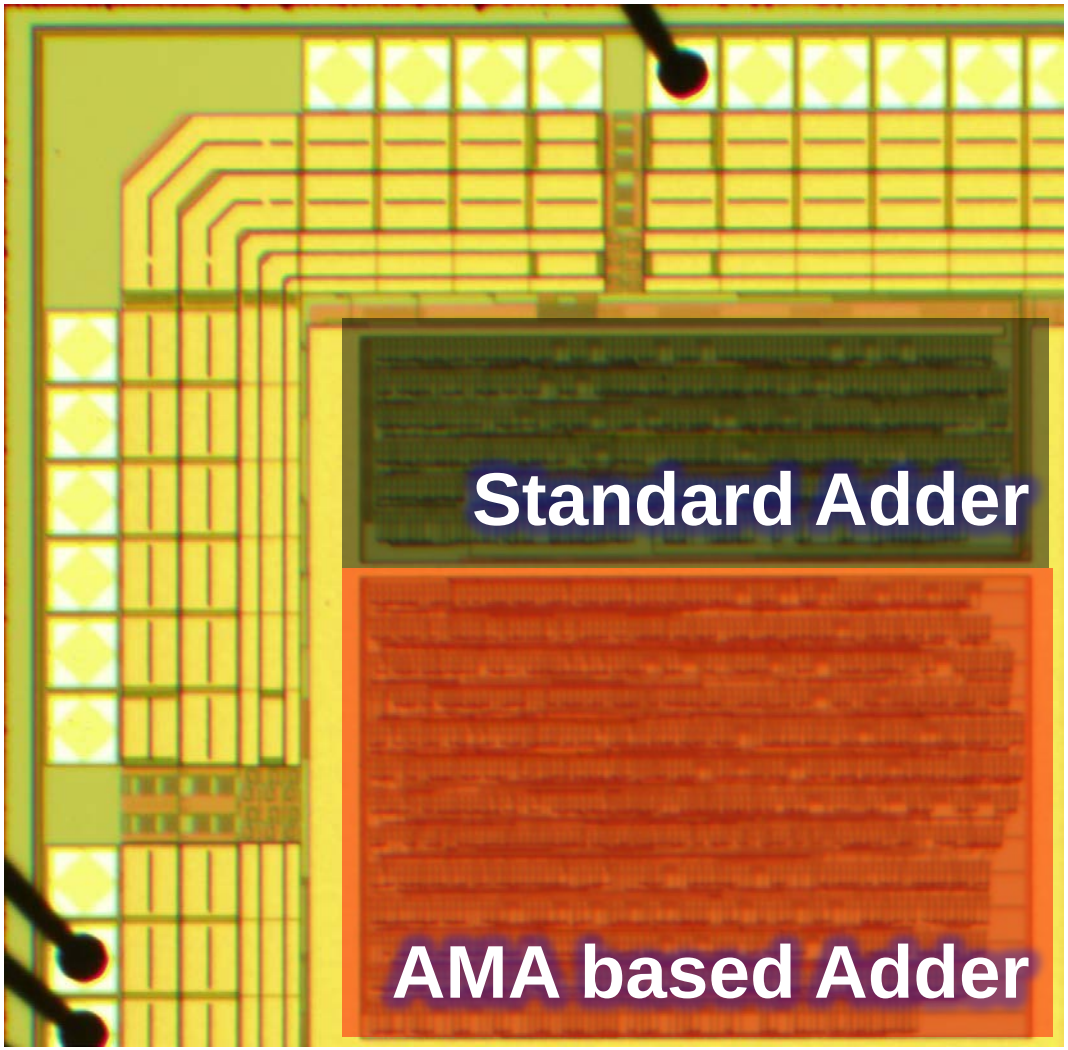
Improvements for Instances with Different MTTFs



(Verilog cell models, data based on BPTM 22nm, 100 simulations, error free control circuitry, 7 standard designs from previous slide)

Results

Test Chip



- CMOS ams c35 (0.35µm)
- Normal Adder
- Redundant Adder based on AMA
- Sleep Transistors
- Prepared for Controlled Destruction
- External Control Circuitry
- In testing phase

Conclusion

- Progressing susceptibility of current technologies against severe failure mechanisms
- Extension of expected lifetime by alternating (de-)activation of redundant blocks via sleep transistors
- **Identification** and **deactivation** of faulty blocks
- Extended **control flow**
- Increase of **MTTF** by
  - **Factor 2** for **equally** distributed failure probabilities
  - More than **factor 3** for **unequally** distributed failure probabilities

Thank you!

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