Parameter Exploration of Carbon Nanotube Field Effect Transistor predictive Technology

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***Abstract* –The definition of parameters of integrated circuit technologies is driven by technological constraints as well as by intended applications. In case of the latter, opposing criterion, like design delay, power consumptions and area, have to be considered. This work presents a figure of merit to be used as an evaluation criterion for the exploration of technology parameter values using a predictive technology based on Carbon nanotubes.**

Keywords- Standard-cell; Carbon nanotubes; Design space exploration; Integrated circuit technology;

INTRODUCTION

Integrated circuit technologies possess a wide range of technology parameters, like transistor channel length, doping profiles, or thickness of gate oxide. These parameters are untouchable by the circuit designers, and thus, are the same in all designs based on that technology [1]. Usually, the choice of the technology parameter values is mainly driven by manufacturing constraints, such as limitations of the lithography process or characteristics of applied materials. Another impact comes from intended applications of the technology. For example, a common option of current technologies oriented for consumer applications are devices with high-performance or low-standby-power profile [2]. Thereby, devices differ in its threshold voltage and/or gate oxide thickness.

Standard cell design is an extensively applied methodology for digital circuit design [3]. In order to enable design analysis before fabrication, each standard cell has to be characterized in terms of delay, power consumption, and area. This characterization can be done using previously fabricated cells or be based on precise transistor level simulation. Hence, it also possible to characterize designs that use predictive technologies, as for example done by Qing et al. for a 5 nm FinFET technology [4] and Bobba et al. for a Carbon nanotube technology [5].

This work extends the approach of using standard cells libraries presenting a criterion to guide the exploration of technology parameters values for a CNTFET technology. This methodology uses the standard cell design flow and synthesis-report in order to create an evaluation criterion to analyze the influence of the technology parameters.

PRELIMINARIES

This section introduces the technology applied in this work.

A. *Carbon nanotubes Transitor*

The Carbon nanotubes field-effect transistor (CNTFET) is one of the most promising potential successors of the MOSFET transistor [6]. Its base component, the Carbon nanotube (CNT), is a nanocylinder composed by a sheet of Carbon atoms that possesses excellent electrical, thermal, and mechanical properties. Further, the ultrathin Carbon nanotube body provides a precise electrostatic control of its conductance. This enables the CNTFET to have extraordinary improvements of the intrinsic delay compared to common MOSFET technologies [7].

0 depicts the basic CNTFET structure. Similar to existing MOSFET technology, CNTFET features drain and source semiconductor regions as well as a gate electrode. Drain and source are connected via Carbon nanotubes, which act as a channel whose conductance is controlled by an electrical field applied over gate and substrate.

A significant advantage compared to other novel nanotechnologies is its compatibility to the conventional MOSFET fabrication process [8]. That is, source, drain, and gate region can built by existing manufacturing processes, while only the CNT region requires a Carbon nanotube grow

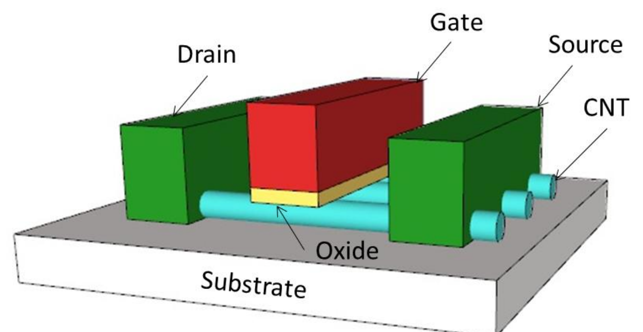

Fig.1. Principal architecture of a Carbon Nanotubes Field-Effect Transistor (CNTFET).

process. Further, the CNTFET technology offers p-type and n-type devices, which permits the utilization of the CMOS approach.

The current principal problem of CNTFET fabrication is the control of the CNTs density and chirality. Variations of the density have considerable impact in the device performance [6]. Further, uncontrolled chirality can lead to metallic CNTs that cause source-drain short circuits and increase greatly the circuit power consumption [8].

Evaluation CRITERION of Technology Parameter values

This section presents a figure of merit for evaluating a set of values of technology parameters. After the design of a standard cell library, its characterization, the evaluation of the technology parameter values is based on synthesis results from representative designs. The fundamental idea is the analysis of how a technology parameter affects the designs in terms of delay, area, and power consumption.

The proposed evaluation criterion is given by the figure of merit F. Thereby, the relative changes of principal design parameters, that is maximum delay t_{delay}, dynamic power consumption P_{dyn}, leakage power consumption P_{leak}, and area A, are weighted. This estimation is done over the sum of all chosen benchmark designs, following equation (1) with φ and γ are the weighting factors defined by the designer. Further, and $P_{dyn,i,init}$, $P_{leak,i,init}$, $t_{delay,i,init}$, and $A_{i,init}$ indicate the default parameter values of each design. It is desired that all principal design parameters decrease. Hence, a reduction of F for the chosen technology parameter values of the set Φ indicates an improvement.

$$F(\Phi) = \varphi_1 \left(\sum_{designs} \frac{P_{dyn,i}(\Phi)}{P_{dyn,i,init}} \right)^{\gamma_1} + \varphi_2 \left(\sum_{designs} \frac{P_{leak,i}(\Phi)}{P_{leak,i,init}} \right)^{\gamma_2} + \varphi_3 \left(\sum_{designs} \frac{t_{delay,i}(\Phi)}{t_{delay,i,init}} \right)^{\gamma_3} + \varphi_4 \left(\sum_{designs} \frac{A_i(\Phi)}{A_{i,init}} \right)^{\gamma_4} \quad (1)$$

IV Simulation Environment

This section presents the simulation environment that enables the verification of the proposed criterion. Further, the parameters of the applied technology are detailed.

B. Characterization

The characterization of each cell can be done by comercial tools like Synopsys SiliconSmart [9] or open-source programs like LIBFILL [10]. Initially, the characterization environment must be configured. This configuration includes the set-up of the ranges for capacitive loads and input signal slews, operating voltages and temperature, logic voltage levels, and the thresholds values for the calculation of cell delay and transition times. Further, convergence parameters as well as cells specific characterization table values must be defined.

The created simulation environment applies the software SiliconSmart. Propagation delays are defined as the time intervals between input and output signals cross 50 % of V_{DD}. The transition times are defined as the time a signal requires to transit from 10 % to 90 % and 90 % to 10 % of V_{DD} for rising and following slopes, respectively. The ranges of the capacitive loads are set to 1X – 30X of the input capacitive load of the minimum inverter of the technology and feature size. The range of the transitions times of the input signal is set to 1X –5X of the FO4 the transition times of a minimum inverter of same technology and feature size.

Technology Model

As stated in the section II, Carbon nanotube transistor (CNTFET) is a promising technology for future integrated circuits. There is still no widely accepted completely analytical spice model, though, as this technology is still under development. Hence, this work applies the semi-empirical Stanford University Virtual Source CNFET VerilogA model that describes the current-voltage and charge-voltage characteristics of a short-channel CNTFET [11]. This model proved to have good accuracy as it considers gate resistance and capacitances, Schottky Barrier Effects, as well as parasitics on the Carbon nanotubes, source and drain [11]. The model is hierarchical and composed by three layers of abstraction.

Table I lists the most relevant parameters and its typical values taken from [4] and [7], separating feature size dependent and independent parameters. The analysis has been executed for the features sizes of 2 nm, named CNTFET22, whose parameters are listed in Table II.

C. Standard cell Library

The applied standard cell library contains a basic set of combinational and sequential cells. Further, all combinational cells are realized with two different sizes. Thereby, the cell sizing is based on the inverter cells, *i.e.* all cells have same driving strength as the inverter with same size.

D. Benchmark Designs

The applied benchmark designs in this work are a mix of combinational designs (c1908, c2670, c3540, c499, c5315, c7552), taken from the ISCAS benchmark suite [15], and sequential designs (b01 and b05) of the ITC99 benchmark suite [16].

Paramter exploration for CNTFET

This section presents the results of the application of the proposed parameter evaluation criterion to guide a parameter exploration for the Carbon nanotube transistor (CNTFET) technology.

SELECTED PARAMETER FOR APPLIED CNTFET TECHNOLOGIES

Feature size dependent		
Parameter	**Description**	**Typical Value**
W_{gate}	Gate width	3a
L_{ch}	Channel length	2a
L_{ss}	Doped CNT source-side extension region length	2a
L_{dd}	Doped CNT drain-side extension region length	2a
N_{tubes}	Number of nanotubes in a device	$(W_{gate}/Pitch)-1$
Feature size independent		
d_{CNT}	Tubes diameter	1.5 nm
Pitch	Distance between the centers of two adjacent CNTs within the same device	4 nm
Distance	Distance between the corners of two adjacent CNTs	2.5 nm
Tubes density	Tubes density in the device	250 CNT/µm
T_{ox}	Thickness of high-k top gate dielectric material	4 nm
L_{geff}	Mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.	200 nm
C_{sub}	Coupling capacitance between channel region and substrate	200 nF
E_{fi}	The Fermi level of the doped S/D nanotube.	0.6 eV

Parameter Selection

According to [8], an increase of the diameter d_{CNT} of the nanotubes within a CNTFET leads to an exponential increase of the OFF current, while the ON current increases linearly. This turns the diameter to a key parameter to balance speed and leakage power consumption. Hence, the proposed approach was applied to explore the impact of this parameter on actual designs in the CNTFET22 technology.

As can be noted in Table I, several geometric parameters of CNTFET impact each other, such as the diameter d_{CNT} and the distance between the nanotubes if a constant metal gate width W_{gate} is assumed.

During parameter exploration, a constant distance of 2.5 nm and a constant W_{gate} of 33 nm have been defined. The initial parameter value for d_{CNT} was set to 2 nm, following recommendations of the literature [5,6], which results in a nanotube amount N_{tube} of 8. Following simulations on inverter,

TABLE II. PARAMETERS FOR CNFET CELLS

	CNTFET22
W_g	33 nm
L_{ch}, L_{ss}, L_{dd}	22 nm
N_{tubes}	7
V_{DD}	0.75 V

NAND2, and FlipFlop cells indicated an adequate range for d_{CNT} of $d_{CNT,min}$ = 1 nm and $d_{CNT,max}$ = 4 nm.

Exploration Flow

The design parameters maximum delay t_{delay}, dynamic power consumption P_{dyn}, and leakage power consumption P_{leak} have been chosen for the exploration of the technology parameter d_{CNT}. The related weighting factors φ and γ have been equalized to 1, with exception of γ_{leak} which was set to 1.5 in order to compensate the exponential relation between P_{leak} and CNT diameter [5, 6].

Based on the parameters defined in the previous subsection, an initial standard cell library was characterized. Next, this library was applied for synthesis and characterization of the benchmark designs. With the initial values for maximum delay, dynamic power consumption, and leakage power consumption at hand, d_{CNT} was increased to d_{CNT} = 3 nm, which resulted in a new nanotube amount of N_{tube} = 5. Subsequently, the process of standard cell library characterization, synthesis, and benchmark design analysis was executed again. Based on the extracted values the merit factor F could be determined using equation (1). The results indicated a deterioration of the technology, as F increased from 32.5 to 103.0. Thus, d_{CNT} and N_{tube} were set to 1.5 nm and 7, respectively. This resulted in a better value for F, which decreased to 20.6. In the next step, d_{CNT} and N_{tube} were set to 1.25 nm and 8, which increased F to 28.4. Thus, the estimated best value for d_{CNT} is 1.5 nm, which complies with values known from the literature [5, 6].

However, it can be concluded that the dynamic power consumption does not change much. This is an expected behavior as the gate width is kept constant.

Fig. 3 illustrates the leakage power dissipation for different diameter of the nanotubes related to the results for d_{CNT} = 2 nm. As can be noted by the logarithmic axis, the leakage power consumption changes very strongly, which is expected as the

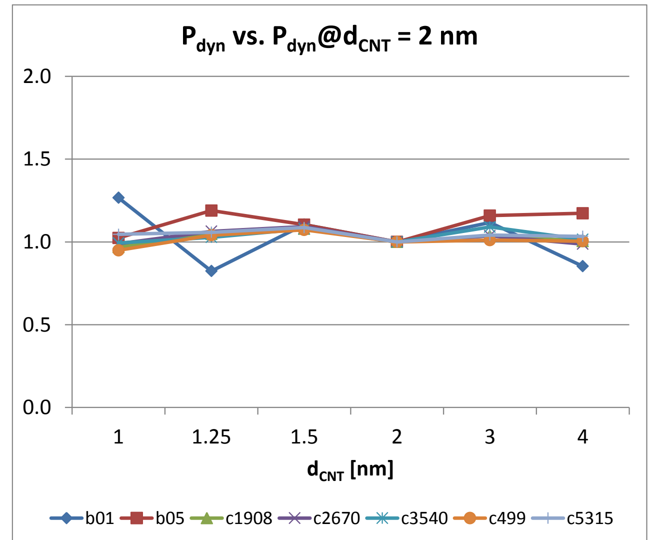

Fig.2. Dynamic power dissipation P_{dyn} for different diameter d_{CNT} of the nanotubes related to the results for d_{CNT} = 2 nm.

relation between P_{leak} and d_{CNT} is known to be exponential [5, 6].

Analysis

In the following, the observed behavior undergoes a detailed analysis. Fig. 4 depicts the maximum design delays for different diameter of the nanotubes related to the results for $d_{CNT} = 2$ nm. It can be noted that the relation of the results amongst combinational (cXXX) and sequential designs (bXX) is very similar. Further, the results indicate that for wider but less nanotubes the t_{delay} is not affected.

Fig. 2 shows the dynamic power dissipation for different diameter of the nanotubes related to the results for $d_{CNT} = 2$ nm. It can be observed that combinational and sequential designs behave slightly different from each other. This is based on the FlipFlops which have high impact on both sequential designs.

CONCLUSION

This work proposed a figure of merit for the evaluation of the impact of technology parameters on actual designs. This considerably supports process engineers in the selection of technology parameters and enables researchers to explore the influence of novel technologies on integrated designs. Further, the application on a predictive Carbon nanotube based technology confirmed the usability of the proposed criterion.

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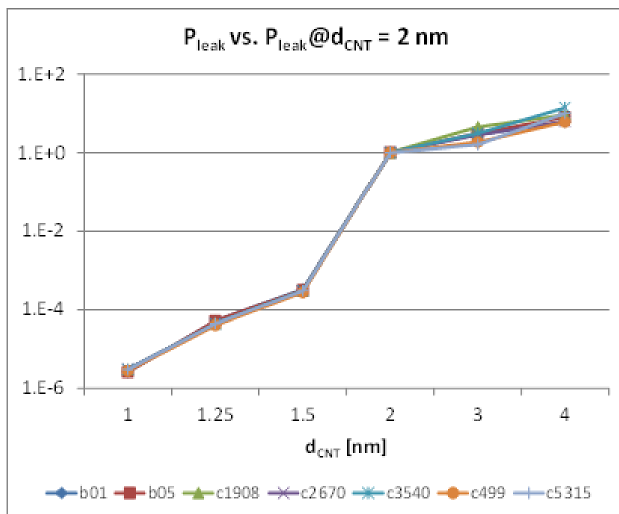

Fig.3. Leakage power dissipation P_{leak} for different diameter d_{CNT} of the nanotubes related to the results for $d_{CNT} = 2$ nm.

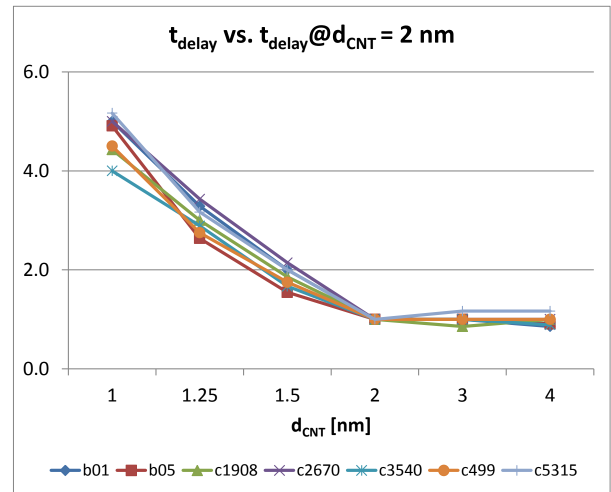

Fig. 4. Maximum design delay t_{delay} for different diameter d_{CNT} of the nanotubes related to the results for $d_{CNT} = 2$ nm.

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