CHIP IN BAHIA 2015

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Exploration of Technology Parameter Values of Integrated Circuits

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Focus / Principal idea:

Technology Parameter Exploration of Integrated Circuits

Standard-Cell Characterization Flow for Novel Technologies

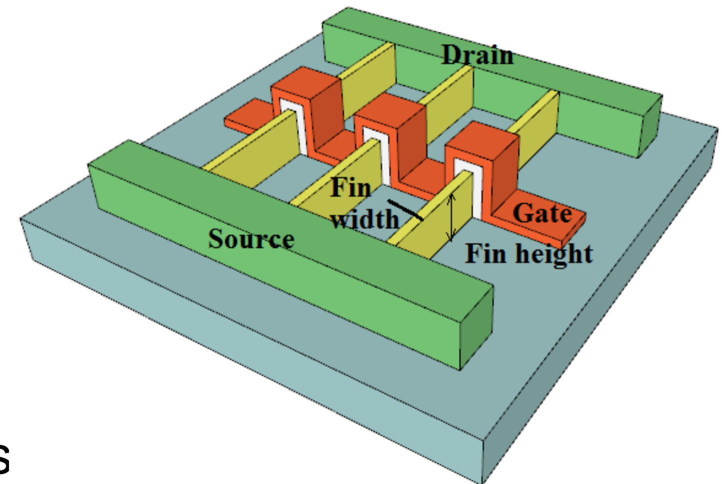
Outline

1. Motivation
2. Methodology
3. Results
4. Conclusion

Motivation

Technology Parameters

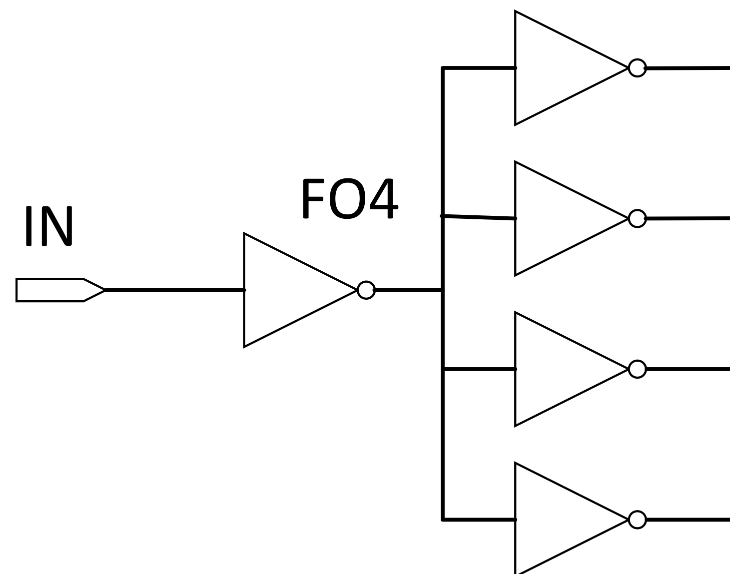
- Integrated circuit technologies offer two kind of parameters:
  - Design parameters (e.g. transistor width, transistor length)
  - Technology parameters (e.g. doping, oxide thickness)
- Design parameters
  - Constrained
  - Modifiable by circuit designers
- Technology parameters:
  - Constrained
  - Not accessible by circuit designers
  - Can be oriented to consumer applications profiles (e.g. High performance / Low-power)



Motivation

Technology Parameter Values

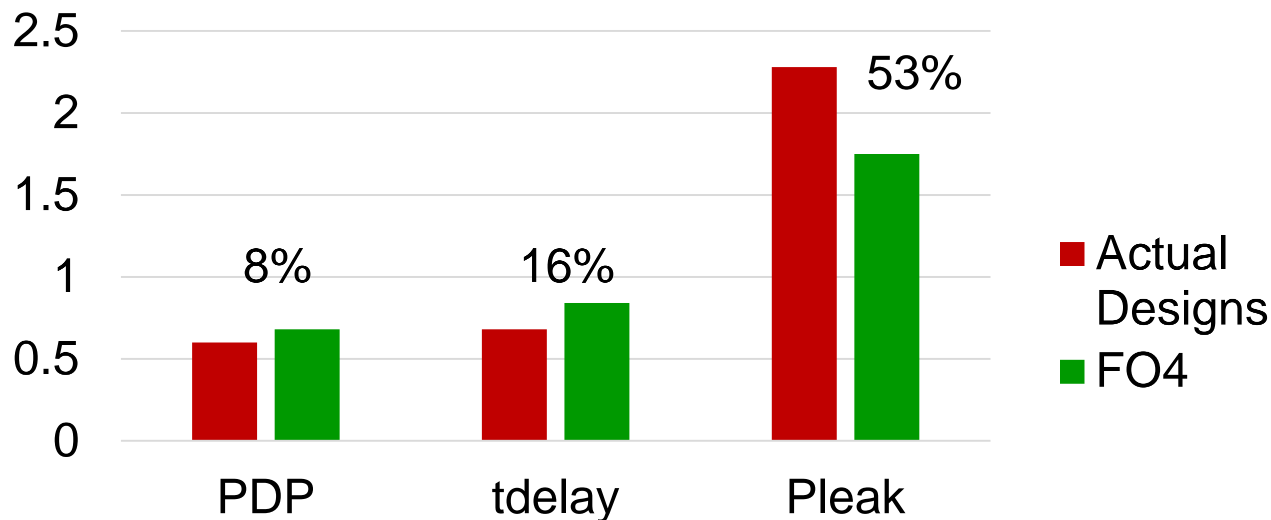
- Question: How to chose values for technology parameters?
- Several constraints: I_{on} vs. I_{off} currents, area, gain, …
- Interesting for:
  - Technology engineers
  - Researchers for novel technologies (CNTFET, SET, …)
- Common approach:
  - Analysis using selected cells (FO4 configuration)
  - Sweep of input parameters (e.g. slope, input value, …)



Motivation

Novel Approach

- Problem: Common solution not accurate enough
- Example: Average CMOS PTM22 gains in relation to CMOS PTM32



- Proposal:
  – Analysis of technology parameter based on actual designs

Methodology

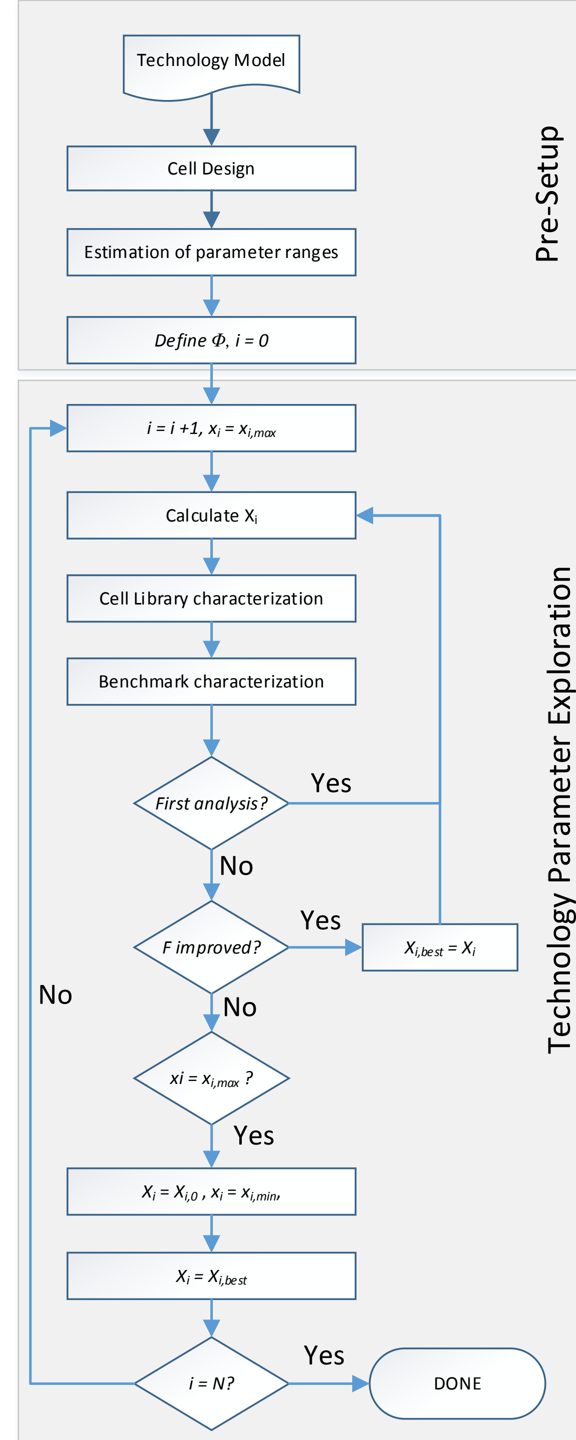
Presentation

- Principal ideas:
  - Analysis of technology parameters impact using characterized standard cell library and test designs
  - Interactive parametric exploration

- Application of comercial tool(s) for standard cell library characterization
- Technology can be given on Spice, Circuit, or Verilog-A level
- Test designs oriented in future application of selected technology

Methodology

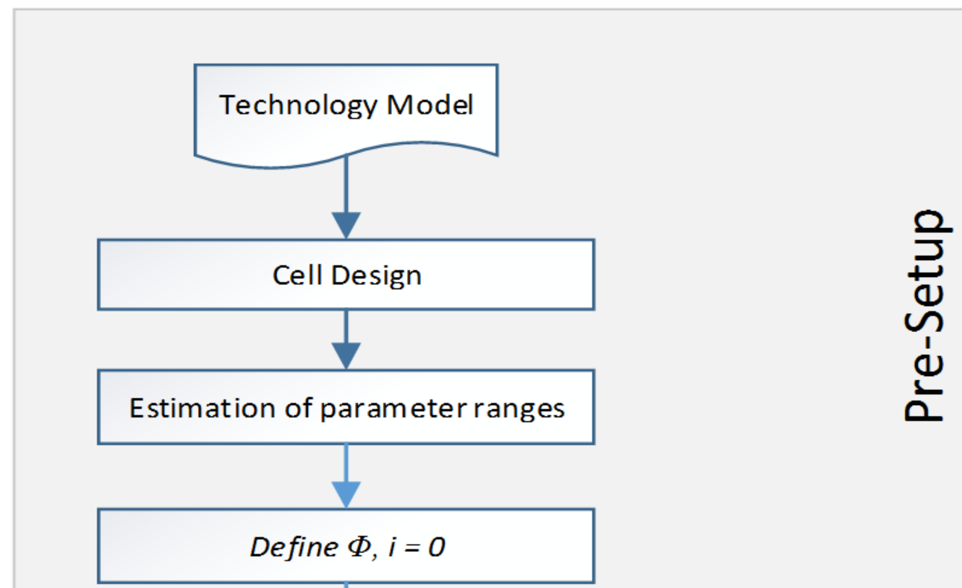
- Two step flow:
  - Pre-Setup
  - Technology Parameter Exploration
- Pre-Setup
  - Environment Setup
  - Standard-cell representation
- Technology parameter Exploration
  - Standard-cell characterization
  - Benchmark and analysis



Methodology

Pre-Setup Stage:

- Design of standard cell library with default parameter values
- Extraction of parameters for look-up tables in characterization flow
- Selection of most important technology parameters and its ranges for exploration

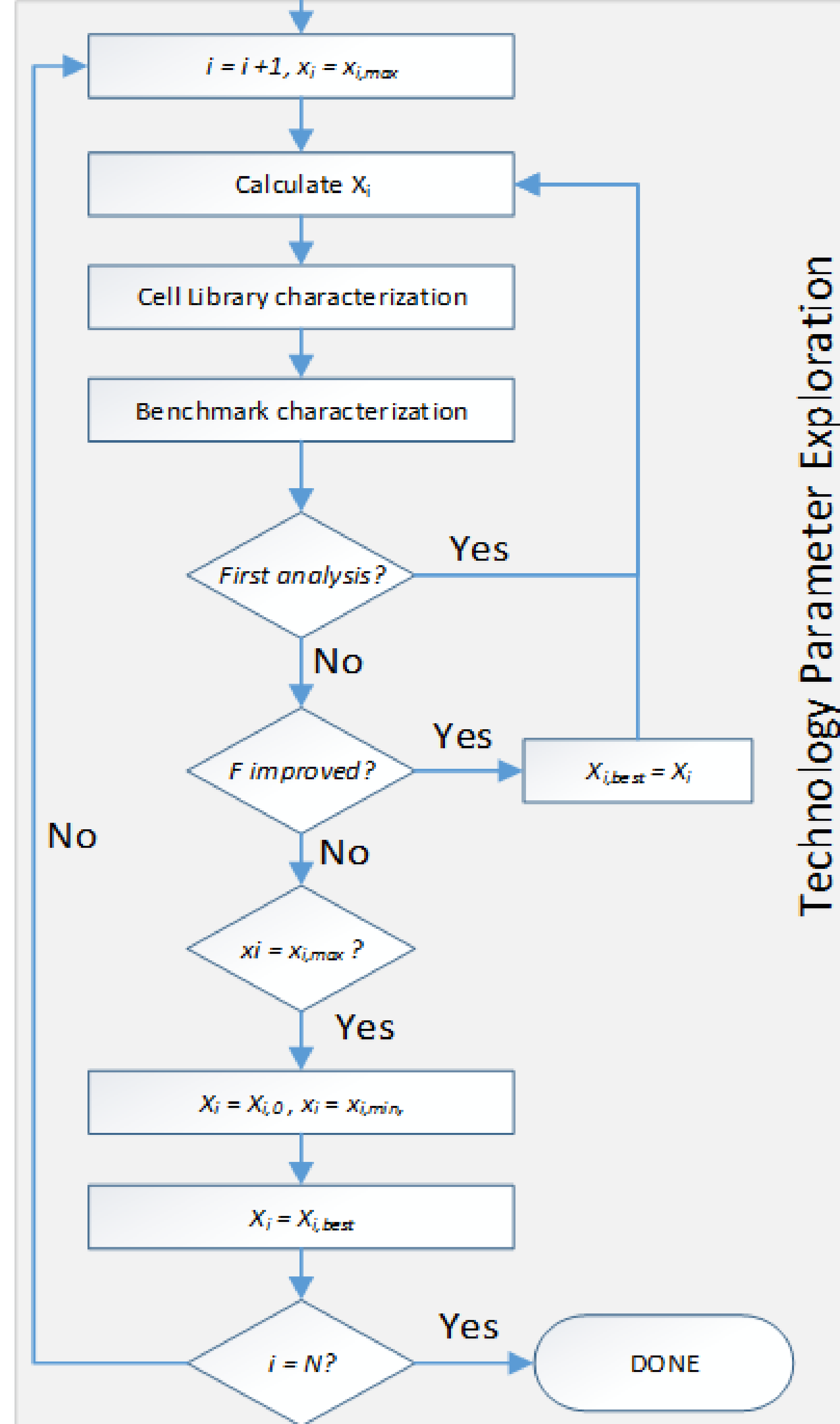


Methodology

Technology Parameter Exploration

- Start parameters with default values
- Perform characterization and benchmark with actual designs
- Figure of Merit evaluation and analysis
- Iterate

$$F(\Phi)=\varphi_1\left(\sum_{designs}\frac{P_{dyn,i}(\Phi)}{P_{dyn,i,init}}\right)^{\gamma_1}+\varphi_2\left(\sum_{designs}\frac{P_{leak,i}(\Phi)}{P_{leak,i,init}}\right)^{\gamma_2}+\varphi_3\left(\sum_{designs}\frac{t_{delay,i}(\Phi)}{t_{delay,i,init}}\right)^{\gamma_3}+\varphi_4\left(\sum_{designs}\frac{A_i(\Phi)}{A_{i,init}}\right)^{\gamma_4}$$



Results

Environment

- Analyzed Technologies:
  - PTM22 and PTM32 (based on Predictive Technology Model - PTM)
  - FINFET10-HP FINFET10LL (based on PTM)
  - CNTFET32 and CNTFET22 (based in Stanford CNFET Model)
- Basic standard cell library (10 cells, different sizes, FlipFlop)
- Test Designs:
  - ISCAS suite: c1908, c2670, c3540, c5315, c7552
  - ITC99 suite: b01, b05
- Tools:
  - Cell library characterization: SiliconSmart (Synopsys)
  - Simulation: Virtuoso Analog Design Environment (Cadence)

Results

Technology Comparison – Delay (t_{delay})

- Versus results for PTM32

t_{delay} vs. t_{delay}@PTM32

1.2
1.0
0.8
0.6
0.4
0.2
0.0

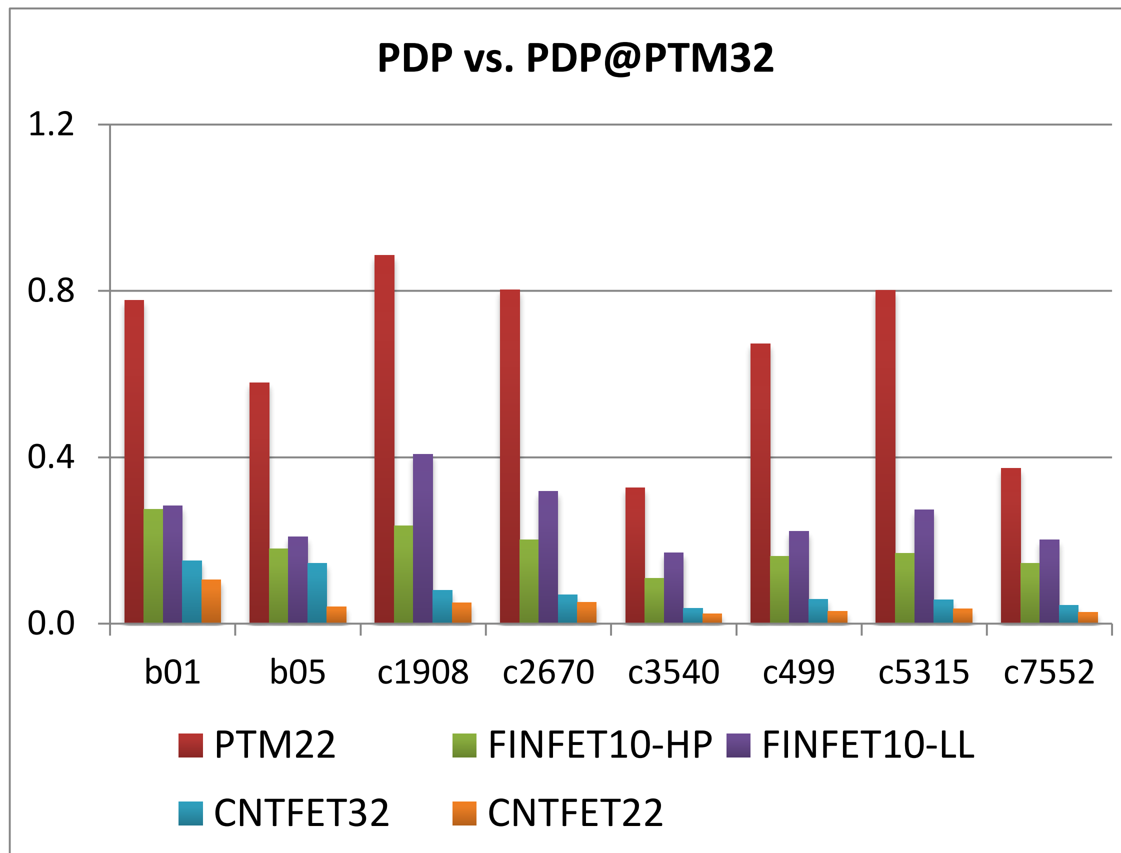
b01 b05 c1908 c2670 c3540 c499 c5315 c7552

PTM22 FINFET10-HP FINFET10-LL CNTFET32 CNTFET22

Results

Technology Comparison - Power Delay Product (PDP)

- Versus results for PTM32



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Results

Technology Comparison – Leakage (P_{leak})

- Versus results for PTM32

P_{leak} vs. P_{leak}@PTM32

5.0
4.0
3.0
2.0
1.0
0.0

b01 b05 c1908 c2670 c3540 c499 c5315 c7552

PTM22 FINFET10-HP FINFET10-LL CNTFET32 CNTFET22

Results

Technology Comparison

- Comparison of relation to PTM32 of FO4 analysis and proposed flow

Comparison FO4 data vs. Flow

60%
40%
20%
0%
-20%
-40%

PDP
tdelay
Pleak

PTM22
FINFET10-HP
FINFET10-LL
CNTFET32
CNTFET22

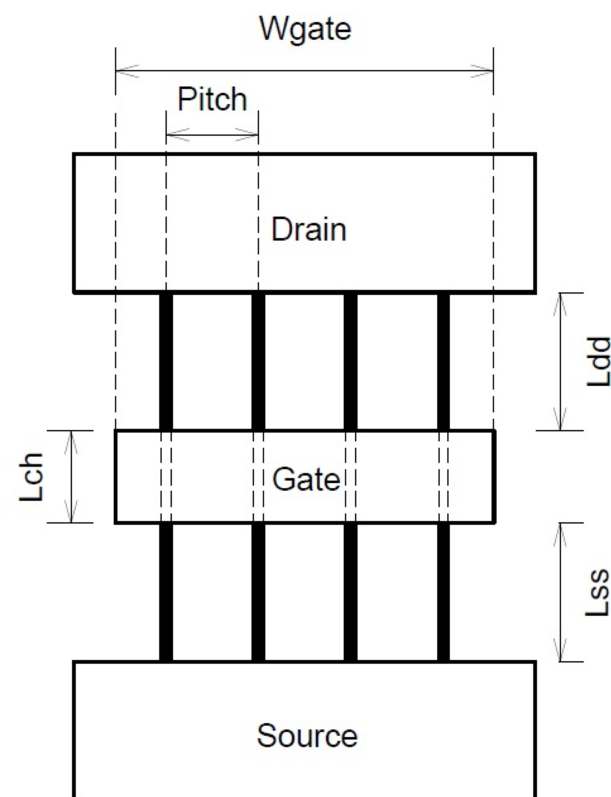
Results

Parameter Exploration

- Exemplary parameter exploration on CNTFET22 technology
- Key parameter: tube diameter (high impact on ON/OFF current)
- Note:
  - Number of tubes (N_{tubes}): changes

    $$\rightarrow \; N_{tubes} = \frac{W_{gate}}{Pitch} - 1$$

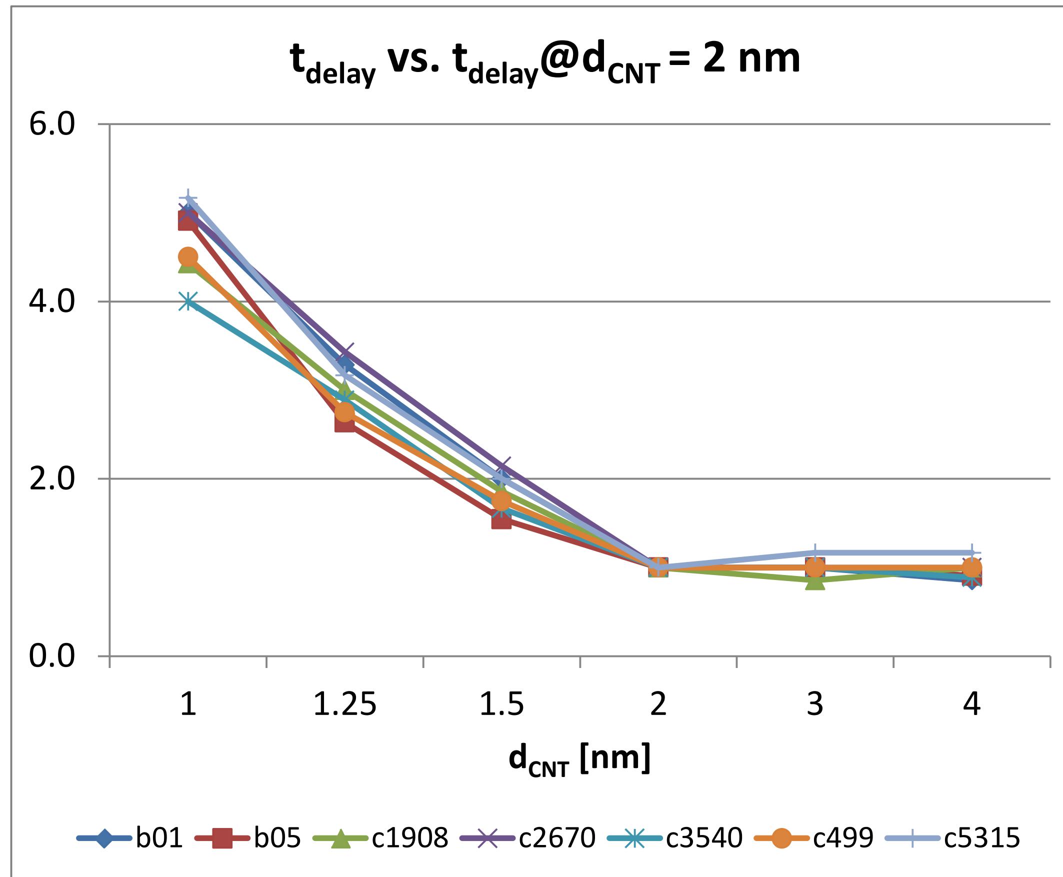
  - Distance between tubes (pitch): constant
  - Channel length (L_{ch}): constant



Results

Parameter Exploration

- Results for delay in comparison to standard diameter (d_{CNT} = 2nm)



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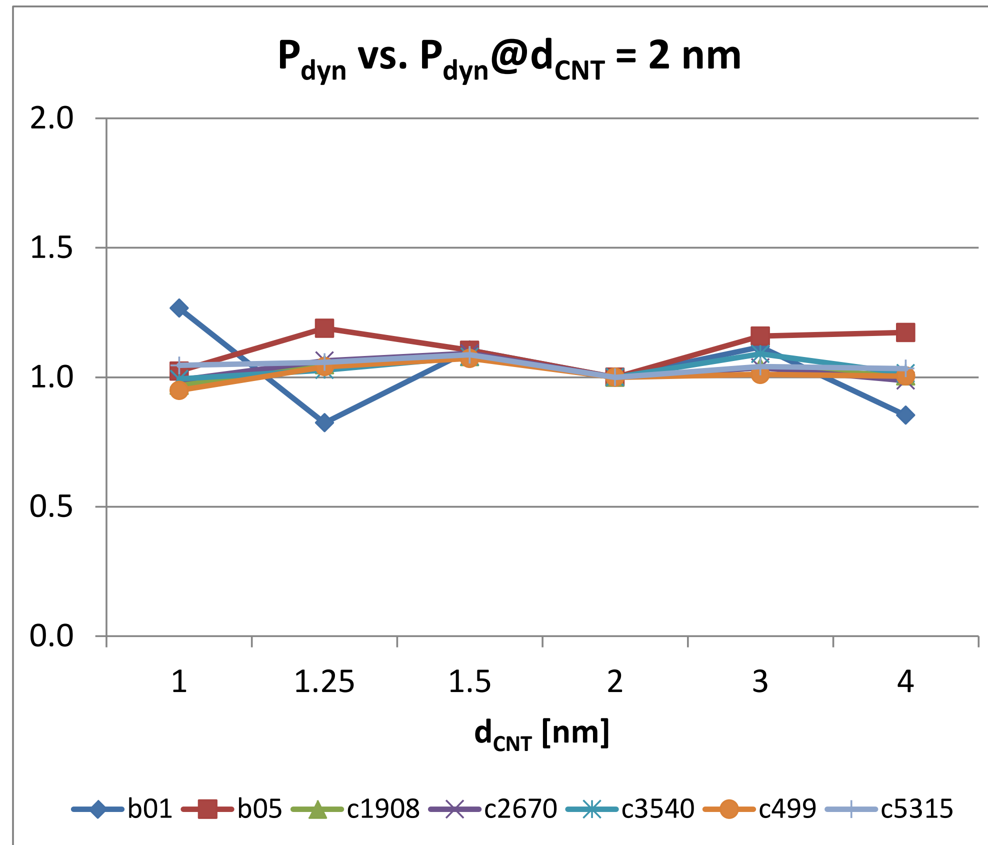
Results

Parameter Exploration

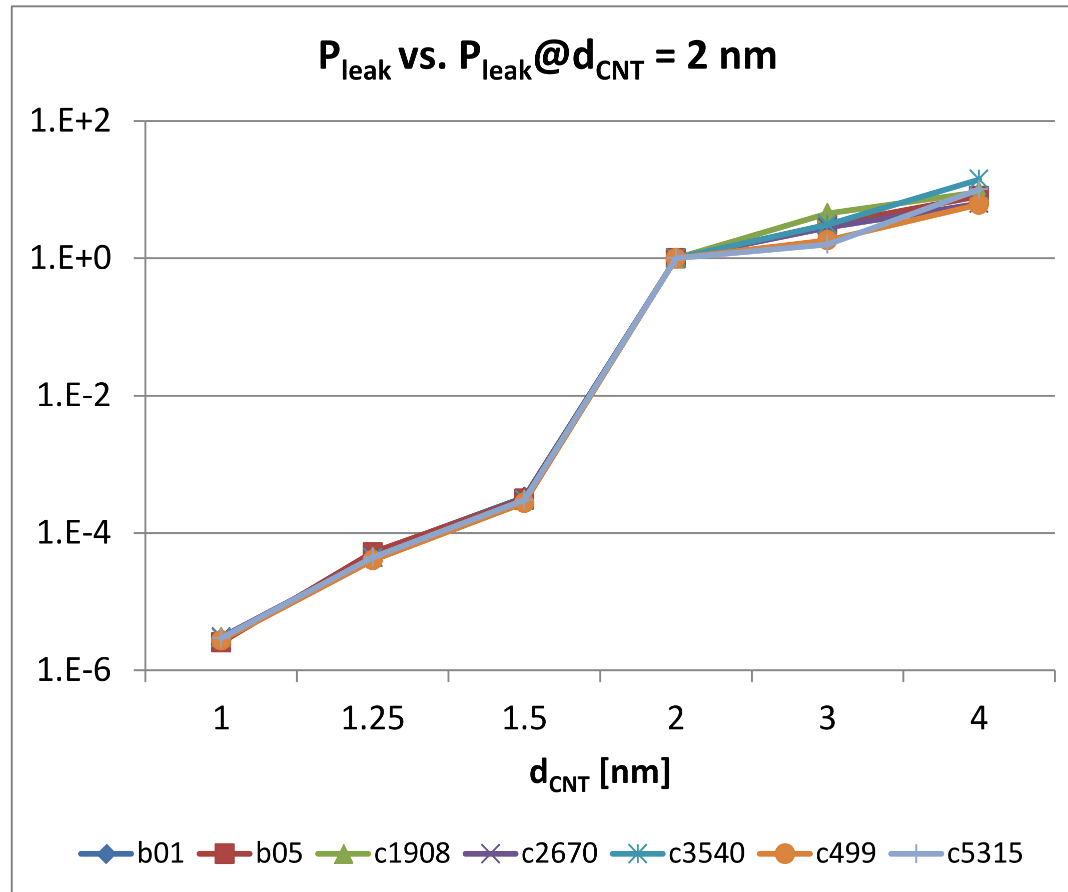
- Results for dynamic power consumption (P_{dyn}) in comparison to standard diameter (d_{CNT} = 2nm)



Results

Parameter Exploration

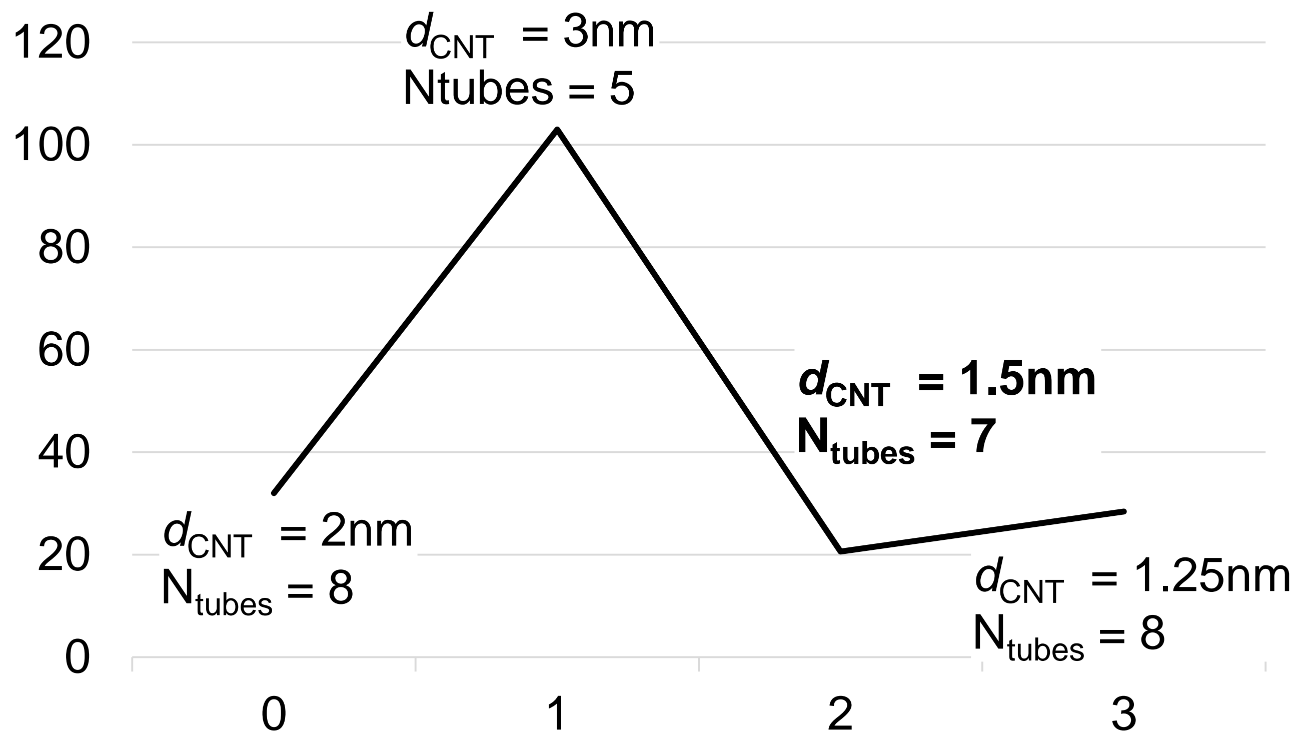
- Results for leakage in comparison to standard diameter



Results

Parameter Exploration

- Figure of Merit with weights $\varphi = 1$, $\gamma = 1$, $\gamma_{leak} = 1.5$



Conclusion

- New flow for exploration of technologies parameters
- Proposal of Figure of Merit for evaluation of technology parameter set
- Approach based on actual designs
- Increased the quality of predictions by up to 46%
- Applied successfully in CNTFET based technology

Thank you!

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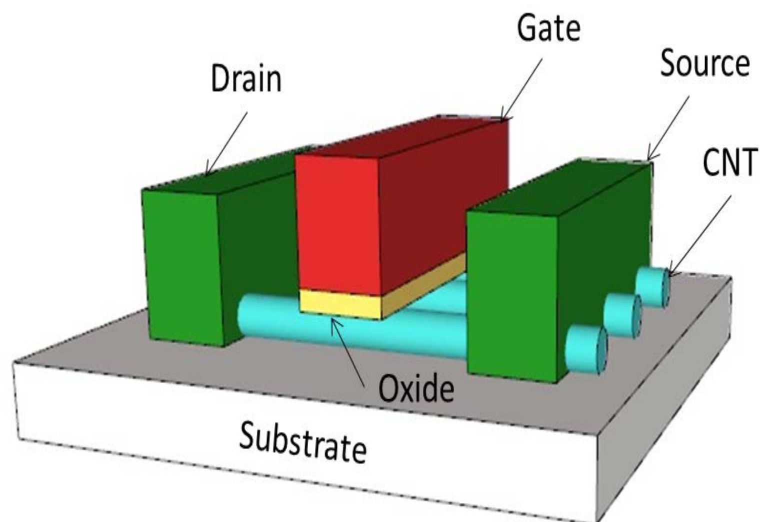
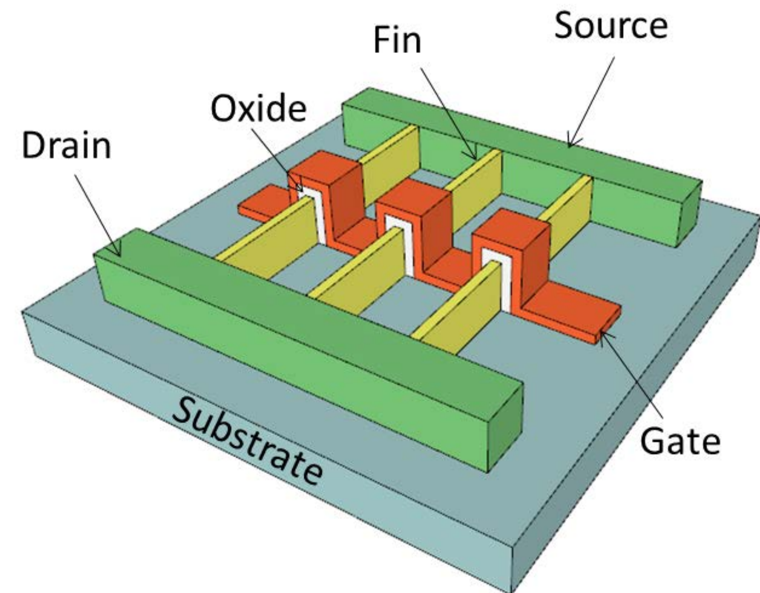
EXTRA CNFET



Feature size dependent		
Parameter	**Description**	**Typical Value**
W_{gate}	Gate width	3a
L_{ch}	Channel length	2a
L_{ss}	Doped CNT source-side extension region length	2a
L_{dd}	Doped CNT drain-side extension region length	2a
N_{tubes}	Number of nanotubes in a device	(W_{gate}/Pitch)-1
Feature size independent		
d_{CNT}	Tubes diameter	1.5 nm
Pitch	Distance between the centers of two adjacent CNTs within the same device	4 nm
Distance	Distance between the corners of two adjacent CNTs	2.5 nm
Tubes density	Tubes density in the device	250 CNT/µm
T_{ox}	Thickness of high-k top gate dielec-tric material	4 nm
L_{geff}	Mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.	200 nm
C_{sub}	Coupling capacitance between channel region and substrate	200 nF
E_{fi}	The Fermi level of the doped S/D nanotube.	0.6 eV

EXTRA FINFET

	Technology	
Parameter	FINFET10-HP	FINFET10-LL
L_{ch}	14 nm	14 nm
P/N*	1x1	1x1
V_{DD}	0.75 V	0.75 V
Fin height	21 nm	21 nm
Fin width	8 nm	8 nm
EOT	0.68 nm	0.88 nm
ETA0	0.6778	0.4079



EXTRA BULK

	Technology	
Parameter	PTM32	PTM22
L_{ch}	32 nm	22 nm
W_{min}	64 nm	44 nm
V_{DD}	1.0V	0.9V