Exploration of Technology Parameter Values of Integrated Circuit Technologies

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***Abstract* –The definition of parameters of integrated circuit technologies is driven by technological constraints as well as by intended applications. In case of the latter, opposing criteria, like design delay, power consumptions and area, have to be considered. Common approaches focus usually on the analysis based on selected and isolated cells. However, this might not represent the exact impact of a technology parameter on actual designs. Hence, this work proposes a flow for the exploration of technology parameter values that considers the application in real designs. Additionally, the proposed approach allows the comparison of different technology generation with a reasonable effort. Results indicate an improvement of the predictions of up to 46 % in comparison to single cell analysis. Further, the applicability of the approach is successfully evaluated using a predictive technology based on Carbon nanotubes.**

Keywords- Standard-cell; Carbon nanotubes; Design space exploration; Integrated circuit technology;

I. INTRODUCTION

Integrated circuit technologies possess a wide range of technology parameters, like transistor channel length, doping profiles, or thickness of gate oxide. These parameters are untouchable by the circuit designers, and thus, are the same in all designs based on that technology [1]. Usually, the choice of the technology parameter values is mainly driven by manufacturing constraints, such as limitations of the lithography process or characteristics of applied materials. Another impact comes from intended applications of the technology. For example, a common option of current technologies oriented for consumer applications are devices with high-performance or low-standby-power profile [2]. Thereby, devices differ in its threshold voltage and/or gate oxide thickness.

The selection of the parameter values based on intended application requires the analysis of how each parameter impacts characteristics of integrated designs, such as delay, power dissipation, and area. Usually, this analysis is done on selected cells that are integrated in a test environment that emulates typical cases, for example a fanout-4 (FO4) load [3, 4].

Standard cell design is an extensively applied methodology for digital circuit design [5]. In order to enable design analysis before fabrication, each standard cell has to be characterized in terms of delay, power consumption, and area. This characterization can be done using previously fabricated cells or be based on precise transistor level simulation. Hence, it also possible to characterize designs that use predictive technologies, as for example done by Qing et al. for a 5 nm FinFET technology [6] and Bobba et al. for a Carbon nanotube technology [7]. However, to the best of our knowledge, there is no research published on how the results of such analysis can be feed-back to the process of technology parameter selection.

The contribution of this work is the proposal of a flow that automatizes the exploration of technology parameters using actual designs. This considerably supports process engineers in the selection of technology parameters and enables researchers to explore the impact of novel technologies. Further, this flow allows, with reasonable effort, the comparison of different technology generations.

The rest of the paper is organized as follows. Section II presents preliminary information regarding the applied technologies in this work. Section III introduces the proposed flow. Section IV describes the simulation environment including the parameters of each technology. Section V presents the results of the comparison of different technologies, while section VI focuses on the exemplary parameter exploration of a Carbon nanotube based technology. Finally, section VII concludes this work.

II. PRELIMINARIES

This section introduces the technologies applied in this work.

A. Planar Bulk MOSFET

The classical planar bulk Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is still a widely applied transistor type [8]. The n-channel version of a MOSFET is composed of two n-type semiconductor regions, called source and drain, which are separated by a region of p-type semiconductor, called substrate. In case of the p-channel MOSFET, source, drain and substrate regions have opposite doping. A thin layer of insulating material, called gate oxide, covers the region between source and drain, while on top of this layer is located an electrode, called gate. The conductance of the

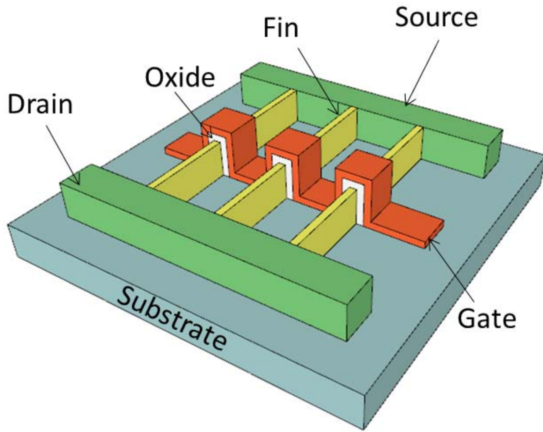

Fig. 1. Principal architecture of a FinFET

channel between drain and source is controlled by an electrical field applied over gate and source. Hence, the MOSFET acts as a switch controlled by its gate voltage.

B. FinFET

The FinFET technology is the current state-of-the-art technology for integrated circuits [9]. FinFET are part of the group of multi-gate field-effect transistors, which integrate more than one gate into a single device [4]. In case of the FinFET, a thin silicon body, called fin and acting as conducting channel, is wrapped by the gate electrode (see Fig. 1). Due to the wrapped gate structure, the electrical control over the channel is improved leading to high on-to-off current ratio, lower leakage currents, and lower susceptibility to short-channel effects [10].

C. Carbon nanotubes Transitor

The Carbon nanotubes field-effect transistor (CNTFET) is one of the most promising potential successors of the MOSFET transistor [11]. Its base component, the Carbon nanotube (CNT), is a nanocylinder composed by a sheet of Carbon atoms that possesses excellent electrical, thermal, and mechanical properties. Further, the ultrathin Carbon nanotube body provides a precise electrostatic control of its conductance. This enables the CNTFET to have extraordinary improvements of the intrinsic delay compared to common MOSFET technologies [12].

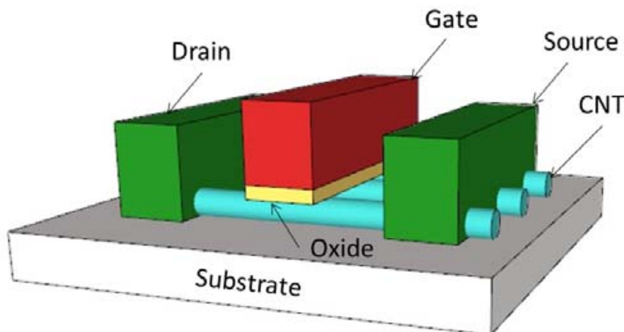

Fig. 2. Principal architecture of a Carbon Nanotubes Field-Effect Transistor (CNTFET).

Fig. 2 depicts the basic CNTFET structure. Similar to existing MOSFET technology, CNTFET features drain and source semiconductor regions as well as a gate electrode. Drain and source are connected via Carbon nanotubes, which act as a channel whose conductance is controlled by an electrical field applied over gate and substrate.

A significant advantage compared to other novel nanotechnologies is its compatibility to the conventional MOSFET fabrication process [13]. That is, source, drain, and gate region can built by existing manufacturing processes, while only the CNT region requires a Carbon nanotube grow process. Further, the CNTFET technology offers p-type and n-type devices, which permits the utilization of the CMOS approach.

The current principal problem of CNTFET fabrication is the control of the CNTs density and chirality. Variations of the density have considerable impact in the device performance [11]. Further, uncontrolled chirality can lead to metallic CNTs that cause source-drain short circuits and increase greatly the circuit power consumption [13].

III. Flow for Exploration of Technology Paramter

This section presents a methodology for exploring the values of parameters of technologies for integrated circuit design. This includes the design of standard cells libraries, its characterization, and the exploration of technology parameter values based on representative designs.

A. Origin of the approach

Choosing appropriate technology parameters is an important step before applying a new technology for integrated circuits. Thereby, a wide range of optimizations of a vast amount of parameters is possible. Thereby, technological constraints, for example minimum distances or lithography limitations, as well desired circuit characteristics, such as delay or power dissipation, have to be considered. In case of the latter, usually single cells are simulated under standard conditions, for example a fanout-4 load and predefined signal probabilities. However, these simulations cannot represent the actual use of the cells within real designs. Hence, there is a certain imprecision regarding the prediction of the impact of technology parameter values in final applications.

The fundamental idea of the proposed flow is the analysis how a technology parameter affects integrated designs and feed-back this information to the parameter selection process. Thereby, each parameter modification is integrated in a standard cell library, which is automatically characterized and utilized for synthesis of benchmark designs.

B. Proposed Flow

The initial step of the flow is the development of the circuit representation of the elements of the standard cell library. This step includes the set-up of the simulation environment, which enables functional tests and extraction of cell parameters. Further, typical load and timing characteristics are estimated in order to define parameters for the look-up tables applied in later cell characterization.

Hereafter, a set $\Phi = \{X_i \mid i = 1 \dots N\}$ of the N most significant technology parameters X_i is generated and the applicable value ranges for each X_i is estimated. This study is based on parametric analysis exploring the impact of the chosen parameters on the characteristics of basic cells, for example Inverter, NAND2, and FlipFlop. Of main interest are delay, area, as well as dynamic and leakage power consumption. The limits of the ranges of the technology values must be chosen such that fabrication is possible and that any increase or decrease, respectively, has no further significant positive impact on any of the characteristics.

Next, the iterative process of the technology parameter exploration is started. Initially, typical parameter values are chosen and all cells of the library are characterized, that is the estimation of input slope and load dependent propagation delays and output slopes, power consumption, and timing constraints in case of sequential cells. The results of the characterization are stored in a file format that can be read by synthesis tools, such as the Liberty Format [14].

Next, the generated cell library is applied for the synthesis of representative benchmark designs. The selection of the designs should be driven by future applications of the technology and contain a wide range of combinational and sequential designs of low and high complexity. Subsequently, all circuits are characterized in terms of delay, area, and power consumption.

In order to explore the technology parameters, the parameter X_i of the pre-chosen parameter set Φ is modified following equation (1):

$$X_i = X_i - \frac{X_i - x_i}{2} \;,\; x_i \in \{x_{i,min}, x_{i,max}\}, X_i \in \Phi \qquad (1)$$

with $x_{i,max}$ and $x_{i,min}$ are the maximum and minimum values of the parameter.

Next, the entire standard cell library characterization and benchmark synthesis is re-performed in order to verify the influence of the selected parameter.

The evaluation of the influence of the parameter modification is based on the figure of merit F. Thereby, the relative changes of principal design parameters, that is maximum delay t_{delay}, dynamic power consumption P_{dyn}, leakage power consumption P_{leak}, and area A, are weighted. This estimation is done over the sum of all chosen benchmark designs, following equation (2):

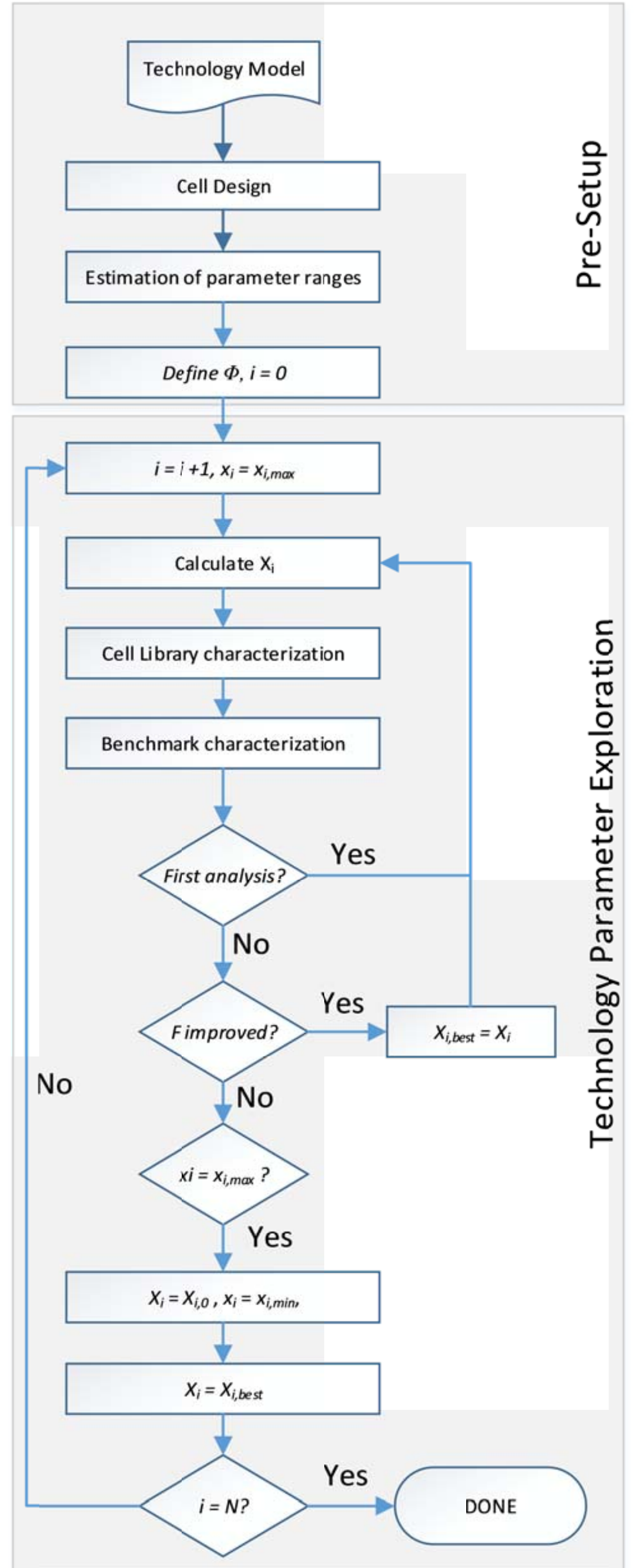

Fig. 3. Design, characterization and exploration flow

$$F(\Phi)=\varphi_1\left(\sum_{designs}\frac{P_{dyn,i}(\Phi)}{P_{dyn,i,init}}\right)^{\gamma_1}+\varphi_2\left(\sum_{designs}\frac{P_{leak,i}(\Phi)}{P_{leak,i,init}}\right)^{\gamma_2}+\varphi_3\left(\sum_{designs}\frac{t_{delay,i}(\Phi)}{t_{delay,i,init}}\right)^{\gamma_3}+\varphi_4\left(\sum_{designs}\frac{A_i(\Phi)}{A_{i,init}}\right)^{\gamma_4} \quad (2)$$

with φ and γ are the weighting factors defined by the designer. Further, and $P_{dyn,i,init}$, $P_{leak,i,init}$, $t_{delay,i,init}$, and $A_{i,init}$ indicate the initial parameter values of each design. It is desired that all principal design parameters decrease. Hence, a reduction of F for the chosen technology parameter values of the set Φ indicates an improvement.

The analysis of each technology parameter X_i starts with an increase, that is $x_{i,x} = x_{i,max}$ in equation (1). The parameter is changed until F is not decreasing any more. Then, the value of X_i that resulted in the best F is stored as $X_{i,best}$, and X_i is set to its initial value $X_{i,0}$. Next, the analysis with decreasing X_i is started. This analysis is continued as long as F is reduced. Afterwards, X_i is set to the value $X_{i,best}$ and the next technology parameter of the set Φ is chosen as well as analyzed following the same procedure until no improvement of F is achieved. The flow stops after analysis of all technology parameter of set Φ.

IV. Simulation Environment

This section presents the simulation environment that enables the verification of the proposed flow. Further, the parameters of the applied current and future technologies are detailed.

A. Characterization

The characterization of each cell can be done by comercial tools like Synopsys SiliconSmart [15] or open-source programs like LIBFILL [16]. Initially, the characterization environment must be configured. This configuration includes the set-up of the ranges for capacitive loads and input signal slews, operating voltages and temperature, logic voltage levels, and the thresholds values for the calculation of cell delay and transition times. Further, convergence parameters as well as cells specific characterization table values must be defined.

The created simulation environment applies the software SiliconSmart. Propagation delays are defined as the time intervals between input and output signals cross 50 % of V_{DD}. The transition times are defined as the time a signal requires to transit from 10 % to 90 % and 90 % to 10 % of V_{DD} for rising and following slopes, respectively. The ranges of the capacitive loads are set to 1X – 30X of the input capacitive load of the minimum inverter of the technology and feature size. The range of the transitions times of the input signal is set to 1X – 5X of the FO4 the transition times of a minimum inverter of same technology and feature size.

B. Technologies

Several current and future technologies were integrated in order to verify the applicability of the simulation environment and the proposed flow. All applied technologies are based on predictive and freely available models.

TABLE I. Selected Parameter Values for Bulk CMOS technology PTM32

	Technology	
Parameter	PTM32	PTM22
L_{ch}	32 nm	22 nm
W_{min}	64 nm	44 nm
V_{DD}	1.0V	0.9V

1) Bulk CMOS

The applied Bulk CMOS technology is based on the predictive technology models PTM for high performance [17], which is based on the BSIM4 spice model [18]. The feature sizes 32 nm and 22 nm, named PTM32 and PTM22, have been implemented. Table 1 lists the most important technology parameters, which are channel length L_{ch}, minimum width W_{min}, and supply voltage V_{DD}.

2) FinFET:

The applied FinFET technology is based on the predictive technology models PTM-MG for multi-gate devices [4], which are based on the BSIM-CMG spice model [19]. The feature size 10 nm with the high performance (HP) and low leakage (LL) versions have been implemented and named as FINFET10-HP and FINFET10-LL. Table II lists for each technology version the most relevant parameters, including the effective oxide thickness (EOT) and the drain induced barrier lowering parameter (ETA0).

3) CNTFET

As stated in the section II, Carbon nanotube transistor (CNTFET) is a promising technology for future integrated circuits. There is still no widely accepted completely analytical spice model, though, as this technology is still under development. Hence, this work applies the semi-empirical Stanford University Virtual Source CNFET VerilogA model that describes the current-voltage and charge-voltage characteristics of a short-channel CNTFET [20]. This model proved to have good accuracy as it considers gate resistance and capacitances, Schottky Barrier Effects, as well as parasitics on the Carbon nanotubes, source and drain [20]. The model is hierarchical and composed by three layers of abstraction.

TABLE II. Selected Parameter for applied FinFET technologies

	Technology	
Parameter	FINFET10-HP	FINFET10-LL
L_{ch}	14 nm	14 nm
P/N*	1x1	1x1
V_{DD}	0.75 V	0.75 V
Fin height	21 nm	21 nm
Fin width	8 nm	8 nm
EOT	0.68 nm	0.88 nm
ETA0	0.6778	0.4079

** Ratio of the PMOS and NMOS devices in the unit inverters*

TABLE III. SELECTED PARAMETER FOR APPLIED CNTFET TECHNOLOGIES

Feature size dependent		
Parameter	**Description**	**Typical Value**
W_{gate}	Gate width	3a
L_{ch}	Channel length	2a
L_{ss}	Doped CNT source-side extension region length	2a
L_{dd}	Doped CNT drain-side extension region length	2a
N_{tubes}	Number of nanotubes in a device	$(W_{gate}$/Pitch)-1
Feature size independent		
d_{CNT}	Tubes diameter	1.5 nm
Pitch	Distance between the centers of two adjacent CNTs within the same device	4 nm
Distance	Distance between the corners of two adjacent CNTs	2.5 nm
Tubes density	Tubes density in the device	250 CNT/µm
T_{ox}	Thickness of high-k top gate dielectric material	4 nm
L_{geff}	Mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.	200 nm
C_{sub}	Coupling capacitance between channel region and substrate	200 nF
E_{fi}	The Fermi level of the doped S/D nanotube.	0.6 eV

Table III lists the most relevant parameters and its typical values taken from [6] and [12], separating feature size dependent and independent parameters. The analysis has been executed for the features sizes 32 nm and 22 nm, named CNTFET32 and CNTFET22, whose parameters are listed in Table IV.

C. Standard cell Library

The applied standard cell library contains a basic set of combinational and sequential cells (see Table V). Further, all combinational cells are realized with two different sizes. Thereby, the cell sizing is based on the inverter cells, *i.e.* all cells have same driving strength as the inverter with same size.

TABLE V. LIBRARY CELLS AND SIZES

Combinational Cells	**Sizes**
Inverter	1x, 2x
AND2, NAND2	1x, 2x
OR2, NOR2	1x, 2x
MUX21	1x, 2x
XOR2	1x, 2x
Sequential Cells	
DFF with RS	1x

TABLE IV. PARAMETERS FOR EACH FEATURE-SIZE CNFET CELLS

	CNTFET32	CNTFET22
W_g	48 nm	33 nm
$L_{ch,}$ $L_{ss,}$ L_{dd}	32 nm	22 nm
N_{tubes}	10	7
V_{DD}	1.0 V	0.75 V

D. Benchmark Designs

The applied benchmark designs in this work are a mix of combinational designs (c1908, c2670, c3540, c499, c5315, c7552), taken from the ISCAS benchmark suite [21], and sequential designs (b01 and b05) of the ITC99 benchmark suite [22].

V. RESULTS

This section presents the comparison of the performance of the implemented technologies.

A. Technology Comparison

A remarkable option of the proposed flow is the possibility to compare with reasonable effort the performance of different technologies based on implementations in actual designs. Further, the flow permits the application of different kind of technology models, like SPICE, circuit level, or VerilogA.

All technologies presented in the previous section have been analyzed by the proposed flow. For each benchmark design have been determined the maximum delay (t_{delay}), the dynamic power consumption (P_{dyn}), and the leakage power (P_{leak}). Further, the power-delay-product (PDP), the product of maximum delay and dynamic power consumption, was calculated. In order to facilitate the comparison, all results were normalized in relation to the PTM32 technology.

Fig. 4 depicts the comparison of the PDP values over all

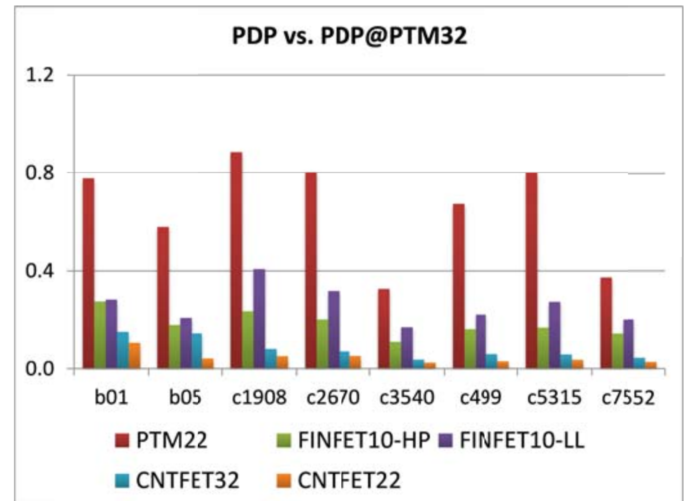

Fig. 4. Comparison of Power-Delay-Product (PDP) of selected technologies related to the PTM32 technology

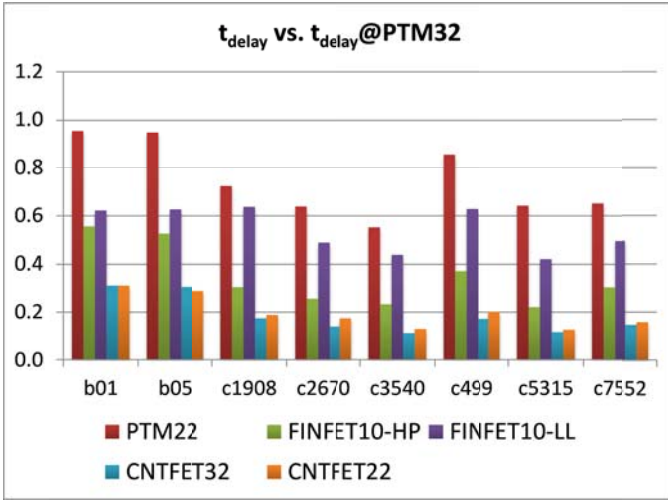

Fig. 5. Comparison of maximum delay (t_{delay}) of selected technologies related to the PTM32 technology

technologies, whereas lower values indicate better results. The PDP is a commonly applied indicator as it combines two of the most significant parameters of today's integrated circuit. An interesting aspect is here that both parameters usually are opposing, that is the reduction of one leads to the increase of the other. The results show that all technologies improve in relation to PTM32. Further, all designs realized in CNTFET technologies outperform their counterparts realized in bulk CMOS or FinFET technologies. The comparison between the high performance (HP) and low leakage (LL) version of the FinFET technology reveals that the former leads to better PDP values.

The comparison of the maximum delay t_{delay} is presented in Fig. 5. As expected, all technologies show a decrease of the maximum delay in comparison to PTM32. Further, the HP version of the FinFET technology leads to considerably faster designs than the LL one. Surprisingly, the CNTFET22 technology results in slightly higher delays than CNTFET32. This observation can be explained with the fact that the characteristics of CNTFET depend less on the channel length, but more on the amount of CNTs and the CNT diameter [7, 12].

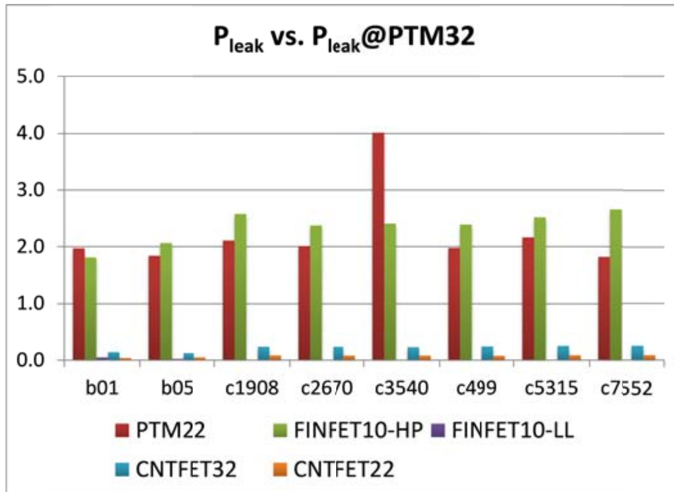

Fig. 6. Comparison of leakage power consumption (P_{leak}) of selected technologies related to the PTM32 technology

The results for the leakage power consumption indicate that only designs realized in the bulk CMOS technology PTM22 and the high performance FinFET technology FINFET10-HP have higher leakage than their counterparts realized in PTM32 (see Fig. 6). Further, the low leakage FinFET technology FINFET10-LL outperforms all other technologies, including CNTFET.

In order to verify the difference between an analysis solely based on a single cell and on actual designs, the average parameter values of all designs were calculated for each technology version and related to the PTM32 technology. Next, the parameters PDP, t_{delay}, and P_{leak} were estimated for an inverter in FO4 configuration in all technologies and again related to the PTM32 technology. The results of this comparison are shown in Table VI. It can be noted that the relation amongst the values for a FO4 inverter are not the same as amongst the designs for different technologies. For example, while the analysis of a FO4 inverter in the PTM22 technology indicates a delay decrease of 16 %, the design analysis revealed a reduction of 32 %.

The comparison in Fig. 7 shows that for PDP and t_{delay} the results of the FO4 inverter differ between 11 to 46 % from the average results estimated by the design analysis. In case of leakage, the maximum difference between results of FO4 and design analysis is 33 %. Consequently, it can be concluded that the proposed flow allows a considerable more accurate estimation of the impact of technology parameter compared to a common analysis on single cells.

VI. Paramter Exploration for CNTFET

This section presents the results of the application of the proposed parameter exploration flow for a Carbon nanotube transistor (CNTFET) technology.

A. Parameter Selection

According to [11], an increase of the diameter d_{CNT} of the nanotubes within a CNTFET leads to an exponential increase of the OFF current, while the ON current increases linearly. This turns the diameter to a key parameter to balance speed

TABLE VI. Average Design Paramters (Flow) and Cell Parameters (FO4) related to PTM32 technology

	Flow PDP	FO4 PDP	Flow t_{delay}	FO4 t_{delay}	Flow P_{leak}	FO4 P_{leak}
PTM32	1.00	1.00	1.00	1.00	1.00	1.00
PTM22	0.60	0.68	0.68	0.84	2.28	1.75
FINFET10-HP	0.19	0.23	0.32	0.44	2.37	1.93
FINFET10-LL	0.27	0.35	0.51	0.64	0.01	0.01
CNTFET32	0.10	0.12	0.17	0.32	0.21	0.23
CNTFET22	0.05	0.06	0.18	0.31	0.08	0.12

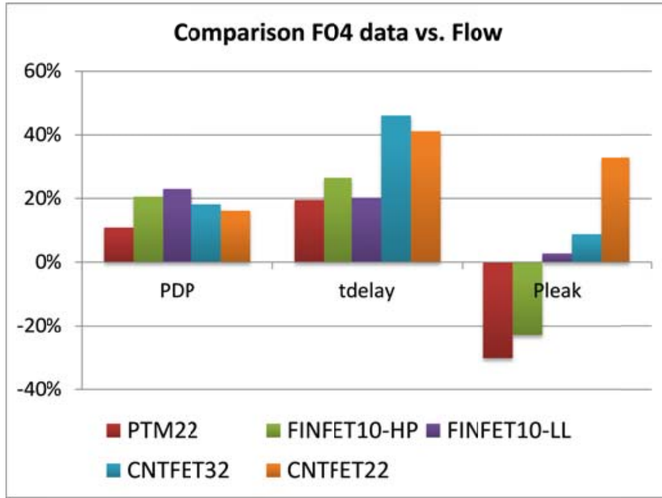

Fig. 7. Difference between average parameter data of all design and data of a FO4 inverter

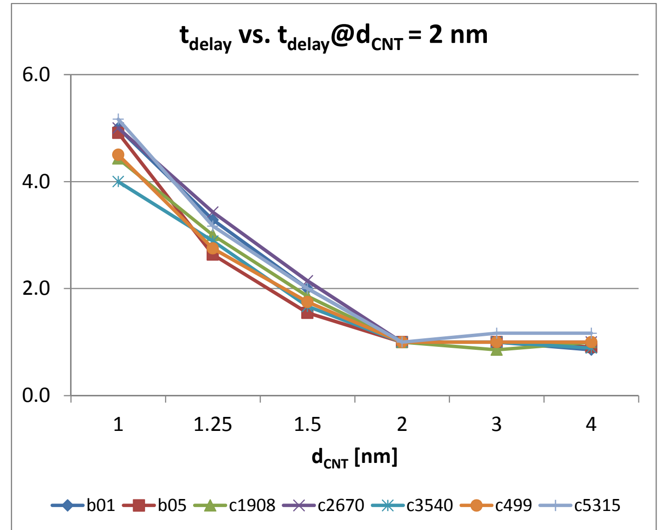

Fig. 8. Maximum design delay t_{delay} for different diameter d_{CNT} of the nanotubes related to the results for d_{CNT} = 2 nm.

and leakage power consumption. Hence, the proposed approach was applied to explore the impact of this parameter on actual designs in the CNTFET22 technology.

As can be noted in Table III, several geometric parameters of CNTFET impact each other, such as the diameter d_{CNT} and the distance between the nanotubes if a constant metal gate width W_{gate} is assumed.

During execution of the flow, a constant distance of 2.5 nm and a constant W_{gate} of 33 nm have been defined. The initial parameter value for d_{CNT} was set to 2 nm, following recommendations of the literature [7, 11], which results in a nanotube amount N_{tube} of 8. Following simulations on inverter, NAND2, and FlipFlop cells indicated an adequate range for d_{CNT} of $d_{CNT,min}$ = 1 nm and $d_{CNT,max}$ = 4 nm.

B. Exploration Flow

The design parameters maximum delay t_{delay}, dynamic power consumption P_{dyn}, and leakage power consumption P_{leak} have been chosen for the exploration of the technology parameter d_{CNT}. The related weighting factors φ and γ have been equalized to 1, with exception of γ_{leak} which was set to 1.5 in order to compensate the exponential relation between P_{leak} and CNT diameter [7, 11].

Based on the parameters defined in the previous subsection, the initial standard cell library was characterized. Next, this library was applied for synthesis and characterization of the benchmark designs. With the initial values for maximum delay, dynamic power consumption, and leakage power consumption at hand, d_{CNT} was increased following equation (1) to d_{CNT} = 3 nm, which resulted in a new nanotube amount of N_{tube} = 5. Subsequently, the complete automatized process of standard cell library characterization, synthesis, and benchmark design analysis was executed again. Based on the extracted values the merit factor F could be determined using equation (2). The results indicated a deterioration of the technology, as F increased from 32.5 to 103.0. Thus, d_{CNT} and N_{tube} were set to 1.5 nm and 7, respectively. This resulted in a better value for F, which decreased to 20.6. In the next step, d_{CNT} and N_{tube} were set to 1.25 nm and 8, which increased F to 28.4. Thus, the estimated best value for d_{CNT} is 1.5 nm, which complies with values known from the literature [7, 11].

C. Analysis

In the following, the observed behavior undergoes a detailed analysis. Fig. 8 depicts the maximum design delays for different diameter of the nanotubes related to the results for d_{CNT} = 2 nm. It can be noted that the relation of the results amongst combinational (cXXX) and sequential designs (bXX) is very similar. Further, the results indicate that for wider but less nanotubes the t_{delay} is not affected.

Fig. 9 shows the dynamic power dissipation for different diameter of the nanotubes related to the results for d_{CNT} = 2 nm. It can be observed that combinational and sequential designs behave slightly different from each other. This is based on the FlipFlops which have high impact on both sequential designs. However, it can be concluded that the dynamic power consumption does not change much. This is an expected behavior as the gate width is kept constant.

Fig. 10 illustrates the leakage power dissipation for different diameter of the nanotubes related to the results for d_{CNT} = 2 nm. As can be noted by the logarithmic axis, the leakage power consumption changes very strongly, which is expected as the relation between P_{leak} and d_{CNT} is known to be exponential [7, 11].

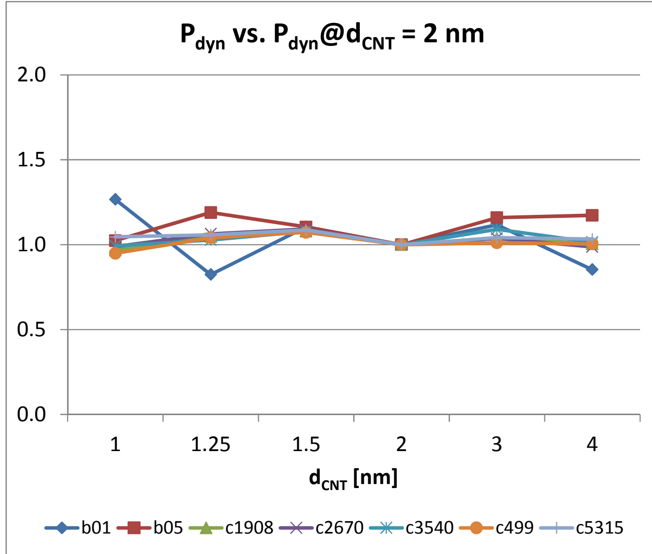

Fig. 9. Dynamic power dissipation P_{dyn} for different diameter d_{CNT} of the nanotubes related to the results for d_{CNT} = 2 nm.

VII. Conclusion

This work proposes a flow for exploration of the impact of technology parameters on actual designs. This considerably supports process engineers in the selection of technology parameters and enables researchers to explore the influence of novel technologies on integrated designs. As indicated by simulation results, the quality of the predictions can be improved by up to 46 % in comparison to single cell analysis. Further, the application on a predictive Carbon nanotube based technology indicated the feasibility of the proposed flow.

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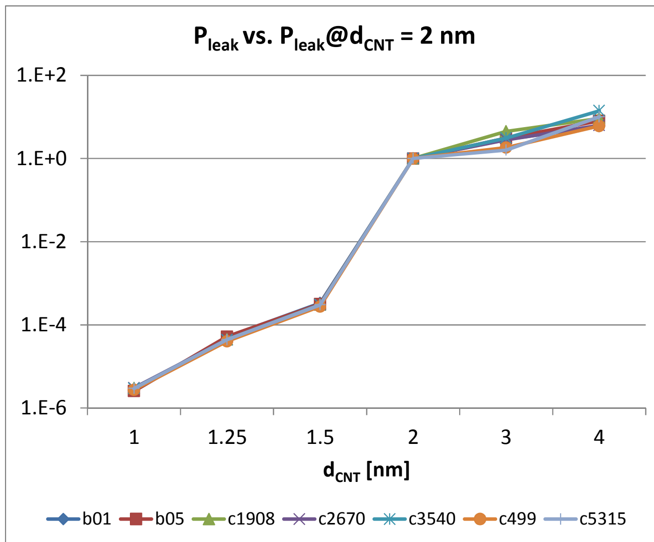

Fig. 10. Leakage power dissipation P_{leak} for different diameter d_{CNT} of the nanotubes related to the results for d_{CNT} = 2 nm.

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