Chip in Brasília

SBCCI 2012

25th Symposium on Integrated Circuits and Systems Design

Robust Modular Bulk Built-In Current Sensors for Detection of Transient Faults

Frank Sill Torres[+], Rodrigo Possamai Bastos[*]

[+] *Department of Electronic Engineering, Federal University of Minas Gerais, Belo Horizonte, Brazil*

[*] *LIRMM, Université Montpellier II / CNRS UMR 5506*

Montpellier, France

Outline

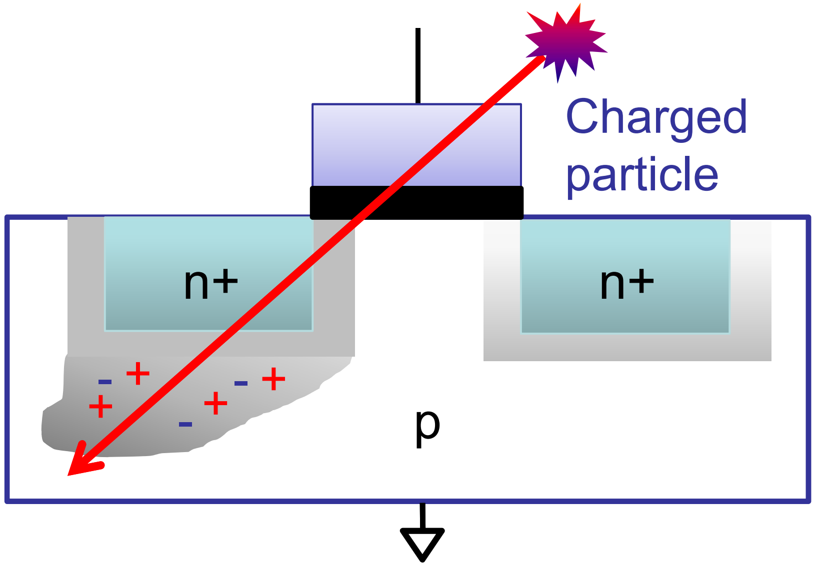
- Preliminaries
- Modular Bulk Built-In Current Sensors
- Results
- Conclusion

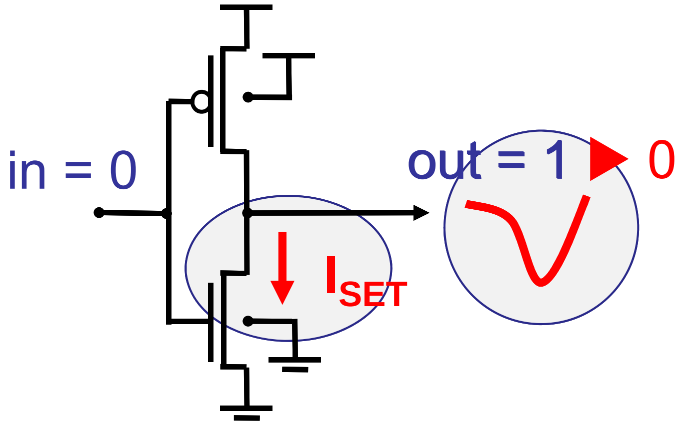
Preliminaries

Transient-Faults in Integrated Circuits (IC)

- Increasing susceptibility of CMOS IC to radiation effects due to decreasing technology sizes
- Environmental (α-particles, neutrons, …) and intentional (laser beams, …) sources

► Can cause transition faults

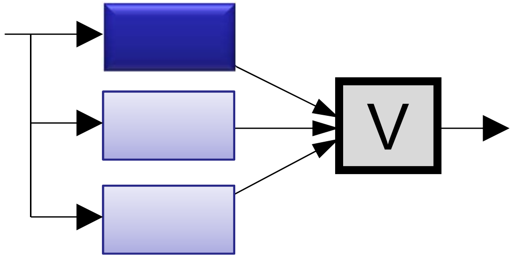




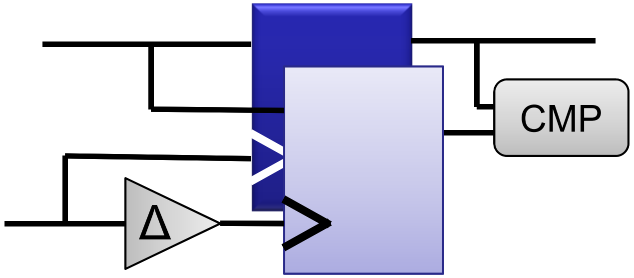
Preliminaries

Solutions for Transient Fault Detection

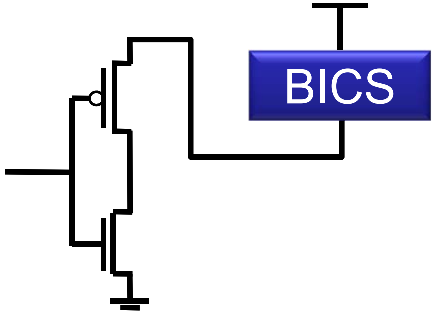
- Redundancy (Time, Logic)
  - Well known approach
  - Strong increase in area, power and/or delay



- Shadow Latches (*Razor*)
  - Moderate area increase
  - Useless against long-duration TF



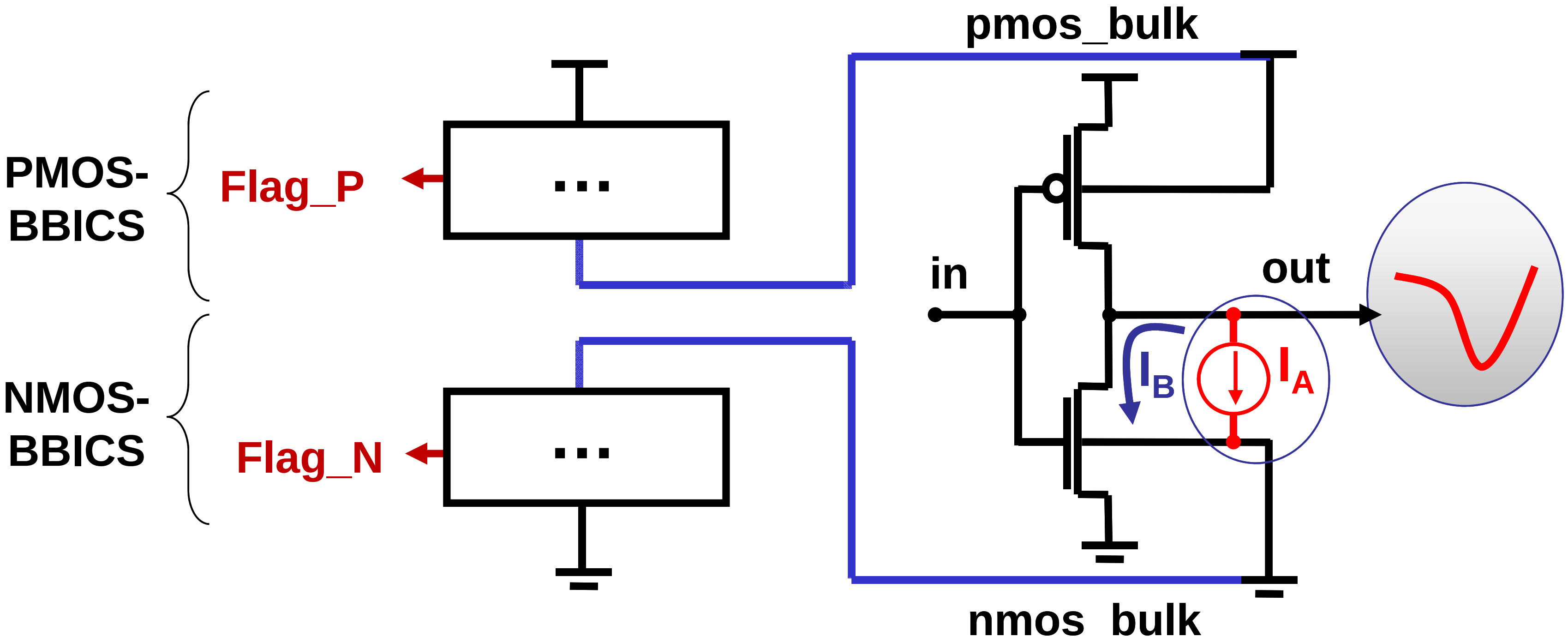
- Built-In Current Sensors (BICS)
  - Good for Memory block
  - Not appropriate for logic



Preliminaries

Bulk Built-In Current Sensors

- At particle strikes transistor in off mode → generation of current between transistor's reverse-biased drain-bulk pn-junction
- Idea: Current sensor between Bulk and ground → Bulk BICS (BBICS)



Neto, Micro, 26/5, p. 10, 2006

Modular Bulk Built-In Current Sensors

Origination of Approach

Common problems of existing Bulk-BICS

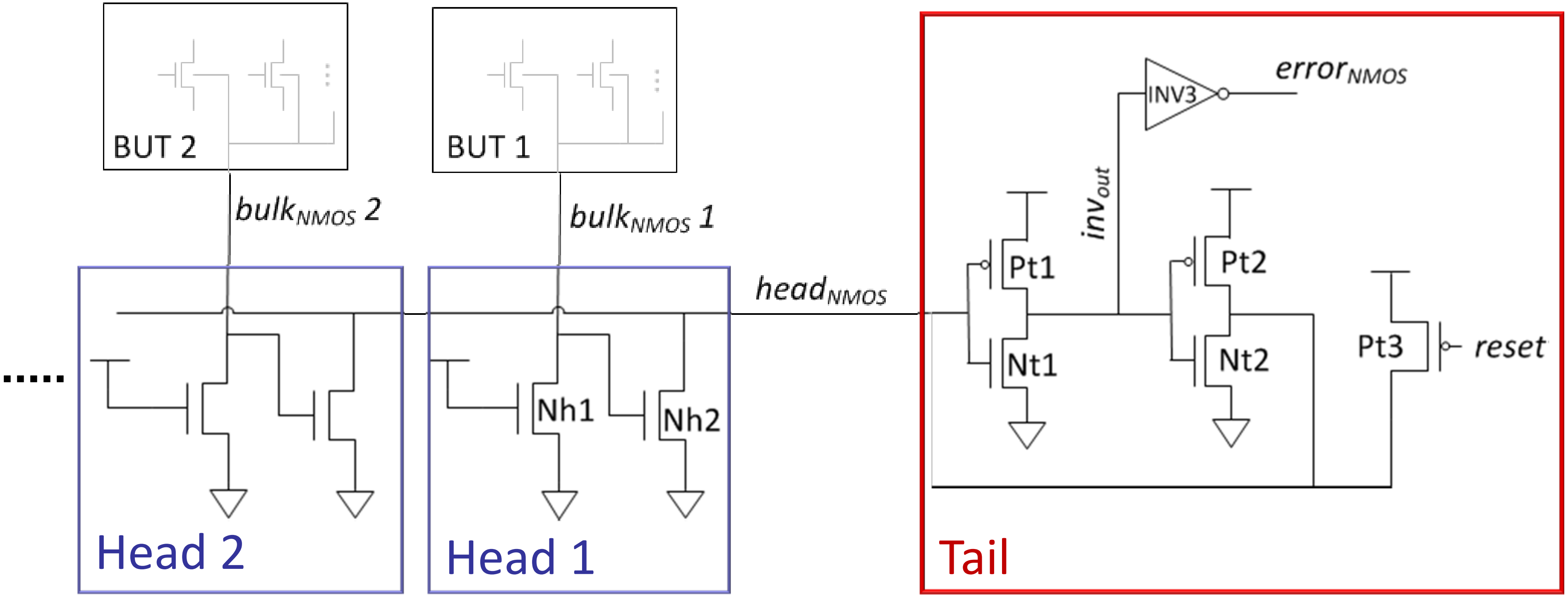
- High **area** effort
- **Strong** susceptibility to parameter / temperature variations
- **Offset** on **bulk** voltage → increased leakage (sub-threshold) of monitored circuits

Proposed solution

- **Functionality sharing** (reduction of power/area)
- **Bulk connected directly** with VDD/GND via a high ohmic transistor (as proposed in “*Wirth, in Mic. Rel., v.48/5, 2008*”)
- Implementation of **positive feedback structure** (increase of stability / decrease of sensor response time)

Modular Bulk Built-In Current Sensors

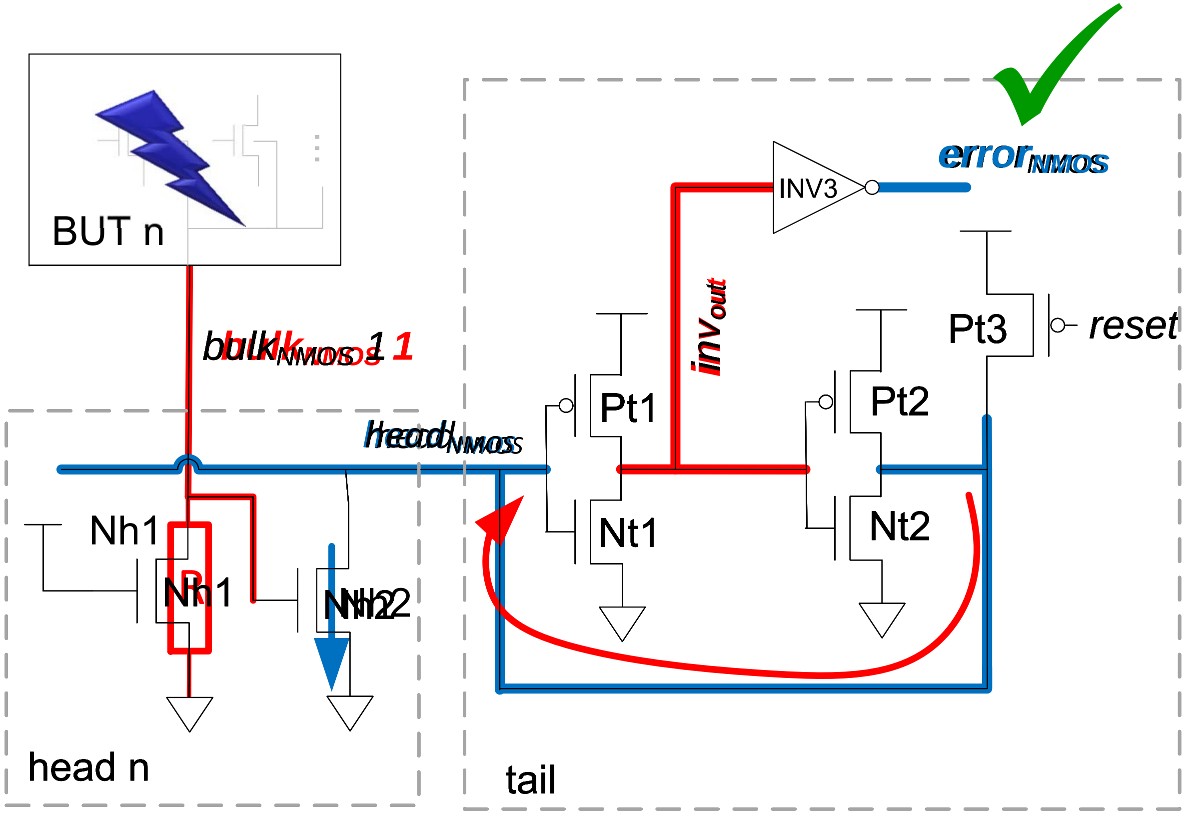
Architecture (only NMOS)



Modular Bulk Built-In Current Sensors

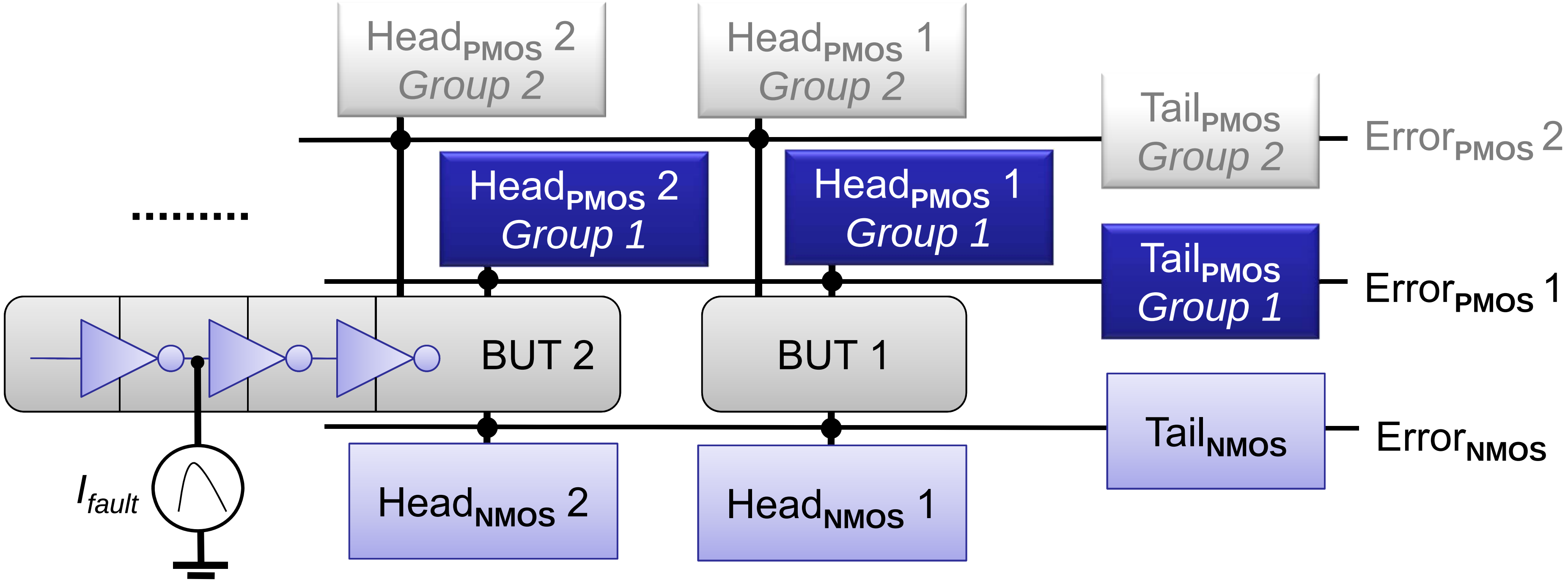
Mode of Operation (NMOS)

1. Particle Strike
2. Current through Nh1 → voltage peak on *bulk*$_{NMOS}$
3. Nh2 starts to conduct → voltage drop on *head*$_{NMOS}$
4. State of *inv*$_{out}$ changes → pos. feedback
5. Error flag set



Results

Simulation Environment



- BUT (Block Under Test): 6 chains of 10 inverter
- 2 groups of PMOS mBBICS (load equalization w/ NMOS mBBICS)
- Particle strike via current source connected to 5th inverter of 1st chain
- Predictive 16 nm technology (Bulk CMOS, Berkeley)

Results

Detection Capability (6 Heads, nominal case)

		PMOS		NMOS	
Q_f	t_f *(tr = 1ps)*		t_{resp}		t_{resp}
1 fC	5 ps	○✗	-	○✗	-
2 fC	5 ps	✶✓	452 ps	✶✓	430 ps
3 fC	5 ps	✶✓	136 ps	✶✓	76 ps
4 fC	5 ps	✶✓	89 ps	✶✓	50 ps
1 fC	10 ps	○✗	-	○✗	-
2 fC	10 ps	✶✓	270 ps	✶✓	210 ps
3 fC	10 ps	✶✓	78 ps	✶✓	62 ps
4 fC	10 ps	✶✓	55 ps	✶✓	43 ps
1 fC	20 ps	○✗	-	○✗	-
2 fC	20 ps	○✓	210 ps	○✓	175 ps
3 fC	20 ps	✶✓	81 ps	✶✓	70 ps
4 fC	20 ps	✶✓	55 ps	✶✓	50 ps

TF – Transient Fault, t_{resp} – Sensor Response Time

○✗ - no TF no detection

○✓ - no TF detection

✶✓ - TF detection

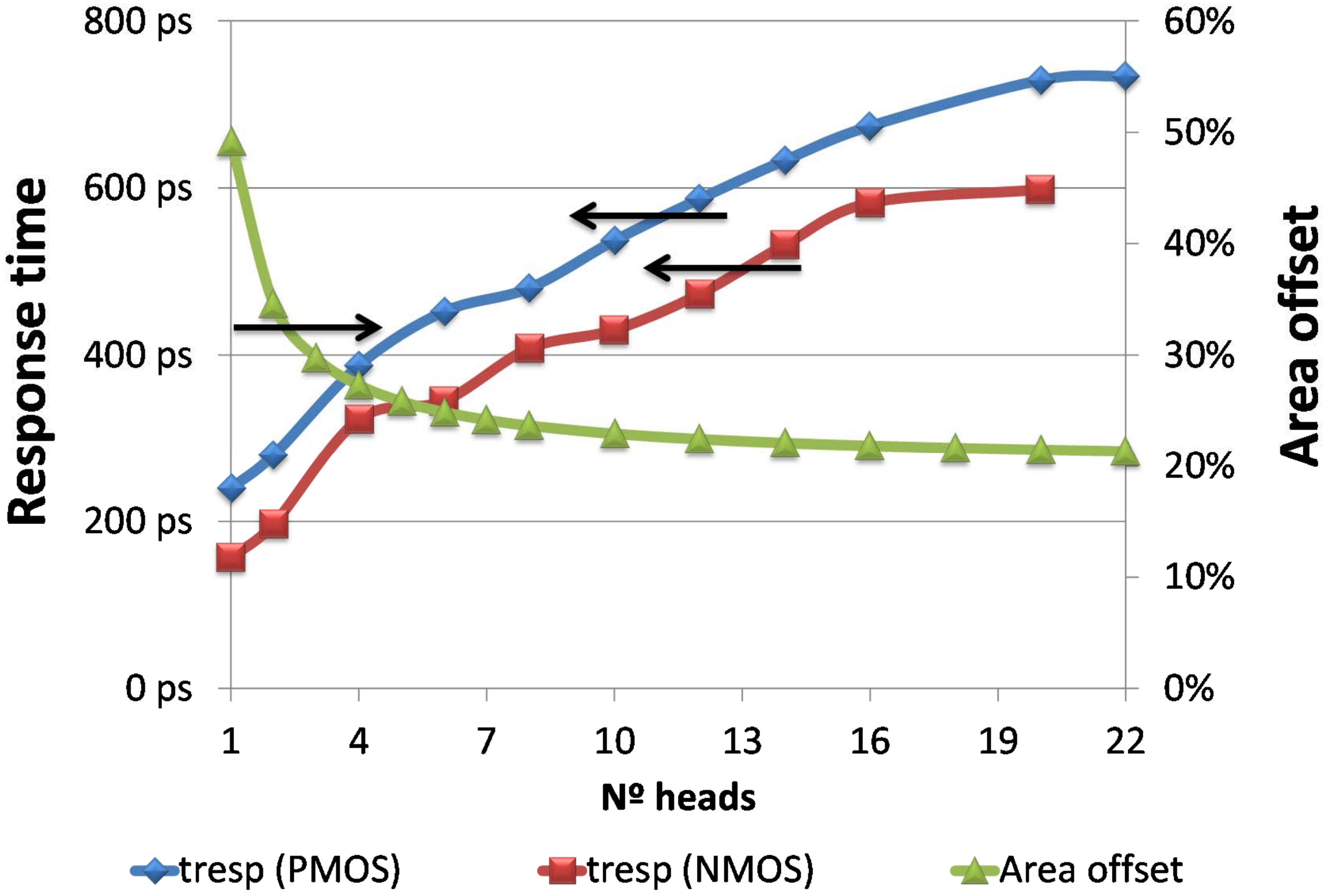
✶✗ - TF no detection

$$I_{fault} = \frac{Q_f}{t_f - t_r} \ldots$$

$$\ldots * \left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right)$$

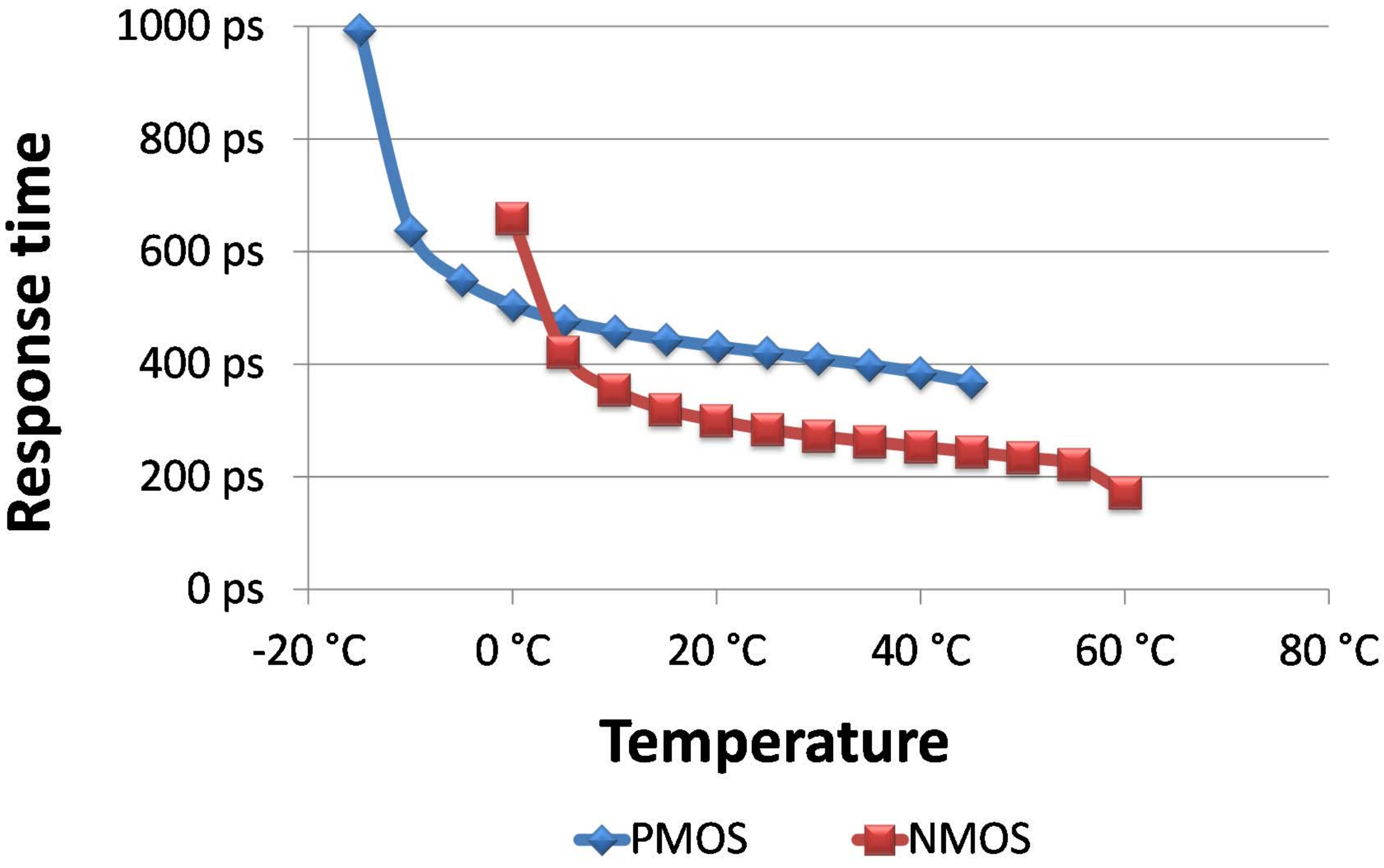
Results

Influence of Heads Amount (Nominal Models, Q_f = 2 fC, t_f = 5 ps)



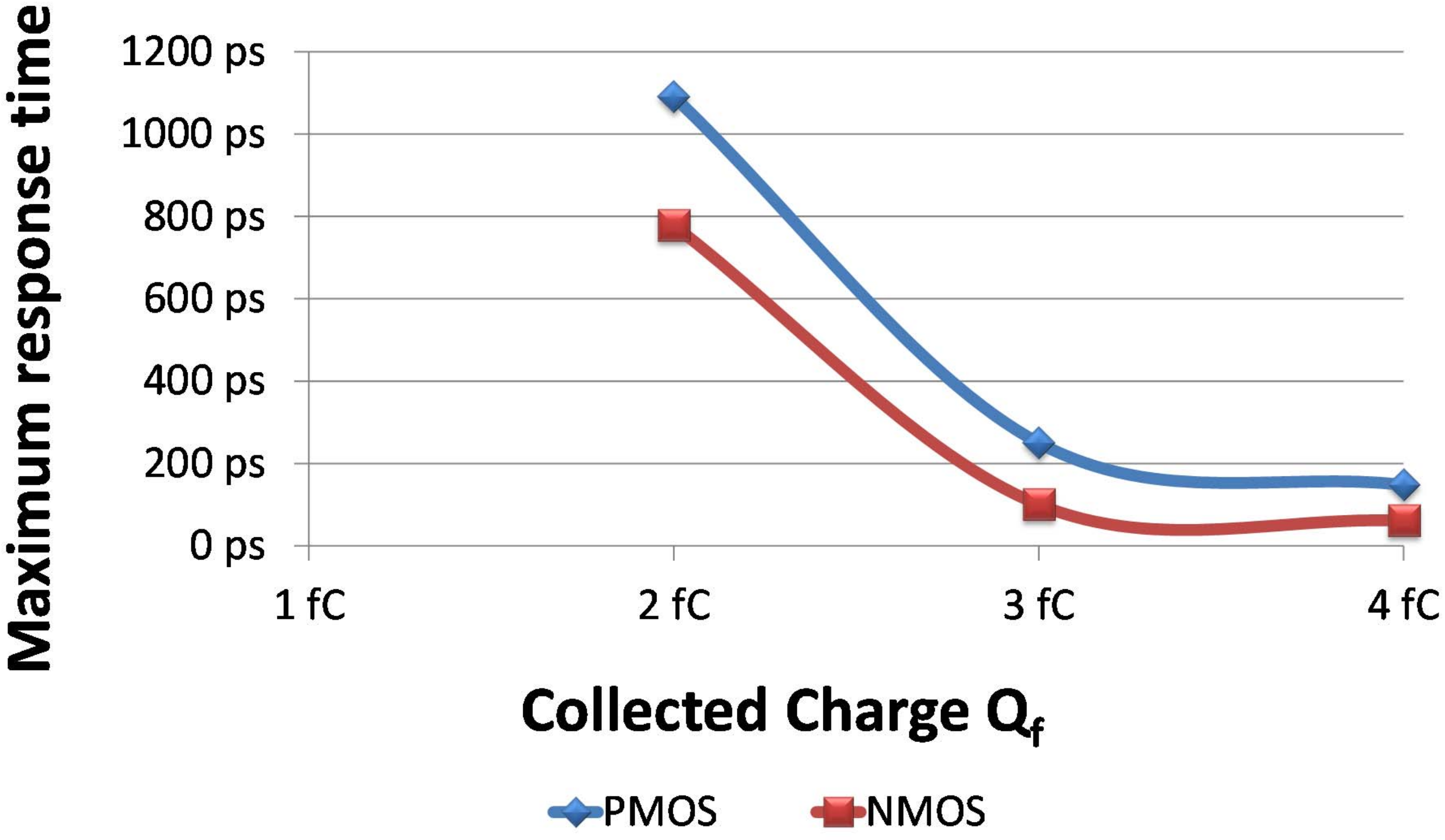
Results

Temperature Analysis (Nominal Models, Q_f = 2 fC, t_f = 5 ps)



Results

Monte Carlo Analysis (t_f = 5 ps)



Conclusions

- Bulk Built-In Current Sensors (BBICS) promising solution to detect soft errors in current CMOS technologies
- Main problems: susceptibility to variations, area, power
- Proposed modular BBICS (mBBICS) combines functional block sharing and positive feedback
- Simulations (16 nm PTM)
  - All injected transition faults detected for nominal and MonteCarlo (MC) case
  - Max. response times of ca. 500 ps (nominal) and ca. 1 ns (MC)
  - Area offset of 25 %
  - Very low increase in power dissipation

Thank you!

franksill@ufmg.br
bastos@lirmm.fr

OptMA^{lab} / ART
www.asic-reliability.com