Reliability Enhancement via Sleep Transistors

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***Abstract*—CMOS is still the predominating technology for digital designs with no identifiable concurrence in the near future. Driving forces of this leadership are the high miniaturization capability and the reliability of CMOS. The latter, though, is decreasing with an alarming pace against the background of technologies with sizes at the nanoscale. The consequence is a rising demand of solutions to improve lifetime reliability and yield of today's integrated systems. Thereby, a common solution is the redundant implementation of components. However, redundancy collides with another major issue of integrated circuits – power dissipation. The main contribution of this work is an approach that increases the lifetime reliability at only low delay and power penalty. Therefore, the well-known standby-leakage reduction technique "Sleep Transistors" is combined with the idea of redundancy. Additional, we propose an extended flow for reliability verification on transistor level. Simulation results indicate that the new approach can increase the lifetime reliability by more than factor 2 compared to initial designs.**

Keywords-reliabiltiy; sleep transistors; redundancy; simulation

I. Introduction

Today's designers of integrated digital circuits are facing a substantial amount of problems and restrictions to meet the required performance of their designs. This includes, among others, delay as well as area restrictions but also the consideration of power dissipation, and lifetime reliability. Unfortunately, all mentioned parameters are strongly related, i.e. the improvement of one leads to a deterioration of the other, and vice versa. Nevertheless, the application of adequate design techniques can mitigate the parameter's effects on each other. This paper proposes such a technique to tackle the problem of decreasing lifetime reliability in CMOS nanometer technologies. These technologies, with structure sizes in the range of several nanometers, suffer under an increased susceptibility to different kinds of failures during operation [1]. In contrast to previous technologies, solutions in the manufacturing process are, nowadays, not sufficient to deal with this kind of issues. Thus, the problem of reliability is an increasing concern also on higher design layers. Thereby, three main strategies can be identified: design techniques that detect errors (I) [2][3], techniques that detect and correct errors (II) [4], and techniques that increase the mean time to failure (III) [5][6]. Our proposed approach relates to strategy (III) and applies the combination of the well-known sleep transistor technique and the idea of redundancy to extend the lifetime reliability of integrated designs.

The rest of the paper is organized as follows: section 2 presents fundamental information to simplify the understanding of this work. Following, section 3 introduces the proposed approach while section 4 presents an extended verification flow for lifetime estimation of integrated circuits. The subsequently section 5 shows simulation results and, finally, section 6 concludes this work.

II. Preleminaries

This section presents a short overview about the main error sources in current nanometer technologies. Further, the sleep transistor approach is shortly introduced.

A. Fundamentals of Reliability

The term Reliability $R(t)$ is to be understood as the probability of a system to perform as desired until time instance t. For instance, $R(t_x) = 0.9$ states that there is an 90 % chance that the system is still running at time t_x. Furthermore, the failure rate λ expresses the probability that a system fails in a given time interval. Assume that 10 out of 100 systems fail in a given year; hence, an individual system will fail with a probability of 10 % in that same year. For most cases, a constant failure rate λ is assumed over the useful system lifetime [7] so that reliability $R(t)$ can be expressed by the exponential function (1). Closely related to the rather probabilistic expressions of reliability and failure rate is the Mean Time To Failure (MTTF), which is the average time that a system runs until it fails. Hence, it is equal to the expected lifetime and is expressed as the inverse of the constant failure rate λ (2).

$$R(t) = e^{-\lambda t} \tag{1}$$

$$MTTF = \int_0^\infty R(t)dt = \frac{1}{\lambda} \tag{2}$$

Even though, these equations are used in most calculations, it needs to be noted that the assumption of a constant failure rate λ is only valid for the regular lifetime. Thus, infant mortality as well as wear-out mechanisms are excluded and are for the most part described by Weibull distributions [7].

B. Failure Mechanisms in Nanometertechnologies

Integrated circuits realized in nanotechnologies suffer under several lifetime degrading effects. The recently most reported ones are Electromigration (EM), Time Dependent Dielectric Breakdown (TDDB), and Negative Bias Temperature

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Instability (NBTI). Thereby, the best-known failure mechanism is electromigration which mainly concerns the aluminum or copper interconnects. Electromigration means the transport of material atoms due to the gradual movement of the ions in a conductor caused by the electric current [8]. Due to this atom migration material can be depleted or accumulated. As consequence, high resistive connections or even abrupt breaks can be created. Another result can be undesired connections between interconnects. Equation (3) shows a widely used model for the *MTTF* due to electromigration based on Black's electromigration equation [9][10]:

$$MTTF_{EM} = A_{EM}\left(J - J_{crit}\right)^{-n} e^{\frac{E_a}{k_B T}} \quad (3)$$

with A_{EM} is an empirically determined constant, J is the current density in the interconnect, J_{crit} is the critical current density required for electromigration, E_a is the activation energy for electromigration, k_B is Boltzmann's constant, T is absolute temperature in Kelvin, and n is an empirical constant. It can be concluded that during the system's runtime the main driving forces for electromigration are high currents which lead to high current densities and high temperatures.

Gate oxide breakdown means the formation of a conducting path between the gate and the substrate or source/drain, respectively [11]. The breakdown can be based on abrupt events, e.g. Electro-Static Discharge, or on destruction over time known as Time Dependent Dielectric Breakdown (TDDB). The latter is due to an autocatalytic loop in which overlapping charge traps create a conducting path between gate and substrate (or source/drain) which leads to increased current flow and heat dissipation. Consequently, thermal damage occurs and more charge traps are created. This positive feedback loop results in an accelerated breakdown and finally in a defect transistor [12]. Following from experimental work performed at IBM [8][13] the mean time to failure due to TDDB can be modeled as:

$$MTTF_{TDDB} \propto \left(\frac{1}{V_{DD}}\right)^{a-bT} e^{\frac{X+\frac{Y}{T}+ZT}{kT}} \quad (4)$$

where V_{DD} denotes the supply voltage, and a, b, X, Y as well as Z are fitting parameters. In [8][13] following values were determined for the fitting parameters $X = 0.759$ eV, $Y = -66.8$ eVK, $C = -8.37E{-}4$ eV/K, a = 78, and b = -0.081. It can be concluded that at runtime TDDB depends on the applied voltage level at the gate and the temperature.

Negative Bias Temperature Instability (NBTI) is a performance degrading failure mechanism observed mainly in PMOS transistors since they usually operate with negative gate-to-source voltage. This temperature-activated effect occurs when a voltage stress is applied to the transistor gate. The consequence of NBTI is a significantly increase of the transistor threshold voltage V_{th} and following higher delays and leakage currents of the affected integrated system. The physical reasons for NBTI are hole trapping in pre-existent oxide traps and the creation of interface states [14]. Thereby, the interface trap generation $N_{it}(t)$ which leads to a linear increase of V_{th} can be expressed with [15]:

$$N_{it}(t) = 1.16\sqrt{\frac{k_f N_0}{k_r}}\left(D_H t\right)^{1/4} \quad (4)$$

where the mobile diffusing species are assumed to be neutral H atoms. N_0 is the concentration of initial interface defects, D_H is the corresponding diffusion coefficient, and k_f and k_r are constant dissociation rate and self-annealing rate, respectively. When the device is in recovery phase, k_f becomes zero, and k_r is unchanged. In summary, at runtime NBTI depends on temperature and the applied gate voltage.

C. Power Gating with Sleep Transistors

The application of sleep transistors for power gating is one of the most effective methods to reduce standby leakage [16][17][18]. A sleep transistor is referred to either a high threshold voltage PMOS or NMOS transistors which are used as switches to disconnect power supplies from design modules during standby mode (see Fig. 1). Thereby, the sleep transistors create a virtual power (PMOS) and/or a virtual ground (NMOS). That means in theory, during standby all leakage currents of the gated module are zeroed. It should be noted that even when all sleep transistors are switched off a small leakage component exists. This is mainly based on sub-threshold leakage of the sleep transistors [16].

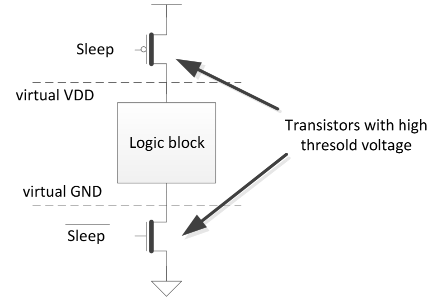

Figure 1. Design module with sleep transistors

In recent years several strategies regarding sizing, placement, and activation of sleep transistors were developed [18]. However, a profound analysis of these techniques is outside the scope of this work. It can be concluded, though, that the application of sleep transistors is a well-known and widely used approach as for instance in current high-end processors [19].

D. Redundancy

Triple Module Redundancy (TMR) is a technique to increase the reliability of integrated designs. Thereby, a calculation is executed with three instances of the same module. In case of different results a subsequent voter chooses the one which is most probable correct. Under the assumption of an ideal voter and a constant failure rate of all instances the reliability of a module implemented with TMR follows from:

$$R_{TMR}(t) = 3R_{mod}(t)^2 - 2R_{mod}(t)^3 \quad (5)$$

with R_{mod} is the reliability of the module. Based on (2) the MTTF of the very same module is:

$$MTTF_{TMR} = \int_0^\infty \left(3e^{-2\lambda_{mod}t} - 2e^{-3\lambda_{mod}t}\right)dt = \frac{5}{6} MTTF_{mod} \quad (6)$$

where λ_{mod} is the failure rate of the module, and $MTTF_{mod}$ is the mean time to failure of the module. It can be see that TMR reduces the mean time to failure and cannot be considered as technique to increase the expected lifetime of a system.

A more theoretical approach is parallel module redundancy (PMR) with an ideal voter with inherent error detection. Again, the module is implemented with several instances. However, in this case the voter is capable of detecting which module produced the wrong result. That means this approach works already with two instances. Under an assumption of an ideal voter the MTTF of a circuit realized with PMR results from:

$$MTTF_{pmr} = \frac{1}{\lambda_{mod}} \sum_{i=1}^{N} 1^{-i} = MTTF_{mod} \sum_{i=1}^{N} 1^{-i} \quad (7)$$

with N is the number of instances. A closer analysis reveals that a second instance increases $MTTF_{pmr}$ by solely 50 % while three instances result in a $MTTF_{pmr}$ which is only 83,3 % longer compared to the circuit with one instance – at an increase of area and power dissipation of more than factor 3. This behavior can be explained by the fact that at all time all instances suffer under the same failure mechanisms previously described.

Major drawbacks of module redundancy, including TMR and PMR, are the multiplication of area and power dissipation, and an increase of the module delay based on the delay of the voter.

III. APPROACH

This section introduces the new approach. Further, required additional logic is discussed.

A. Basic Idea

A notable characteristic of power gating with sleep transistors is the fact that the gated circuit can be almost completely disconnected from the power supply. Hence, in the disconnected state the gated circuit is nearly without any inherent currents and voltages. Additionally, the zero activity of the circuit reduces its temperature. Thus, in standby the three major parameters reducing the lifetime of integrated circuits are eliminated, or at least strongly reduced. Following, the mean time to a failure is extended approximately by the time the circuit is in standby. One way to extend the standby time is to improve the related algorithms. However, in designs with a high activity, as in streaming applications, medical environments, etc., the potential to extend the standby time is strongly limited [18]. Thus, our proposed approach applies another way to extend the standby time of a gated module – *redundant implementation*. Thereby, each gated module is implemented at least two times. At runtime, only one of these instances is active while the others are disconnected from the power supply. In the ideal case, i.e. any additional control logic is omitted and the circuit is completely disconnected from the power supply, the resulting MTTF of the module follows from:

$$MTTF_{STmr} = \sum_{i=1}^{N} MTTF_{mod} = N \cdot MTTF_{mod} \quad (8)$$

with N is the number of instances. That means, for two instances and under ideal conditions the proposed approach doubles the MTTF. Compared to an ideal implementation of parallel module redundancy (PMR) the presented technique results in a MTTF which is 33 % higher. For four instances the improvement compared to PMR increases to 92 % which is already very close to the theoretical maximum of 100 %.

It should be noted that the proposed technique is not limited to designs with high activity. In other words, the MTTF can be reduced also in systems with long standby periods in which all blocks are disconnected from the power supply. The resulting equation for the MTTF under ideal conditions is:

$$MTTF_{STmr,Ia} = N \cdot \left(\frac{MTTF_{mod}}{1 - p_{standby}} \right) \quad (9)$$

with $p_{standby}$ is the percentage amount of time the system is in standby.

An additional advantage of the proposed approach is the extremely low increase of power dissipation. This follows from the fact that in theory at a given time at most one instance is active.

B. Additional Logic

The main problem of the proposed approach is to ensure that the subsequent logic blocks receive the correct input data, i.e. the data from the currently active instance. This can be guaranteed by additional multiplexer. The latter are placed in front of the inputs of the logic blocks following the gated module and multiplex the outputs of all instances (see Fig. 2).

Usually, power gated logic requires some clock cycles as wake-up time [18]. Hence, it is not recommended to connect the signal controlling the sleep-transistor directly with the multiplexer's control signal. The ensure data consistency a clock scheme similar to Fig. 3 should be applied. The picture shows the control signals for the sleep transistors of a module with two instances (Sleep 1, Sleep 2) and the control signal for the multiplexer (MUX-ctrl). At time t0 instance 2 is active while instance 1 is in standby. At time t1 instance 1 is changing to its active state. However, the multiplexer still forwards the outputs of instance 2. At time t2 instance 1 is fully active and the multiplexer starts to forward the outputs of instance 1. Finally, at time t3 instance 2 goes into standby. The same

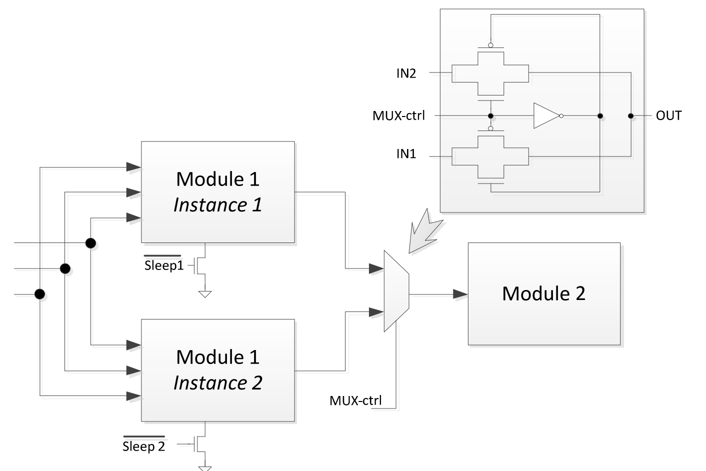

Figure 2. Multiplexer insertion to ensure data consistency and multiplexer realized with transimission gates

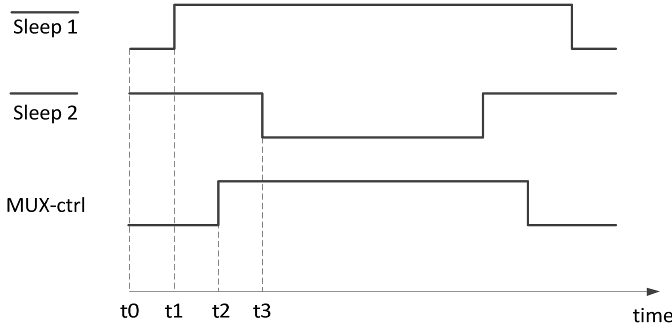

Figure 3. Clock scheme for standby signals and muliplexer control (two instances)

scheme is applied when instance 2 is returning to its active state while instance 1 is going to standby.

It has to be observed that the expected lifetime of the system also depends on the MTTF of the multiplexer. Fortunately, multiplexer realized as transmission gates (see Fig. 3) have only one active path while the others are disconnected. Thus, in the inactive paths lifetime degrading failure mechanisms like electromigration, TDDB, and NTBI are reduced. Nevertheless it is recommended to apply special design strategies for the multiplexers, like transistors with thicker gate oxide [20] and wider wires.

IV. VERIFICATION STRATEGY

The simulation of effects that deteriorate the circuit's characteristics is a common problem of verification of reliability enhancing techniques. This task is complicated if time-dependent effects shall be taken into consideration. In this section, we propose a possible solution for this problem.

A. Modeling of Failure Mechanisms

Several models for failure mechanisms in integrated designs can be found in the literature [7][8][10]. Thereby, spice simulations produce the most accurate results. Thus, we decided for this kind of analysis although it can require immense simulation times which limit the maximum number of elements of the analyzed designs.

Models applied for reliability simulation on transistor level can be grouped in two categories – (1) models based on electronics components, i.e. transistors, resistors, etc., and (2) models based on equations. Examples for category (1) can be found in [21] where the TDDB is modeled with transistors and resistors and in [8] where electromigration is modeled with resistors and capacitors. The second category includes

Figure 5. Example (incl. HSpice code) for modeling of varying gate width based on algebraic expression

transistor aging models extracted from tools like Cadence BSIMPro+ or as described in [22]. Another solution is the application of voltage controlled voltage sources (VSCS) or current sources (VCCS) to model the transistor behavior [23].

All above listed approaches simulate the circuit behavior at a certain time, e.g. after 7 years runtime. Thus, it is possible to analyze the design performance after a given time but not its modification *during* the aging process. Though, for some application the latter might be interesting, e.g. for the prediction of the mean time to failure of a circuit. Hence, our proposal is the extension of the models applied in both previously described categories by controllable elements which are varied during simulation. For the following description the term device means a part of the actual design, like a transistor or a capacitor. In contrast, the term element is related to parts of the device model and can be an electronic component or a parameter of an expression. We identified three possible techniques for the implementation of adjustable elements – (I) voltage or current controlled active or passive components, e.g. voltage controlled voltage sources (VCVS) or voltage controlled resistors (VCR), (II) on variables based algebraic expressions for circuit device parameters, and (III) models extended by VerilogA or VHDL-AMS descriptions. The first technique requires that the time-dependent behavior of the reliability model of the circuit device can be emulated by an inherent voltage or current source or an inherent passive element, respectively. At simulation time, the value of this inherent element is varied via a voltage or current source (see example in Fig. 4).

The second technique demands the identification of device parameters which suffer under time-dependent failure mechanisms. That can be the threshold voltage of a transistor or the resistance of an interconnection. At simulation time, the identified parameter is varied via a current or voltage source (see Fig. 5).

The third technique for the realization of adjustable elements is comparable to the both previous ones. The difference is that the element or even the whole device is realized in a hardware description language which includes analog and mixed-signal extensions, e.g. VerilogA or VHDL-AMS. These languages allow a more complex emulation of the

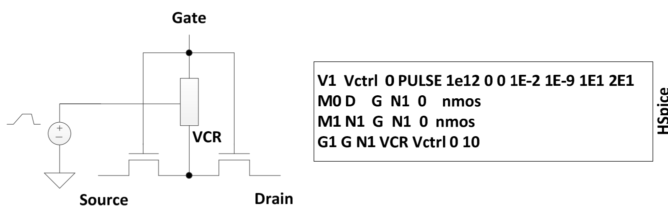

Figure 4. Example (incl. HSpice code) for simple modeling of TDDB with a voltage controlled resistor

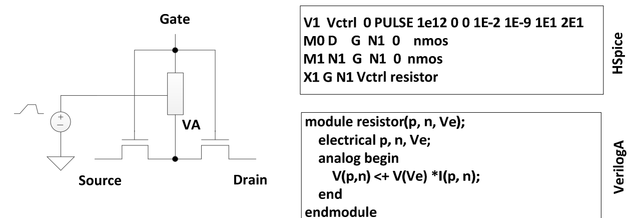

Figure 6. Example (incl. HSpice and VerilogA code) for simple modeling of TDDB with a resistor described in VerilogA

behavior of the circuit device. However, this solution can increase the simulation time. As in the both former techniques a voltage or current sources is used to adjust the device degradation (see Fig. 6) [24].

B. Verfication Flow

The basic architecture of the test environment is similar to common mixed-signal verification structures. The input signals of the Design Under Tested (DUT) are generated by a digital circuit written in VHDL-AMS or VerilogA. Further, the outputs of the DUT are connected to a digital control block which verifies the correctness of the results and determines the time of the first wrong calculation. The devices of the DUT are based on modifiable models as described in the preceding subsection. During simulation the degradation of these devices is controlled via a voltage source. In addition, for each device input a signal probability value is estimated which is used for the TDDB modeling. Thereby, we consider the fact that TDDB depends on the absolute voltage level at the gate (see section 2). For instance, if no voltage is supplied to the gate of an NMOS (gate voltage $V_g = 0$), there is no electric field and TDDB does not occur. On the other hand, if V_g = VDD an electric field and TDDB are present and the $MTTF_{TDDB}$ is smaller compared to the general case with equal input probability. The same applies for PMOS, but with inverse voltage levels — the critical case is $V_g = 0$. Beside this, we also estimate for each logic cell output an activity value as activity is directly related to currents which in turn are directly related to electromigration (see section 2). These calculated activity and probability values are also of interest for the modeling of NBTI (see section 2). All values are inserted as additional factors into the applied device models.

Hence, the final flow is as follows:

1) Synthesis of the design which shall be analyzed
2) Extracting of maximum clock frequency, desired MTTF, signal probabilities and activities
3) Conversion into a Spice netlist whereas the applied devices are based on modifiable models
4) Insertion of degradation factors which follow from signal activity and probability
5) Insertion of a pulsed voltage source with a slope resulting from the desired MTTF
6) Compilation of input signal generation and error verification blocks
7) Simulation of the DUT until the first error occurs

V. SIMULATION RESULTS

In this section we present the configuration of the test environment and discuss final simulation results.

A. Test Environment

All simulations were executed with designs of the ISCAS testbench suite [25] which we implemented in a predictive 22 nm technology [26]. Device degradation is simulated by a TDDB and an electromigration model. That means each transistor is implemented with the simple TDDB model depicted in Fig. 4 whereas a voltage controlled resistor is applied (VCR). Electromigration is modeled with a VCR at the output of each gate. We are aware that very basic models have been used which only permit limited predictions. Nevertheless, these models still allow an elementary evaluation of the proposed approach.

The multiplexer are implemented based on transmission gates (see also Fig. 2). However, we generate the inverted control signal externally to spare the internal inverter. Further, all digital blocks, i.e. input signal generation and error detection, are implemented in VerilogA. The generation of these blocks, the instance duplication, the sleep transistor and multiplexer insertion, and the clock frequency estimation is done by a self-written tool. This tool also halves the degradation factor of each device if a redundant counterpart for its logic cell exists.

B. Results

In a first attempt, each design was realized as initial version without redundant blocks and as version with instance duplication. Thereby, the design components were grouped into two modules which have separated sleep transistors. The clock scheme of the sleep transistor control follows the proposal in Fig. 3 whereas the wake up time is set to one clock cycle. Further, we adjusted the slope of the external voltage source so that the expected MTTF of an initial design is around 300 clock cycles. Then, each design configuration was simulated 100 times.

The first simulations revealed a MTTF increase of an average factor of 2.8. This is considerably higher than expected. It can be explained with - (I) delay and maximum output voltage of logic cell do not degrade linearly under presence of TDDB, and (II) the difference in clock frequency of the design versions. The former means that the extension of the active time by a certain factor reduces the deterioration by a slightly higher factor [27]. Reason (II) follows from the increase of the delay due to the additional multiplexers which results in a lower clock frequency and, thus, relaxed delay constraints. To omit this factor we simulated all initial designs

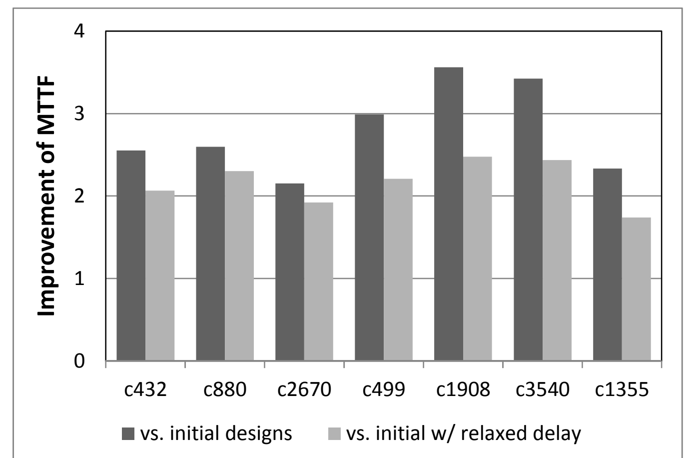

Figure 7. Improvement of MTTF of several ISCAS designs if the proposed approach is applied. The results are compared to initial designs with and without relaxed delay constrainst.

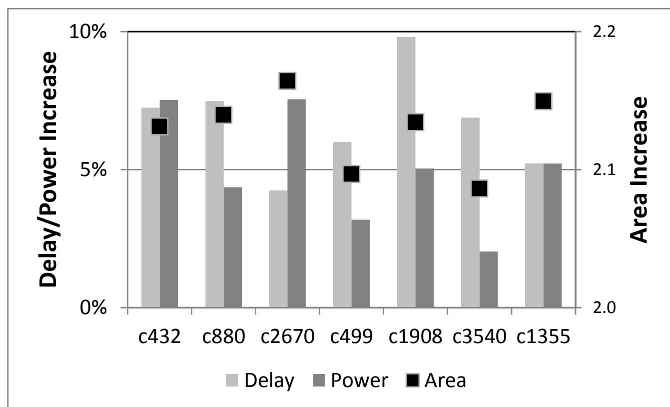

Figure 8. Increase of delay, power (bars) and area (points) of the modified ISCAS designs

with the same clock frequency as its counterparts. As result, the improvement of MTTF reduced to an average factor of 2.2.

Fig. 7 shows the improvement of MTTF due to the proposed approach for all simulated designs. The delay and area penalties are depicted in Fig. 8. The mean area increase is approximately 2.1 while the maximum frequency of the designs decreased in average by 7 %. The increase of power dissipation compared to the initial versions with reduced clock frequency is in average 5 %. That means the relation between area increase and expected lifetime improvement is approximately 1.4 for initial designs and slightly more than 1 for initial designs with relaxed delay. These results are considerably better than the ideal value of 0.75 for parallel module redundancy (see section 2).

VI. CONCLUSION

The progressing susceptibility of nanometer technologies against severe failure mechanisms elevates techniques which extends the lifetime reliability to a main concern in today's integrated circuit design. The presented work relates to these needs and proposes an approach that combines the idea of redundancy and the well-established sleep transistor technique to increase the expected lifetime of an integrated system. Further, we propose an extended verification flow which allows the analysis during time-depended deterioration of design components. Simulations show promising results as the proposed approach could increase the mean time to failure (MTTF) in average by factor 2.2 with a slight power and delay penalty and an approximately doubling of the area.

Future works should relate to the application of more detailed error models and selective redundancy algorithms to enhance the relation between delay and area increase and MTTF improvement [20].

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