HotAging — Impact of Power Dissipation on Hardware Degradation

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Motivation

On chip power dissipation → increases temperature

(Almost) all aging mechanism depend also on temperature

HotAging - How does power dissipation impact circuit degradation over time (*aging*)?

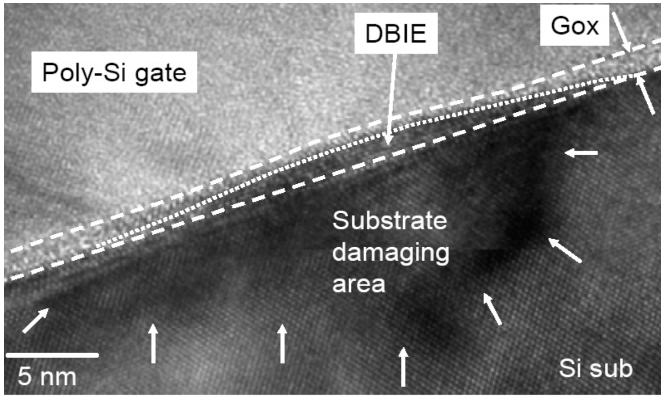
Outline

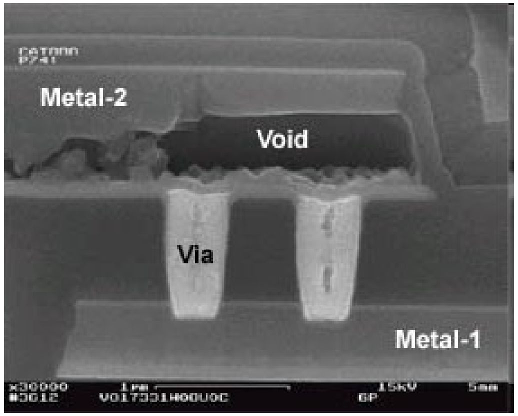
- Aging Mechanism
- Analysis Environment
- Results
- Conclusions

Aging

- Bias Temperature Instability (BTI)
  - Electric field over oxide leads to accumulation of ‘traps’ into silicon-oxide interface → v_{th} increase
- Time-Dependent Dielectric Breakdown (TDDB)
  - Tunneling current through gate oxide generates path from oxide to channel → v_{th} increase
- Electromigration
  - Transport of material caused by gradual movement of ions in wires

→ *delay* increase

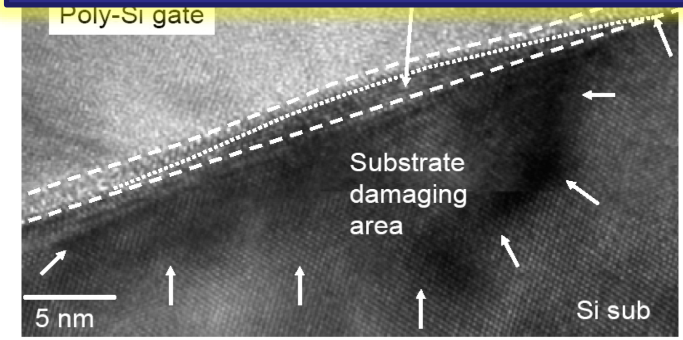


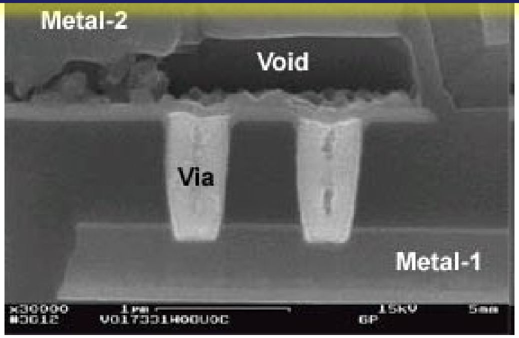


Aging

- Time-Dependent Dielectric Breakdown (TDDB)
  - Tunneling current through gate oxide generates path from oxide to channel → V_{th} increase
- Bi
  - con-
- El
  - ires

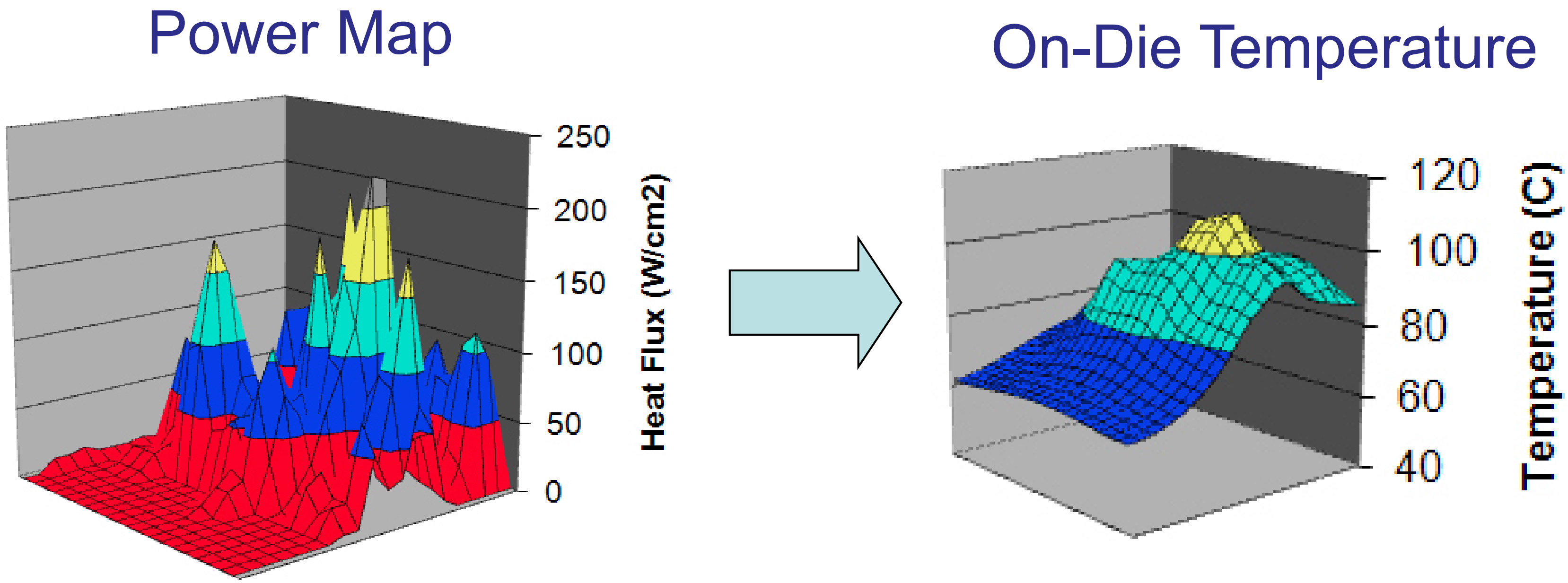
Acceleration due to higher Temperature





Power and Temperature

- Power dissipation can be directly related to temperature



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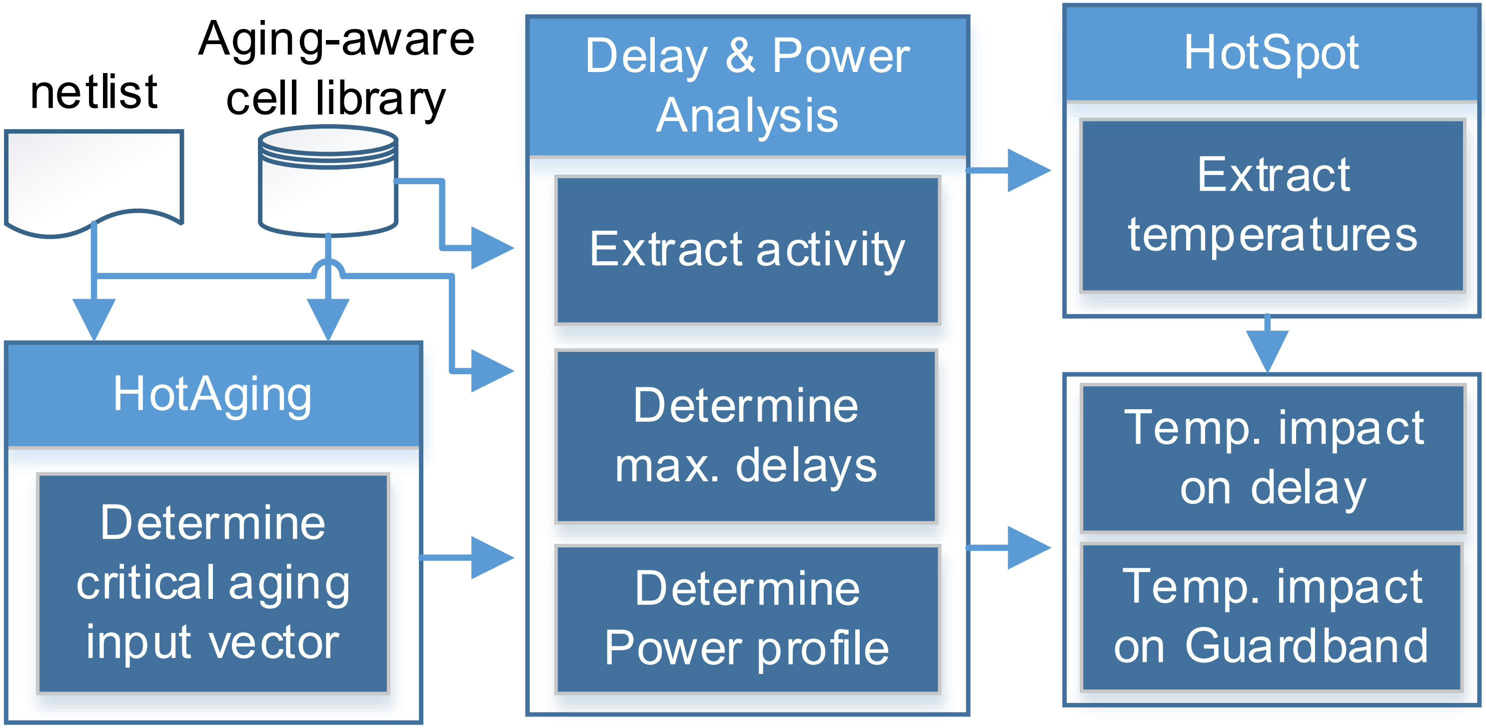
HotAging

- Principal analysis flow



netlist

Aging-aware cell library

HotAging

Determine critical aging input vector

Delay & Power Analysis

Extract activity

Determine max. delays

Determine Power profile

HotSpot

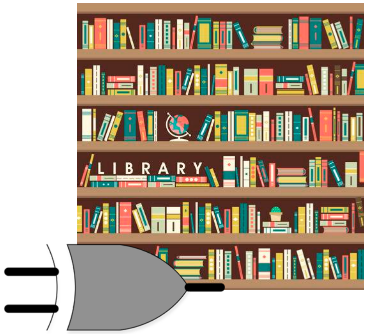
Extract temperatures

Temp. impact on delay

Temp. impact on Guardband

Aging-aware cell library

- Aging analysis on SPICE level
  - Several models with good prediction
  - High flexibility in terms of aging parameters
  - Supported by EDA tools (e.g. Eldo, MOSRA, RelXpert)
  - Inapplicable for designs > 1000 devices
- Analysis on cell level
  - No support by industry
  - Lower flexibility in terms of aging parameters
  - Lower accuracy
  - Applicable for >1M devices



Aging-aware cell library

- Principal flow
  - Based on (freely available) 45nm technology and cell library (FreePDK)
  - BTI aging simulated via its impact on threshold voltage v_{th} and mobility μ
  - Considered BTI factor: stress/recovery time via input duty-cycle
  - All parameters taken from literature
  - All cell characterized for with Cadence Liberate / SPECTRE
  - *Note: temperature impact considered in later step*

Aging-aware cell library

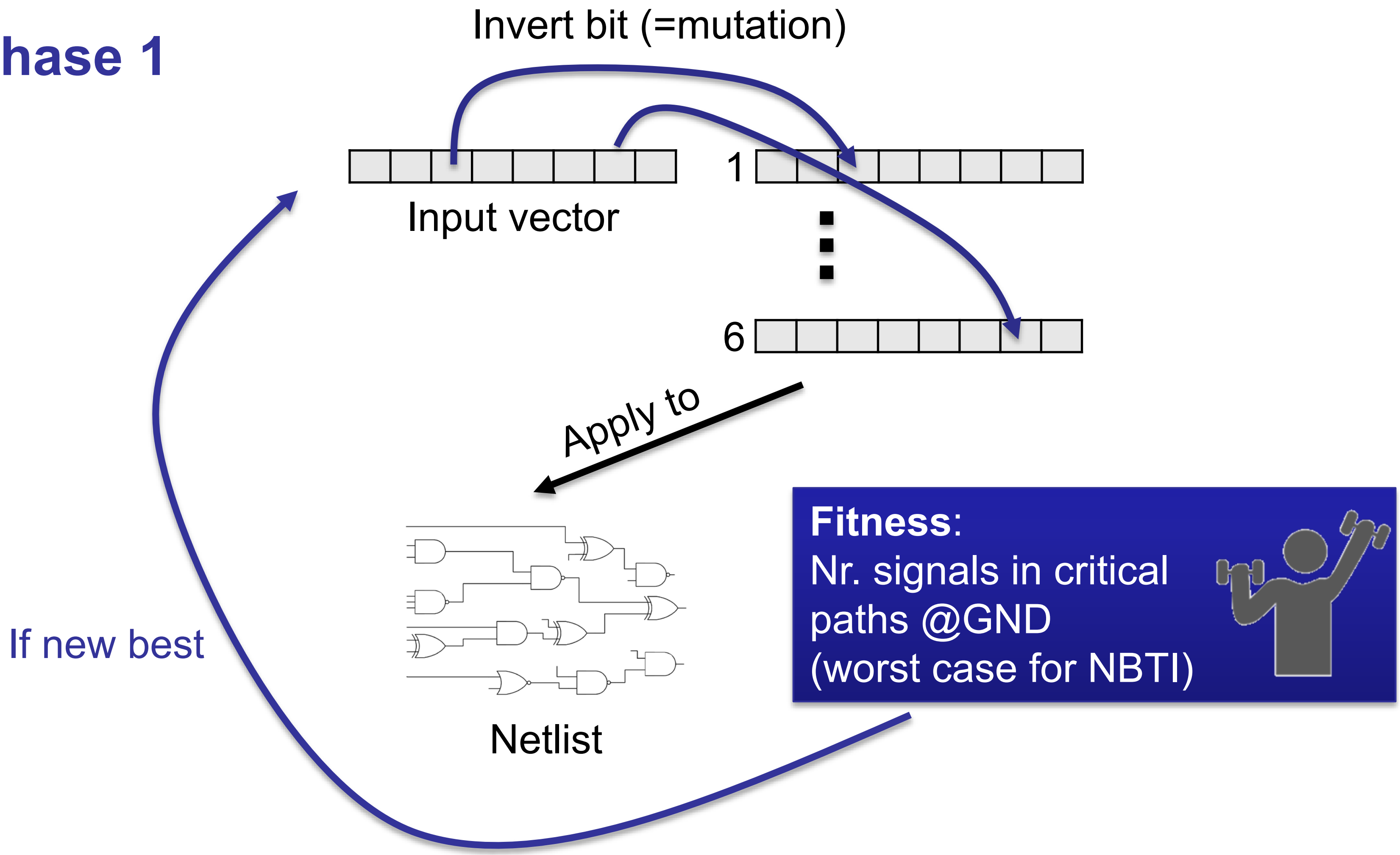
- Aging aware characterization
  - Duty-cycle (dc) varied in steps of 10% for all cell inputs → each cell with 11 (1 input) and 121 (2 inputs) versions for different combinations of input signal probabilities
  - 17 cells (comb/seq)
- Example:
  - INV1 with 40% dc: INV1_40
  - NAND2 with 1st input 20% dc and 2nd input 70% dc: NAND2_20_70

Hot-Aging Algorithm

- Observations
  - Many aging mechanism are data-dependent
  - Power dissipation is data-dependent
- Question: What would be a critical combination of input vectors for maximum aging and power dissipation?
- Hot-Aging algorithm
  - Genetic algorithm
  - Two phases:
    1. Determination of critical aging input vector
    2. In the following: determination of critical power input vectors

Hot-Aging Algorithm

Phase 1



Invert bit (=mutation)

Input vector

Apply to

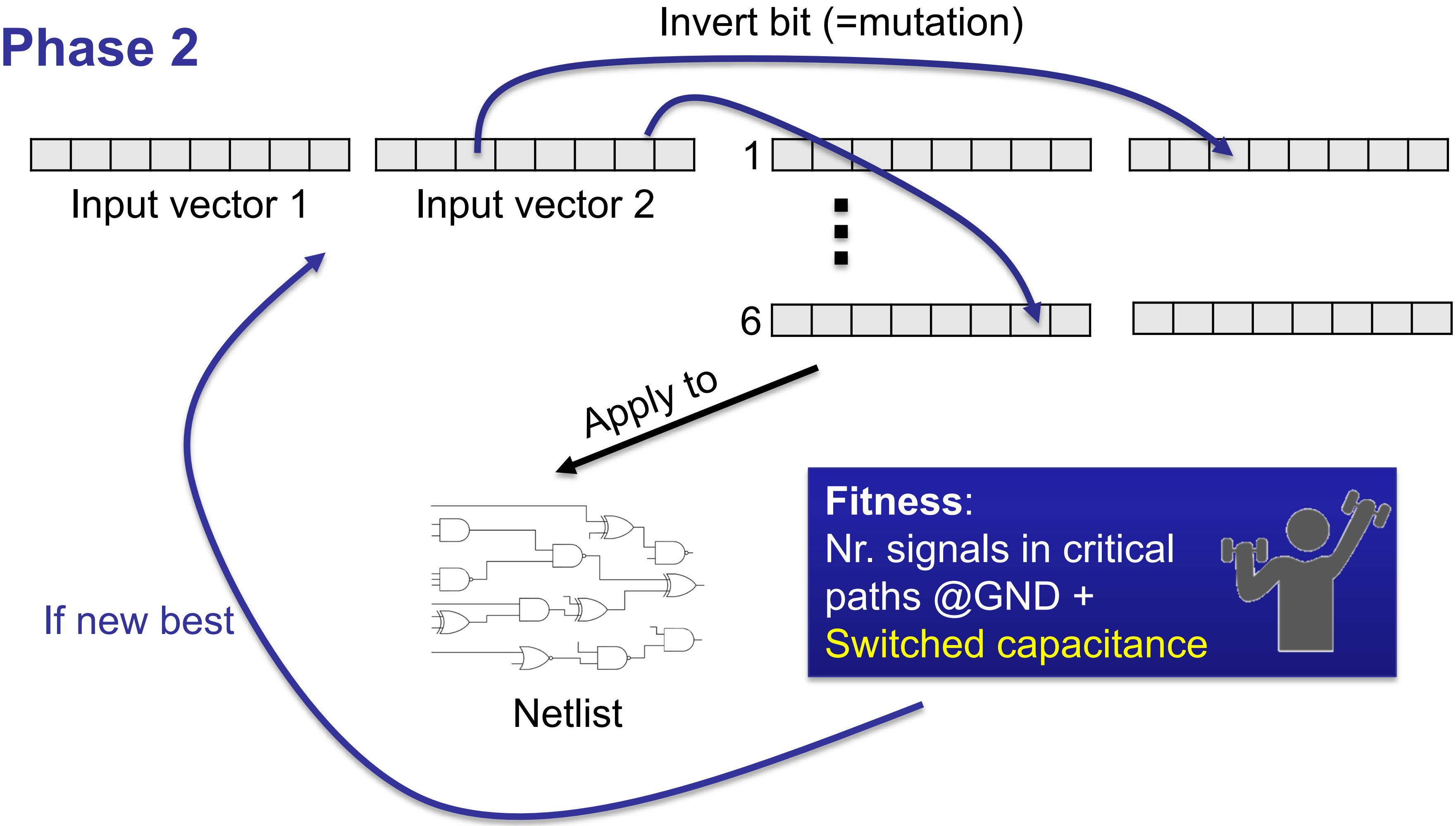
Netlist

Fitness:
Nr. signals in critical paths @GND (worst case for NBTI)

If new best

Hot-Aging Algorithm

Phase 2



Fitness:
Nr. signals in critical paths @GND +
Switched capacitance

Consideration of Temp. impact

- Extraction of power dissipation and max. delay via Modelsim and Synopsys DesignCompiler for determined input vectors using aging-aware cell library
- Extraction of temperature via HotSpot
- Temperature-dependent acceleration factor:

$$AF_{BTI}^{T_{op},T_0} = \exp\left[\frac{E_{aBTI} \cdot \left(T_{op} - T_0\right)}{k_B \cdot T_{op} \cdot T_0}\right]$$

- With:
  - T_{op} – Actual temperature during operation
  - T_0 – Reference temperature (125°C)
  - E_{aBTI} – activation energy (0.58),
  - k_B – Boltzmann's constant

Consideration of Temp. impact

- Delay dependency (approx.) of v_{th} and μ:

$$t_d \propto \left[\mu^{-2} \left(V_{DD} - v_{th} - \Delta v_{th} \right)^2 \right]^{-1}$$

- Delay increase due to BTI over period of 10 years

$$\Delta t_{d,T_{op}} = \frac{\Delta t_{d,T_0}}{\alpha \cdot t_{d,init}} \left(t_{10} \cdot AF_{BTI}^{T_{op},T_0} \cdot \beta \right)^{\gamma}$$

- With:
  - $\Delta t_{d,T0}$ – Delay degradation if operated at T_0 for 10 years
  - $t_{d,init}$ – Pristine delay
  - t_{10} – 10 years
  - α,β,γ – Extracted parameters for chosen technology

Guard-band

- Guard-band (Δt_{guard}): extra delay added to clock against parameters variations (incl. due to aging)
- Extracted model for determining time until delay increase is beyond Δt_{guard}

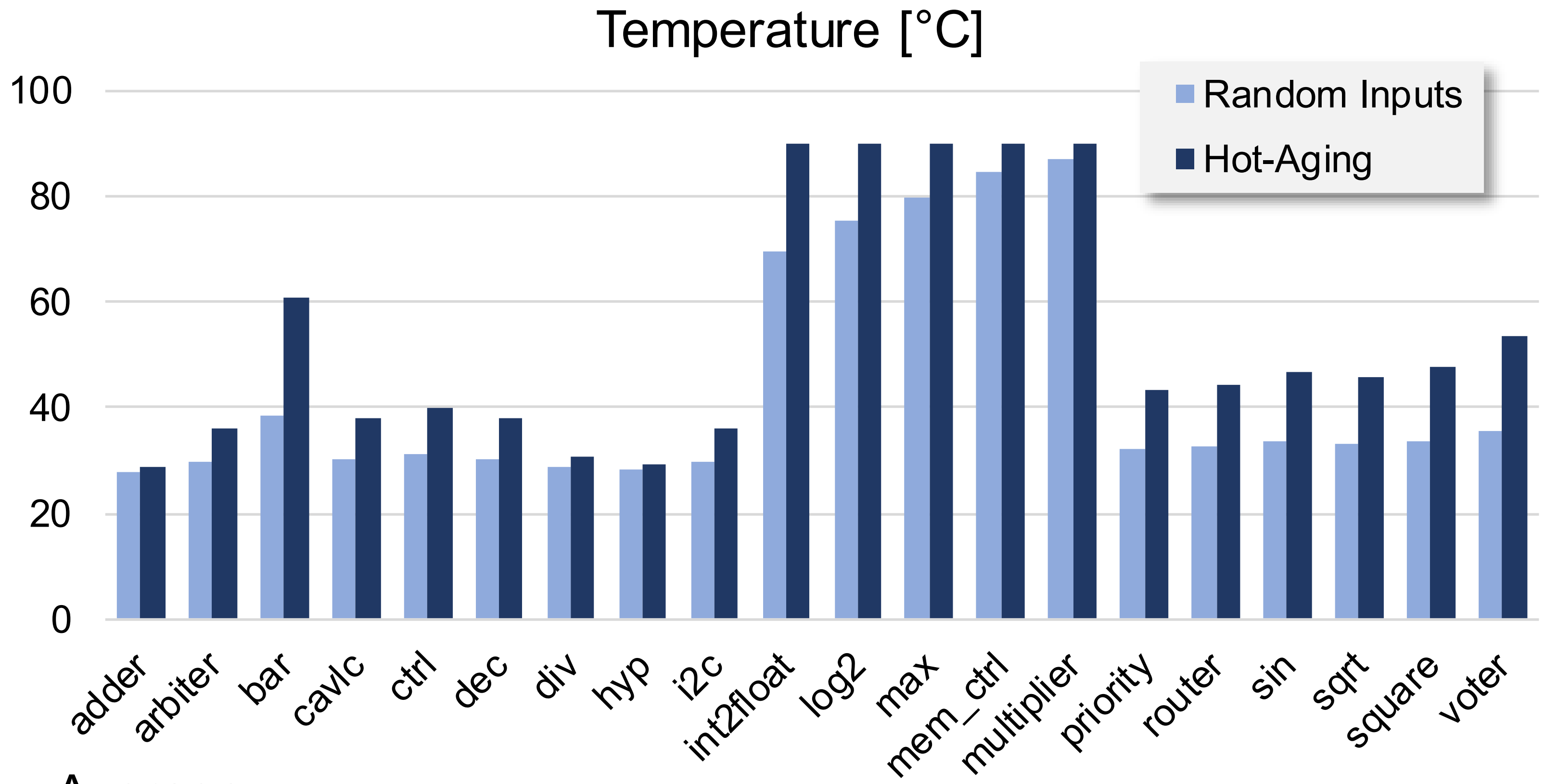
$$t_{age} = \delta \cdot \left(AF_{BTI}^{T_{op},T_0} \right)^{-1} \left(\Delta t_{guard} \frac{\varepsilon \cdot t_{d,init}}{\Delta t_{d,T_0}} \right)^{\varphi}$$

- With:
  - $\delta, \varepsilon, \varphi$ – Extracted parameters for chosen technology

Simulations

- 3 Analyses
  - Aging without and with consideration of temperature
  - Impact on guard-banding
- Input vectors
  - Randomly generated (modeling typical use case)
  - Critical case (GA) (can be malicious or unintentionally)
- Circuits from EPFL benchmark suite

Results – Temp. increase



Average:

- Random inputs increase temperature by 16°C
- Hot-Aging increases temperature by 26°C

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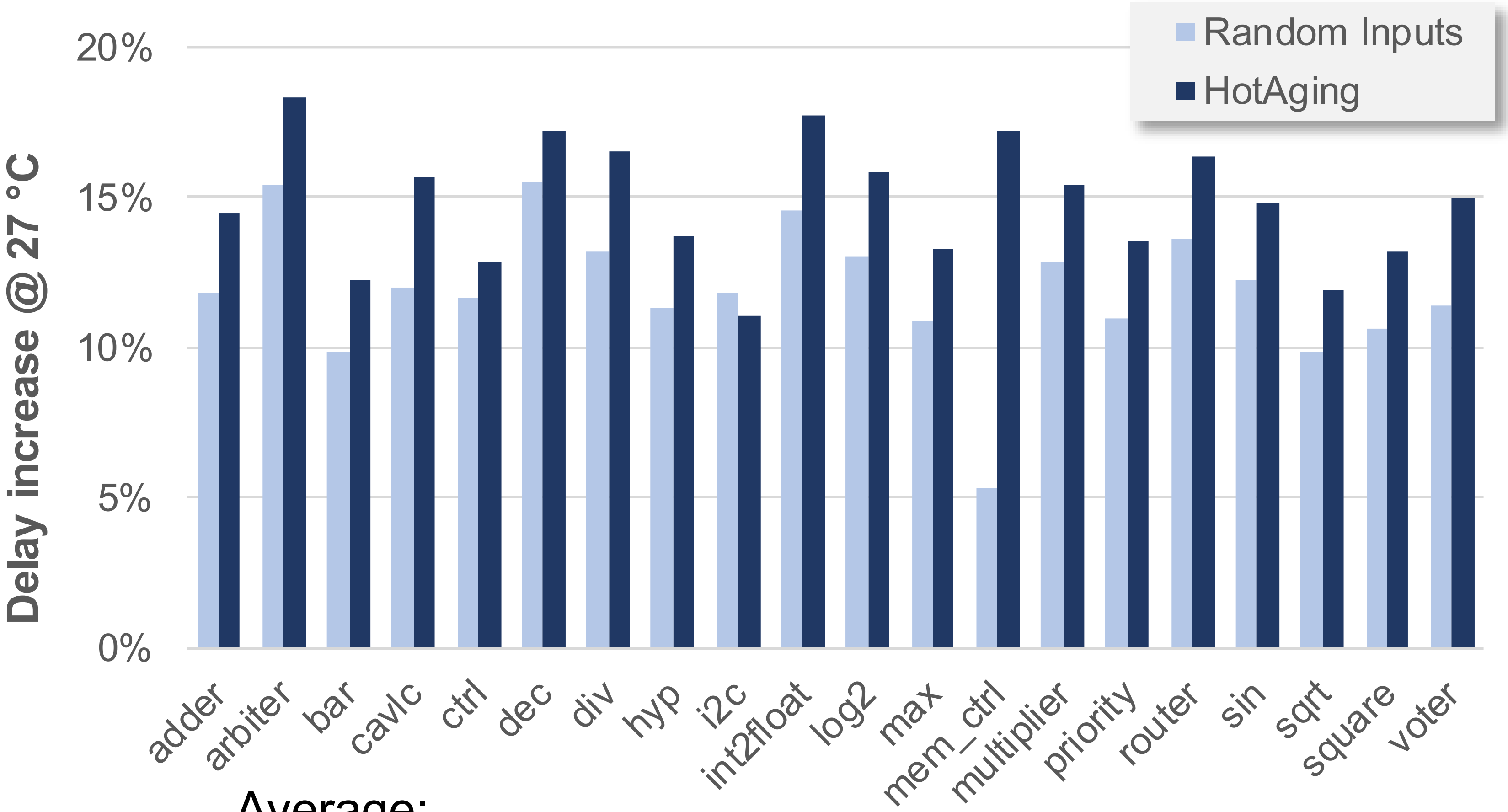
Results – Delay incr. @ 27ºC (10y)



Average:

- Random inputs increase delay by 12%
- Hot-Aging increases delay by 15%

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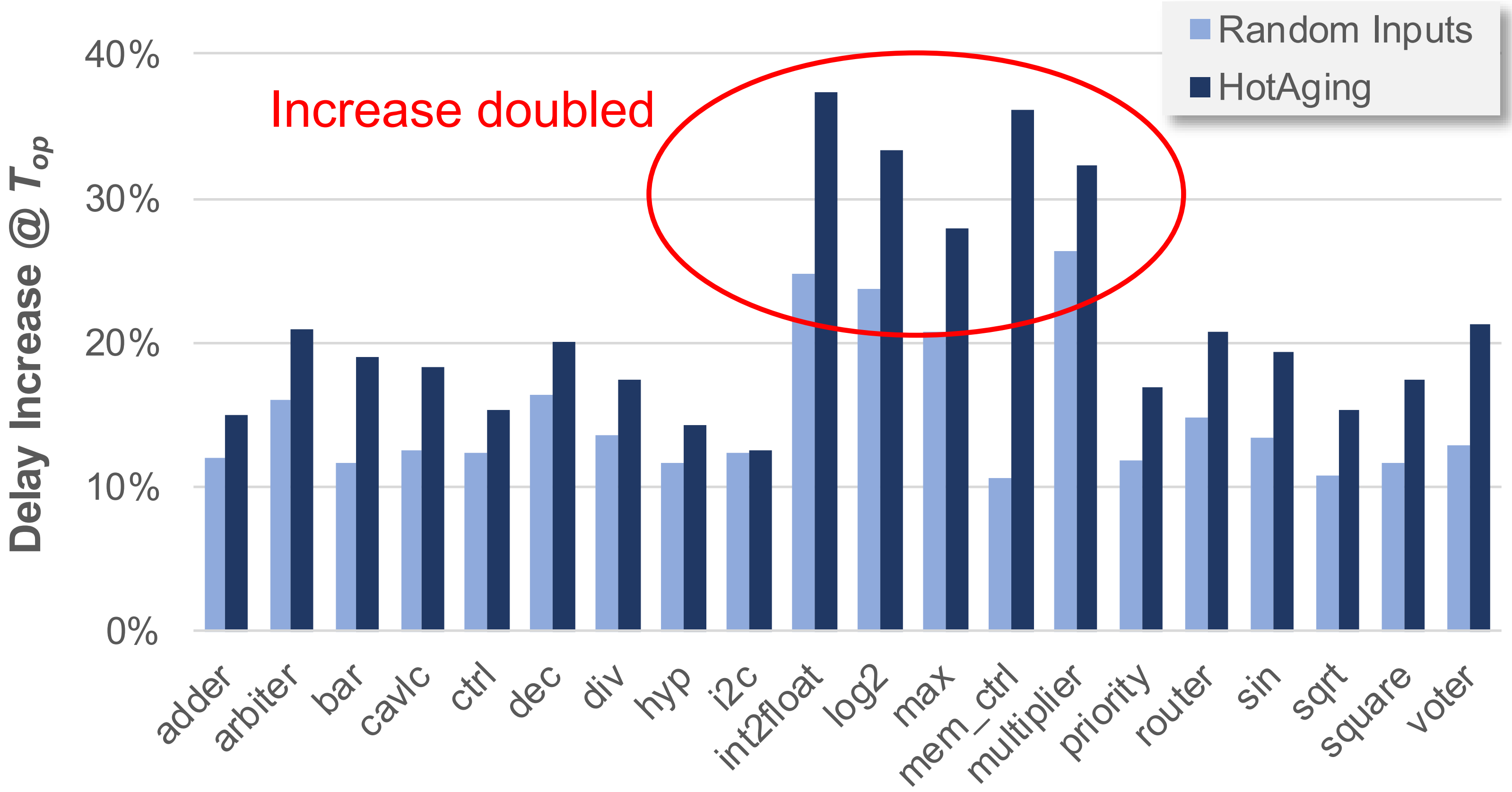
Results: Delay incr. @ T_{op} (10y)



Worst case:

- Random inputs increase delay by 26%
- Hot-Aging increases delay by 40%

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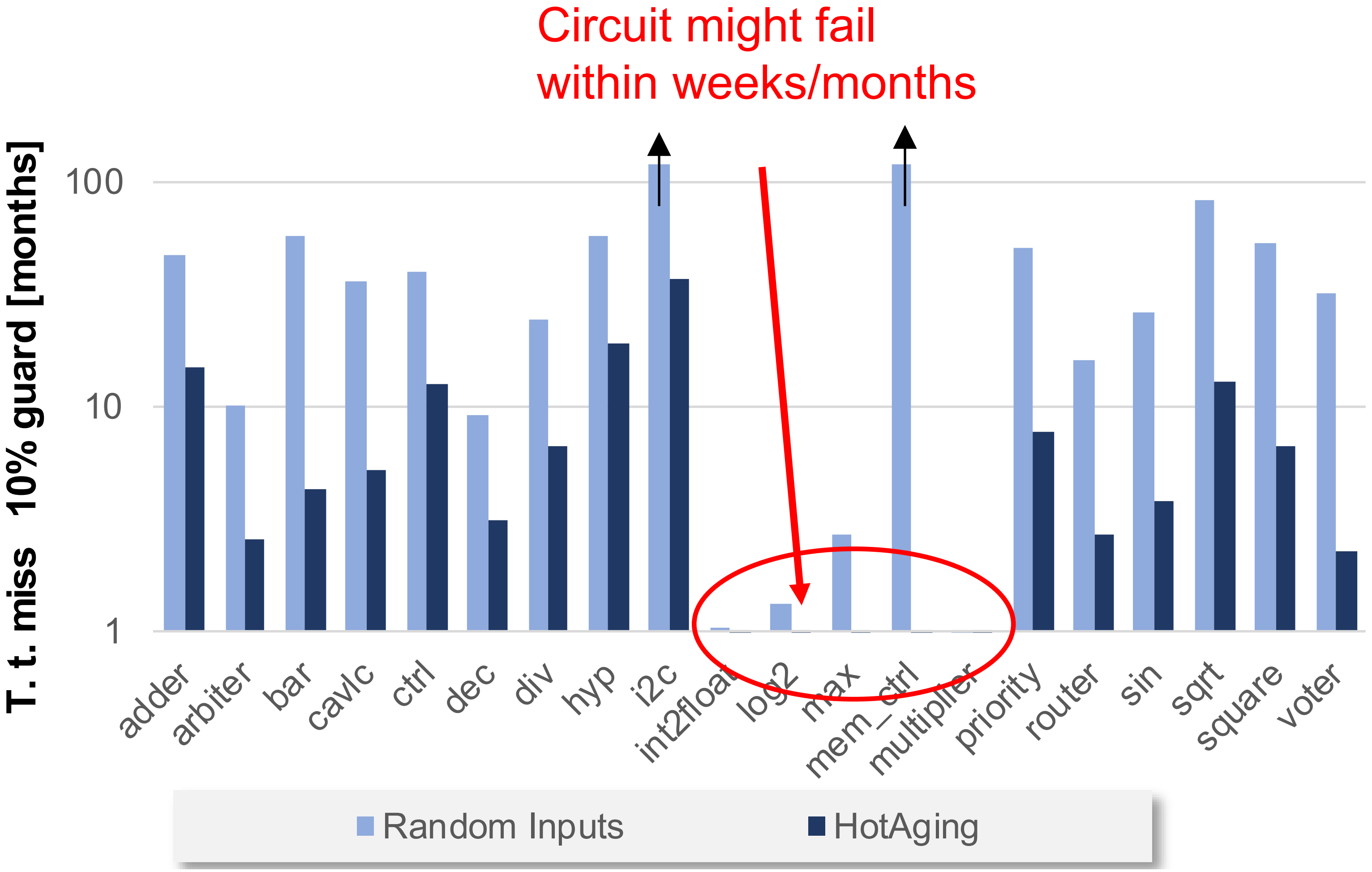
Results: Time to miss 10% guard [months]


Circuit might fail within weeks/months

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Conclusions

- Exploration of relation between hardware degradation and temperature
- Analysis environment
  - Extraction of random and worst case input scenarios
  - Determination of how aging and temperature impact the circuit delay.
- Results indicate
  - If temperature is considered: degradation can increase by more than factor 2
  - If guard-banding is applied: circuits can enter malfunction states within months (random case) or even within weeks (critical case).
- There is a need for appropriate countermeasures

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