SBCCI 2005

18th SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN

CHIP ON THE ISLAND

Total Leakage Power Optimization with Improved Mixed Gates

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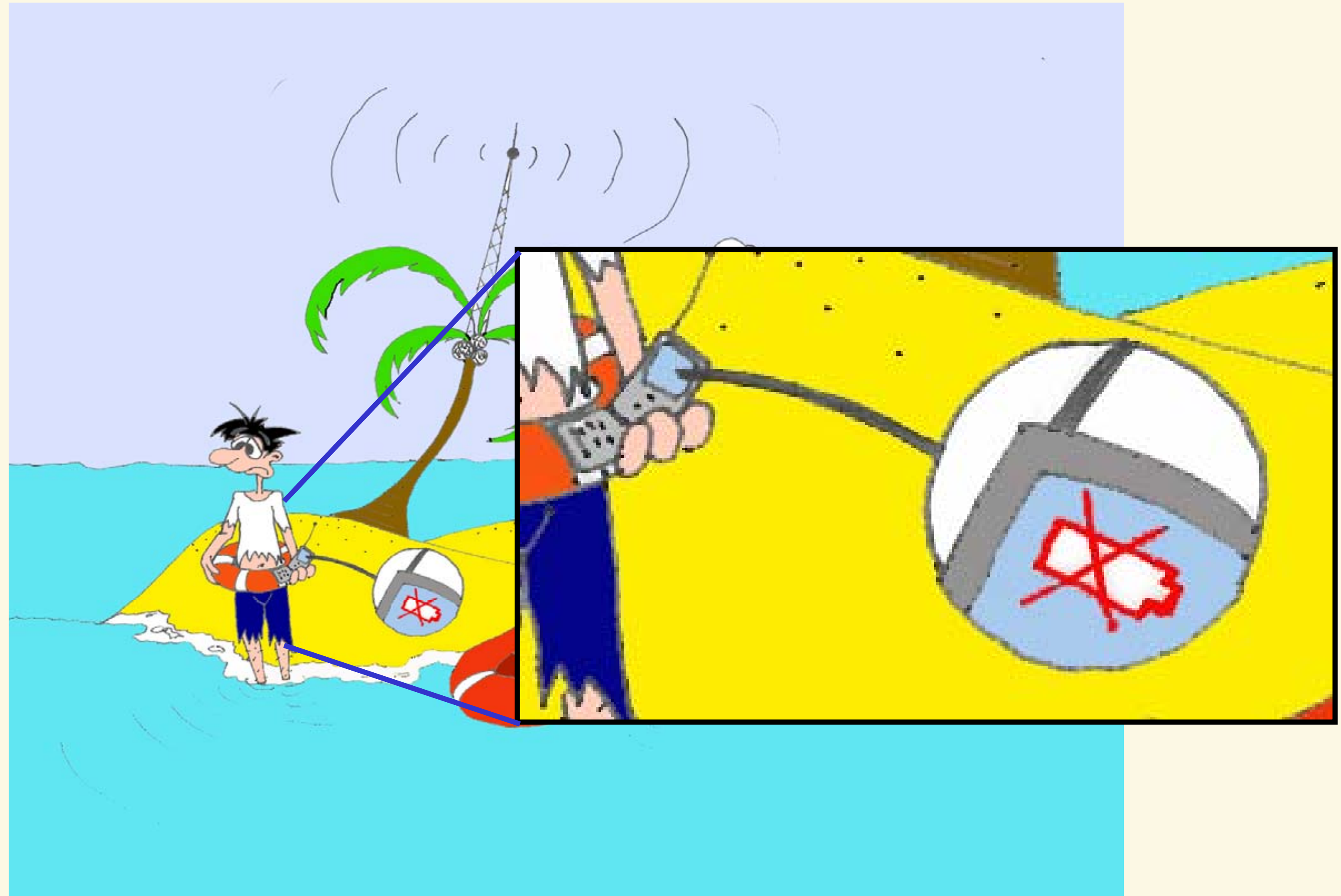
Outline

1. Motivation
2. Basics
3. Improved Mixed V_{th} Gates
4. Modification of Technology Parameters
5. ISCAS – Benchmarks
6. Conclusion

1. Motivation

Why Thinking about Leakage?



Trend: Power

10 mm Die

Power (W), Power Density (W/cm²)

SiO2 Lkg
SD Lkg
Active

1400
1200
1000
800
600
400
200
0

90nm 65nm 45nm 32nm 22nm 16nm

S. Borkar, ‘05

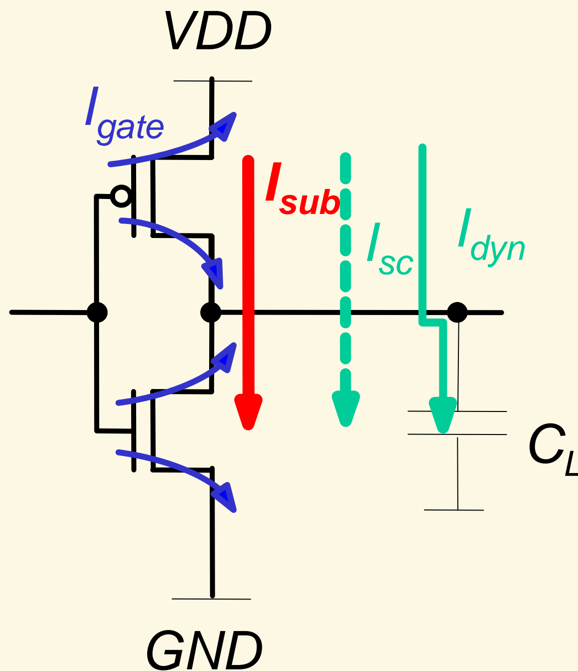
Focus of this Work

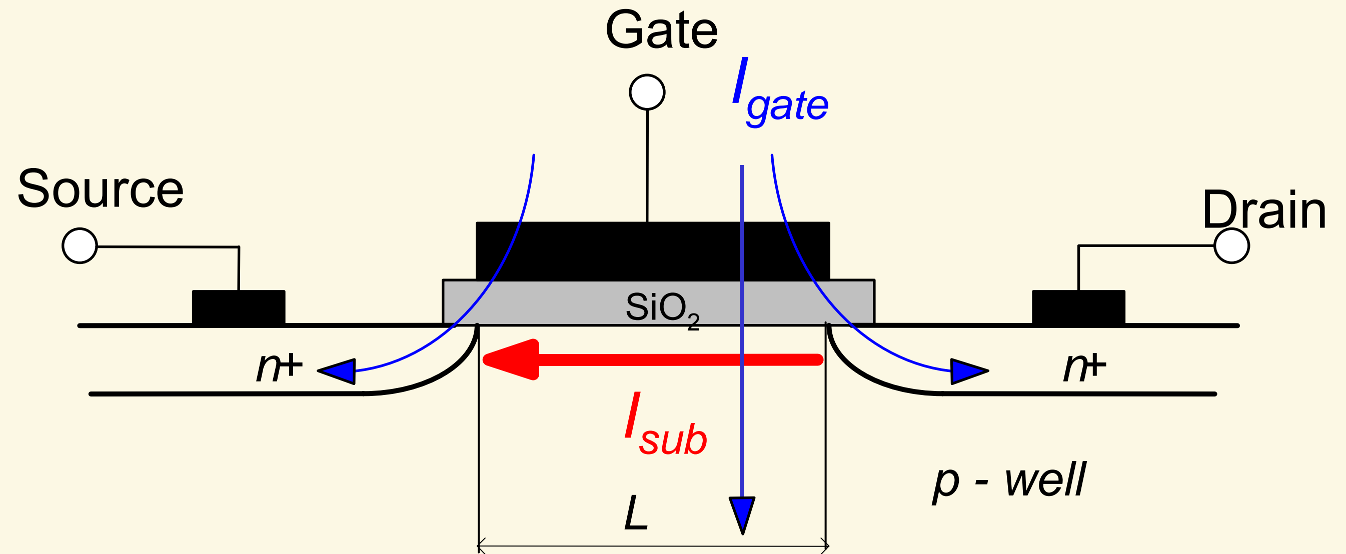
1. Modification of established Leakage Reduction Approach (DTCMOS)

2. Analysis to determine significant technology parameters

2. Basics

Power Dissipation in CMOS





- I_{sub} occurs if $V_g < V_{th}$
- carriers move by diffusion along surface
- I_{gate} caused by direct tunneling through gate oxide

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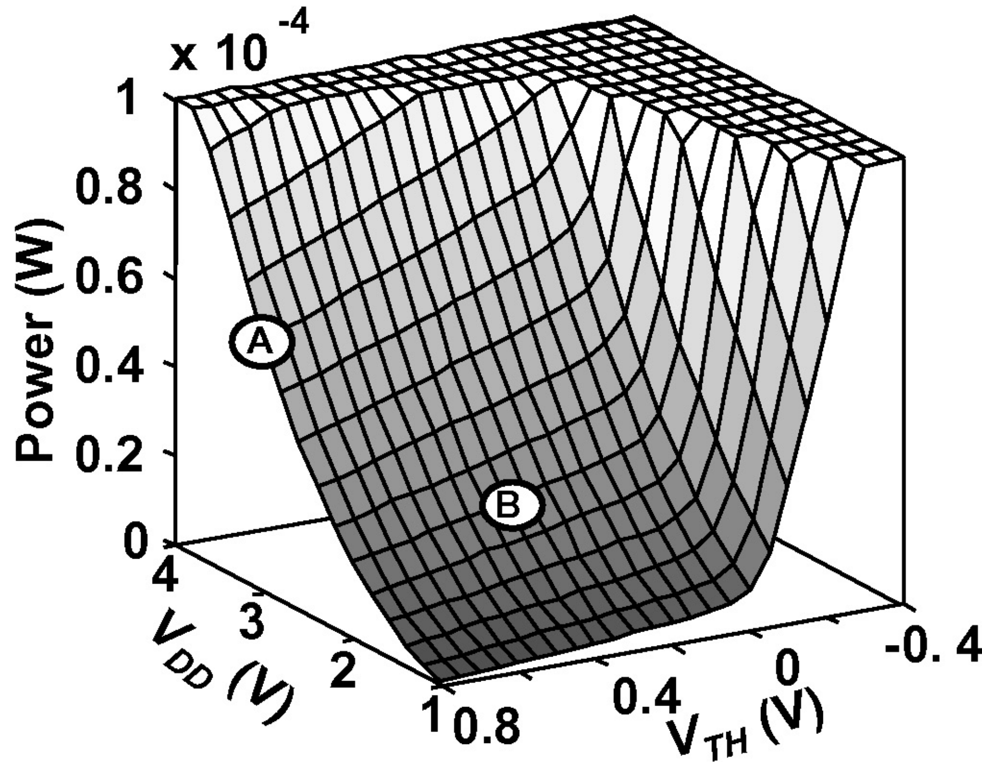
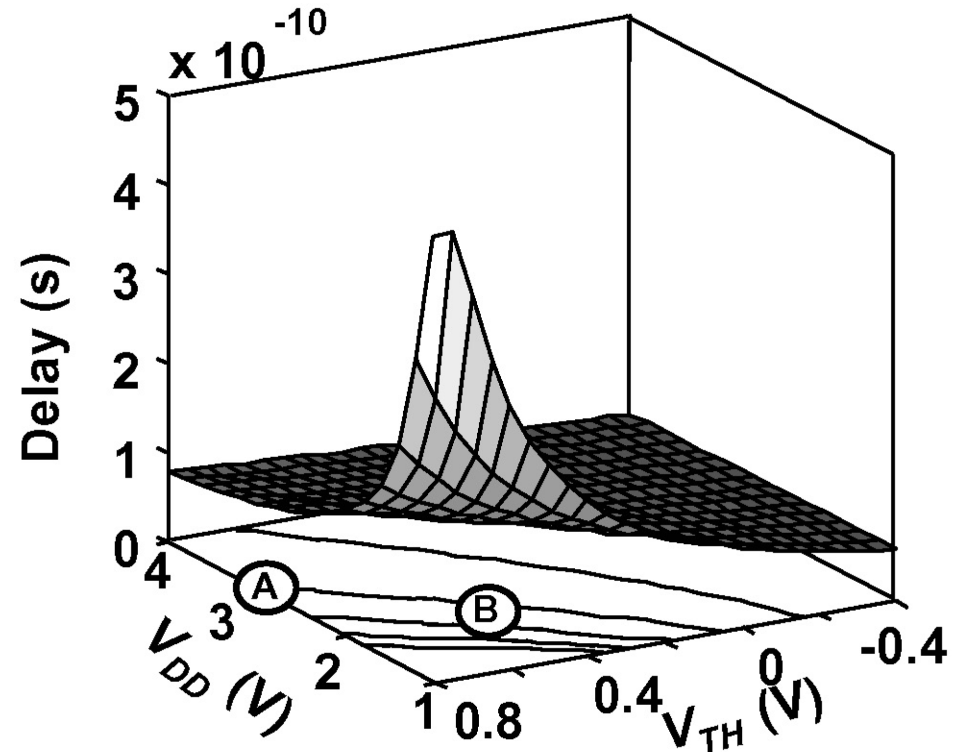
Power & Delay Dependence

$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^{\;2} + I_0 \frac{W_T}{W_0} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

w.o. gate leakage





Sakurai, ‘01

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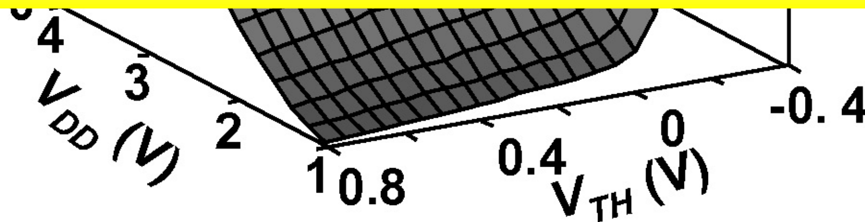
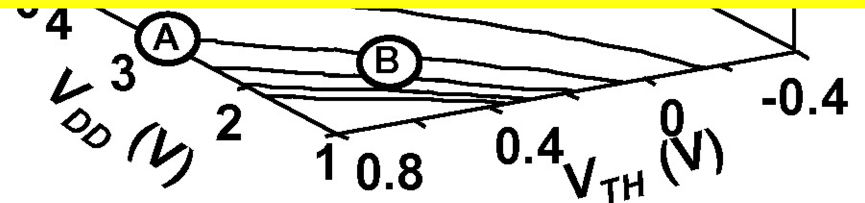
Problem:

fast transistors with high power dissipation (low V_{th})

or

slow transistors with low power dissipation (high V_{th})





Sakurai, '01

Dual Threshold Voltages (DTCMOS)

- Use different V_{th}'s
  - use lower threshold for devices on the critical paths
  - use higher threshold for devices off the critical paths
- Decrease power without performance penalty
- Approaches at:
  - Gate level (V.Sundararajan, et al., LPED'99)
  - Transistor level (L.Wei, et al., DAC'99)

3. Improved Mixed V_{th} Gates

Mixed-V_{th} Pull-*Down/Up*-Paths

Goal (for fast gates): keep the delay while leakage decreases

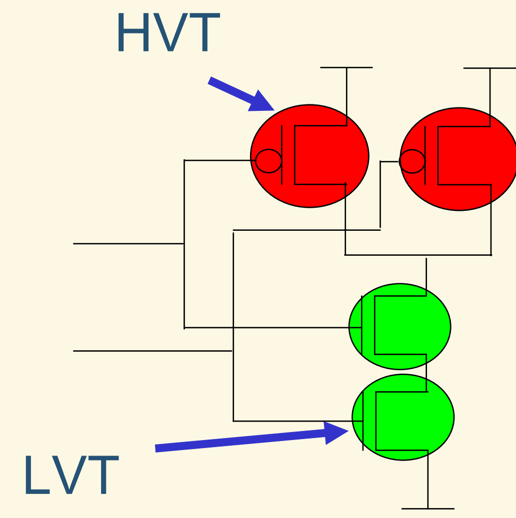
if all transistors in gates are dimensioned regularly

(= PMOS and NMOS have same resistance)

→ different output slopes

up to now: sizing of transistors

idea: use different threshold voltages within a gate to adapt the slopes

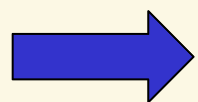


Mixed Stacks

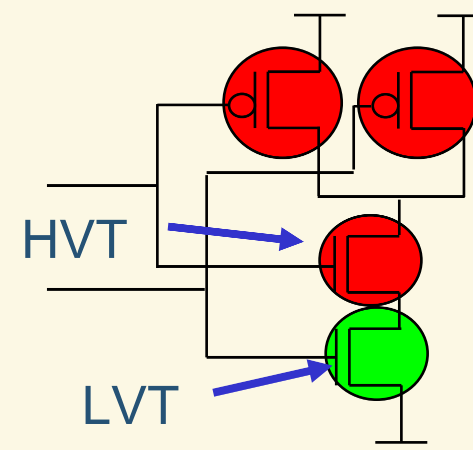
Goal: additionally gate types at constant mask count

only two gate types in DTCMOS at gate level (HVT, LVT)

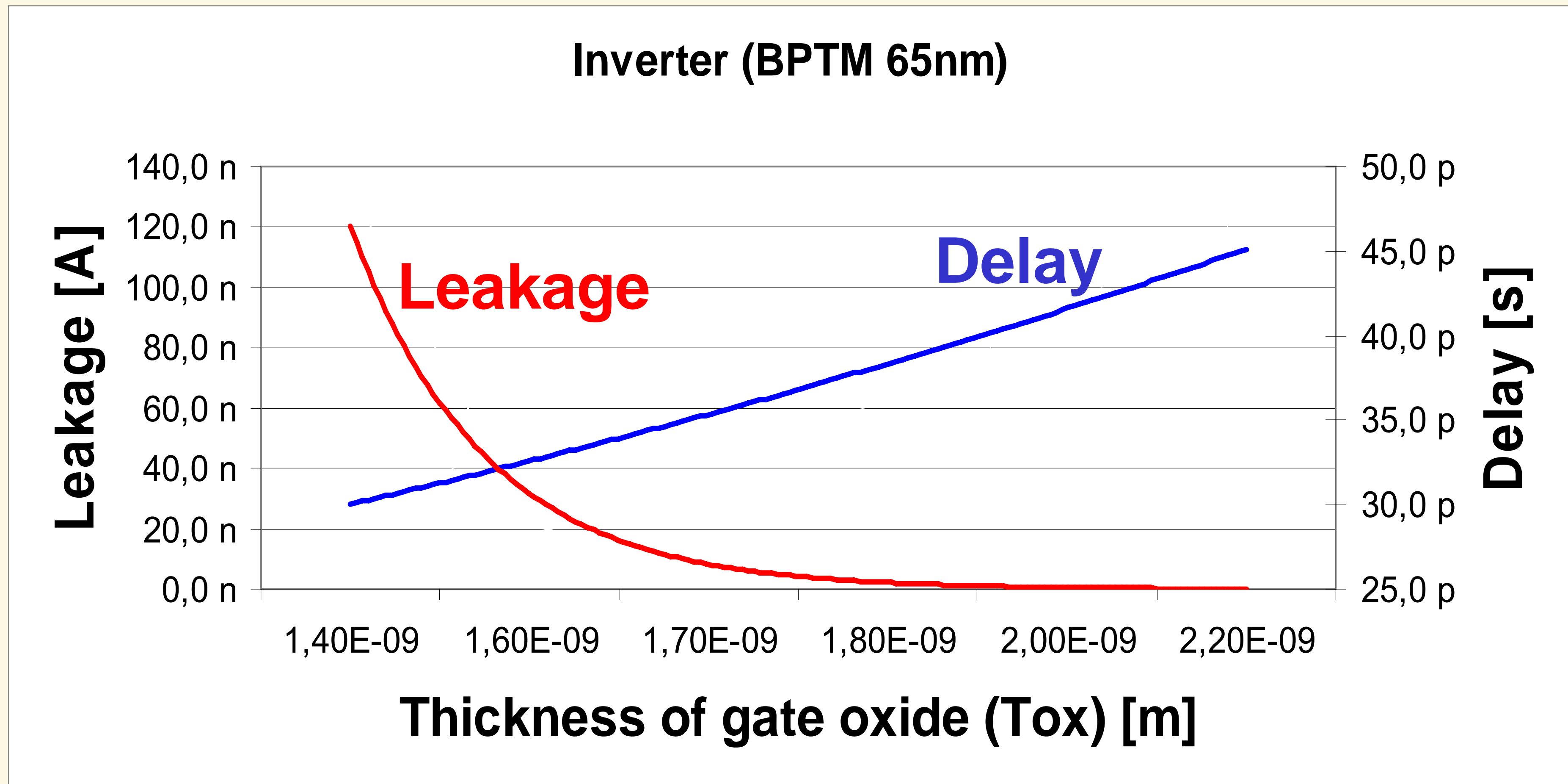
→problem: more LVT gates after optimization as needed to keep the delay



idea: mixed threshold voltages within a gate (stack & Pull-up/Pull-down path)



T_{ox} vs. Delay and Leakage



Improvement

1. Transistors with different V_{th} **AND** T_{ox}

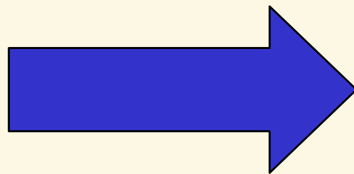
2. Pin – Reordering after gate type assignment

4. Modification of Technology Parameters

Modified Parameters

BPTM 65nm: predictive technology

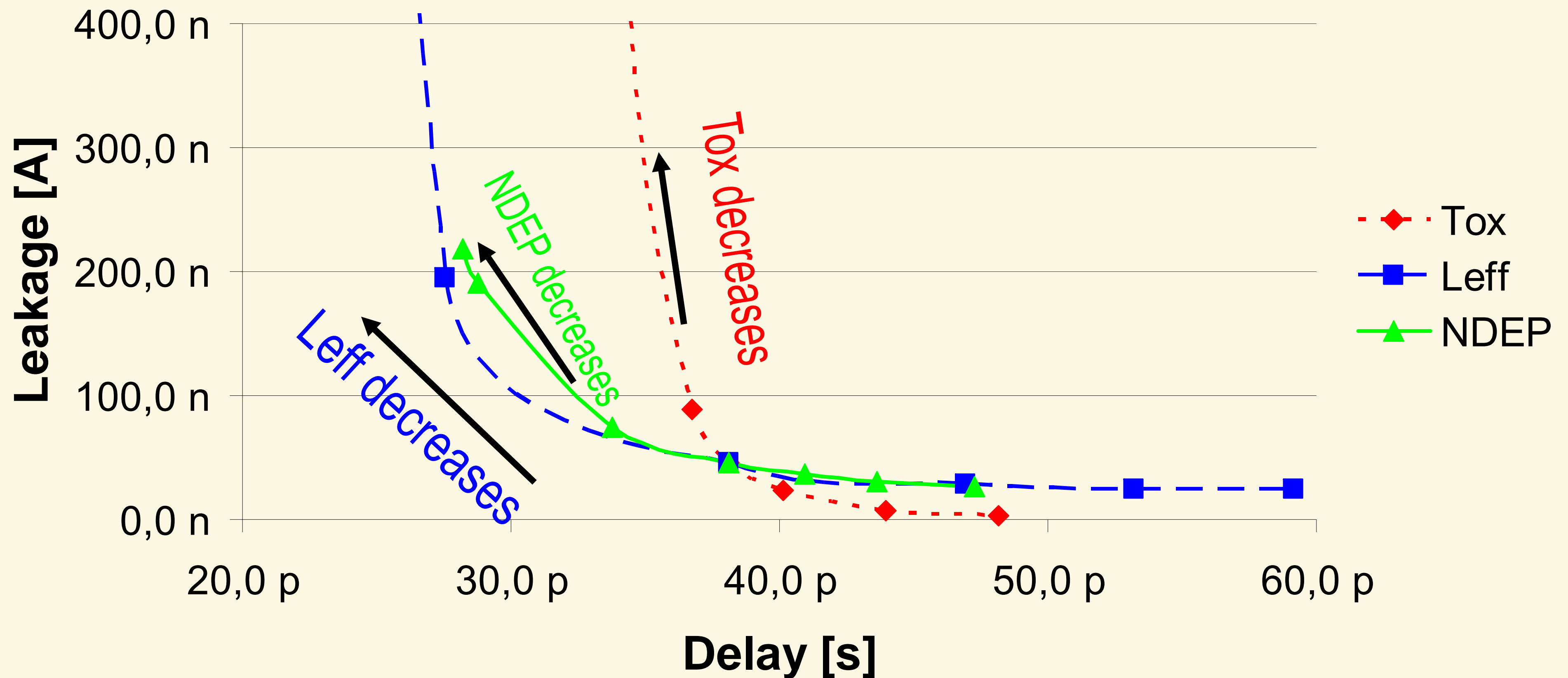
L_{eff}: effective gate length
T_{ox}: thickness of gate oxide layer
NDEP: channel doping concentration



Modification and HSpice Simulation of all parameters

HSpice – Simulation: ***Leakage***

NAND2 (predictive 65nm BPTM-Technology)



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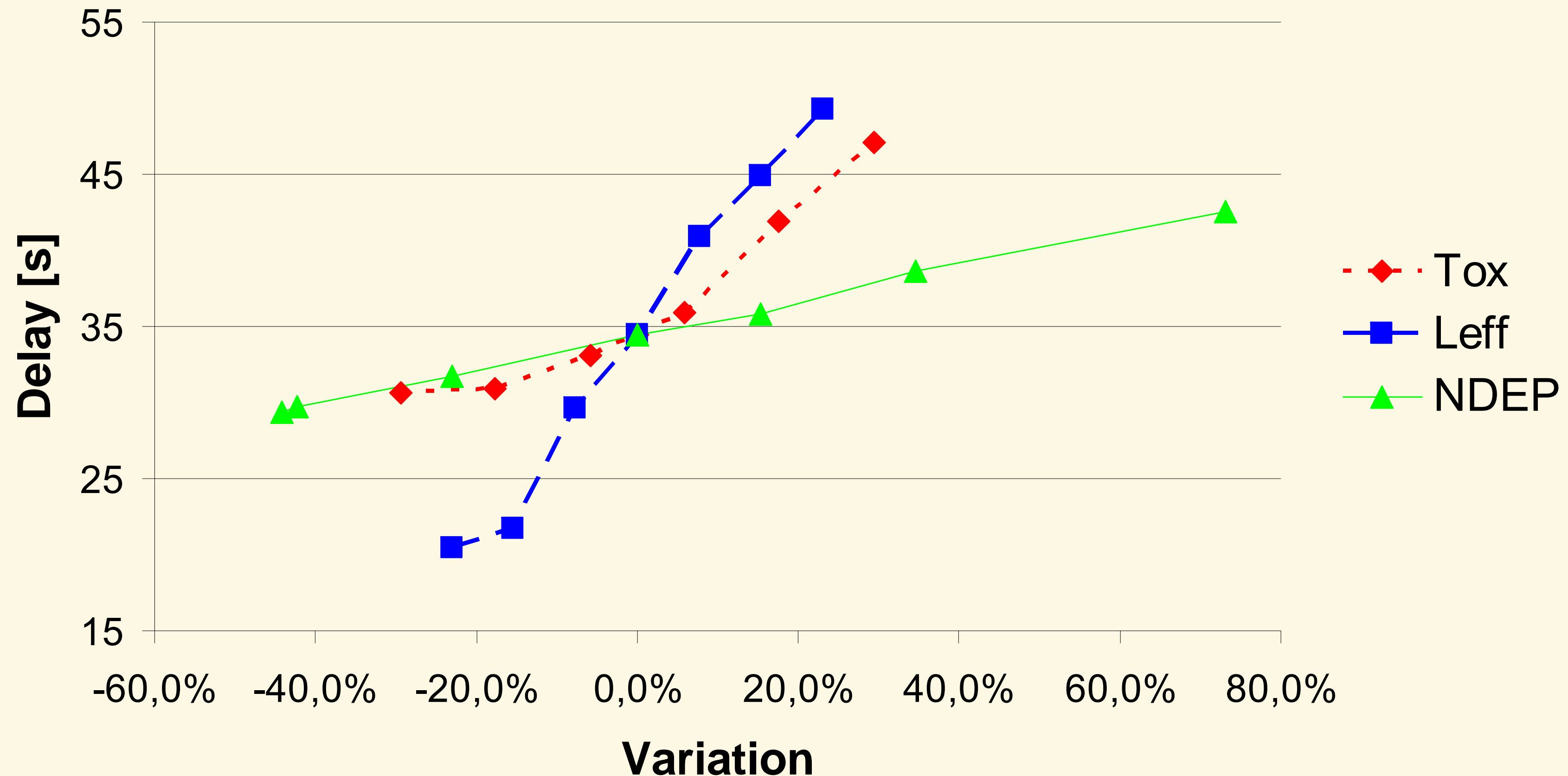
HSpice – Simulation: *Variations*



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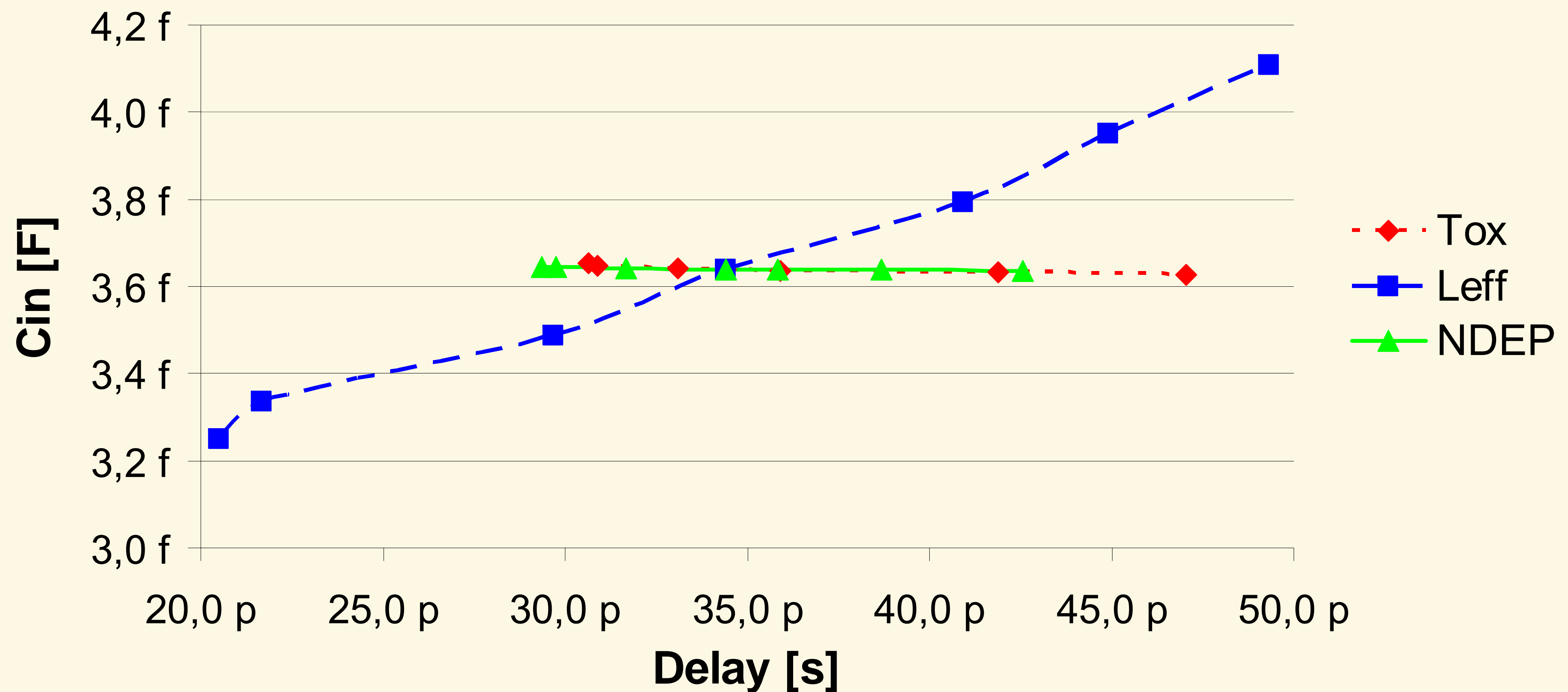
HSpice – Simulation: ***Input Capacity***



Results

- **Increasing of L_{eff}**: *not recommended* (strongly affects C_{in})
- **Reduction of L_{eff}, T_{ox}**: *not recommended* (slightly reduced delay yields drastically increasing leakage)
- **Increasing of T_{ox}, *NDEP***: *recommended* (good tradeoff between delay and leakage)
- **Reduction of *NDEP***: *recommended* (best effect on decreasing delay and leakage, not as strongly affected by random parameter variations as T_{ox}, L_{eff})

Results cont'd

For predictive BPTM 65nm technology

iLVT Transistors:

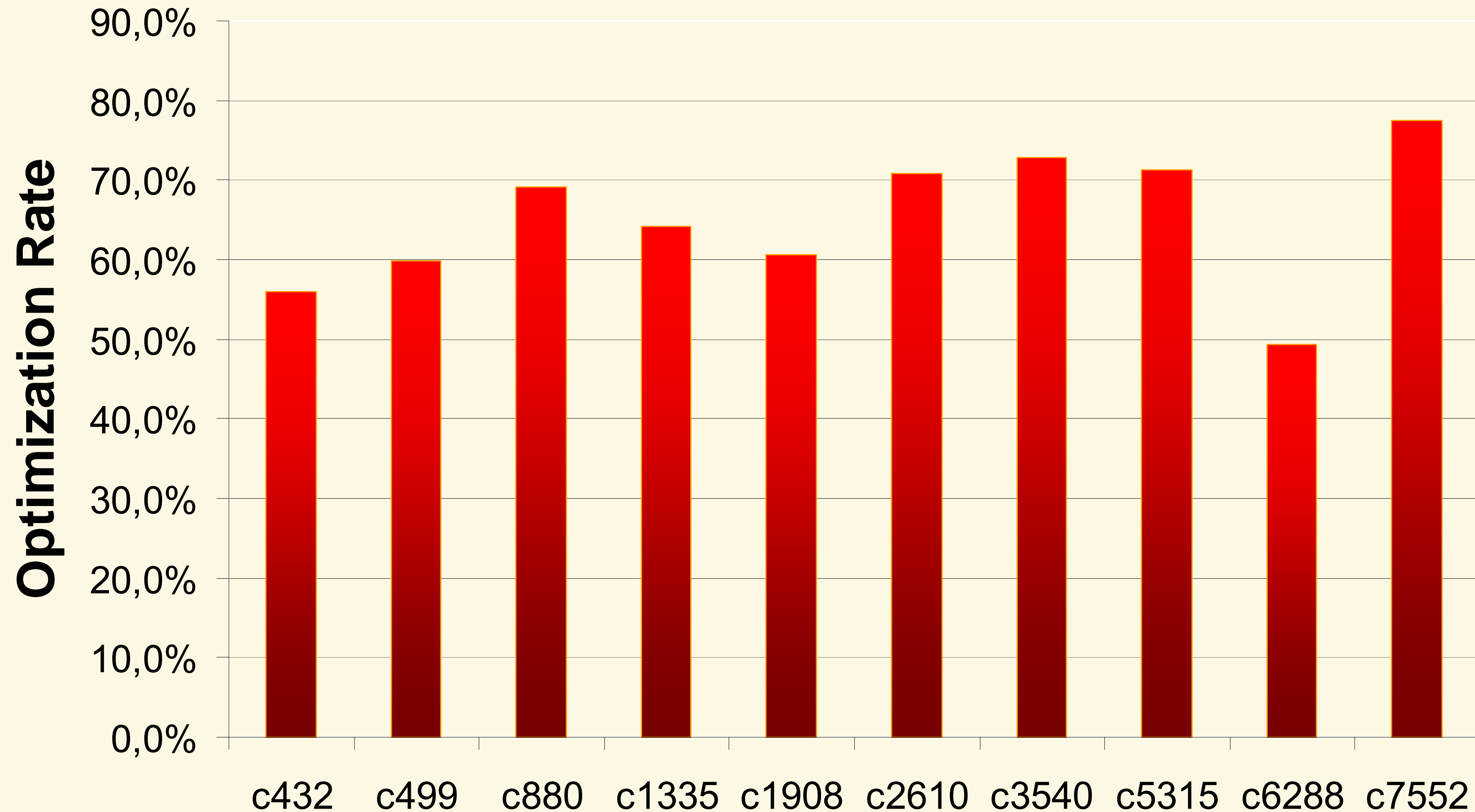
- *NDEP* about *30% lower* than the standard technology value
- T_{ox} and L_{eff} not changed

iHVT Transistors:

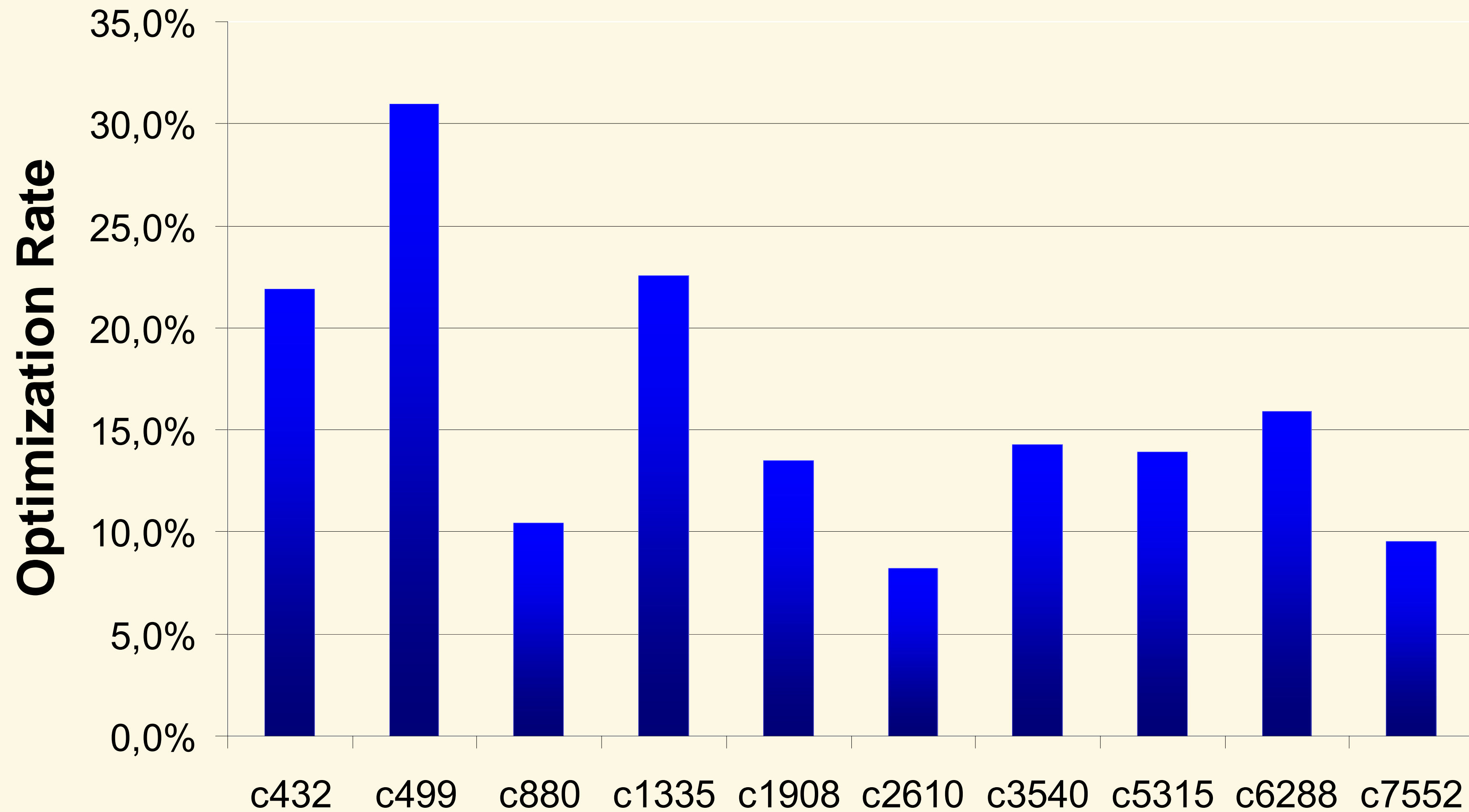
- *NDEP* and *Tox* approximately *10% higher* than standard values
- *Leff* not changed

5. ISCAS - Benchmarks

LVT vs. iMVT



DTCMOS vs. iMVT



5. Conclusion

- Subthreshold current and gate oxide leakage dominate leakage power
- Variation of NDEP, T_{ox}, and L_{eff} affect leakage, delay, and input capacity
- Improved Mixed-V_{th} (iMVT) combines advantages of DTCMOS and Dual-Tox-CMOS at transistor and gate level
- Average 65% *(vs. LVT)* and 18% *(vs. DTCMOS)* leakage reduction at constant delay

Thank you!

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