SBCCI 2004

17th SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN

CHIP ON THE REEFS

Low Power Gate-level Design with Mixed-V_{th} (MVT) Techniques

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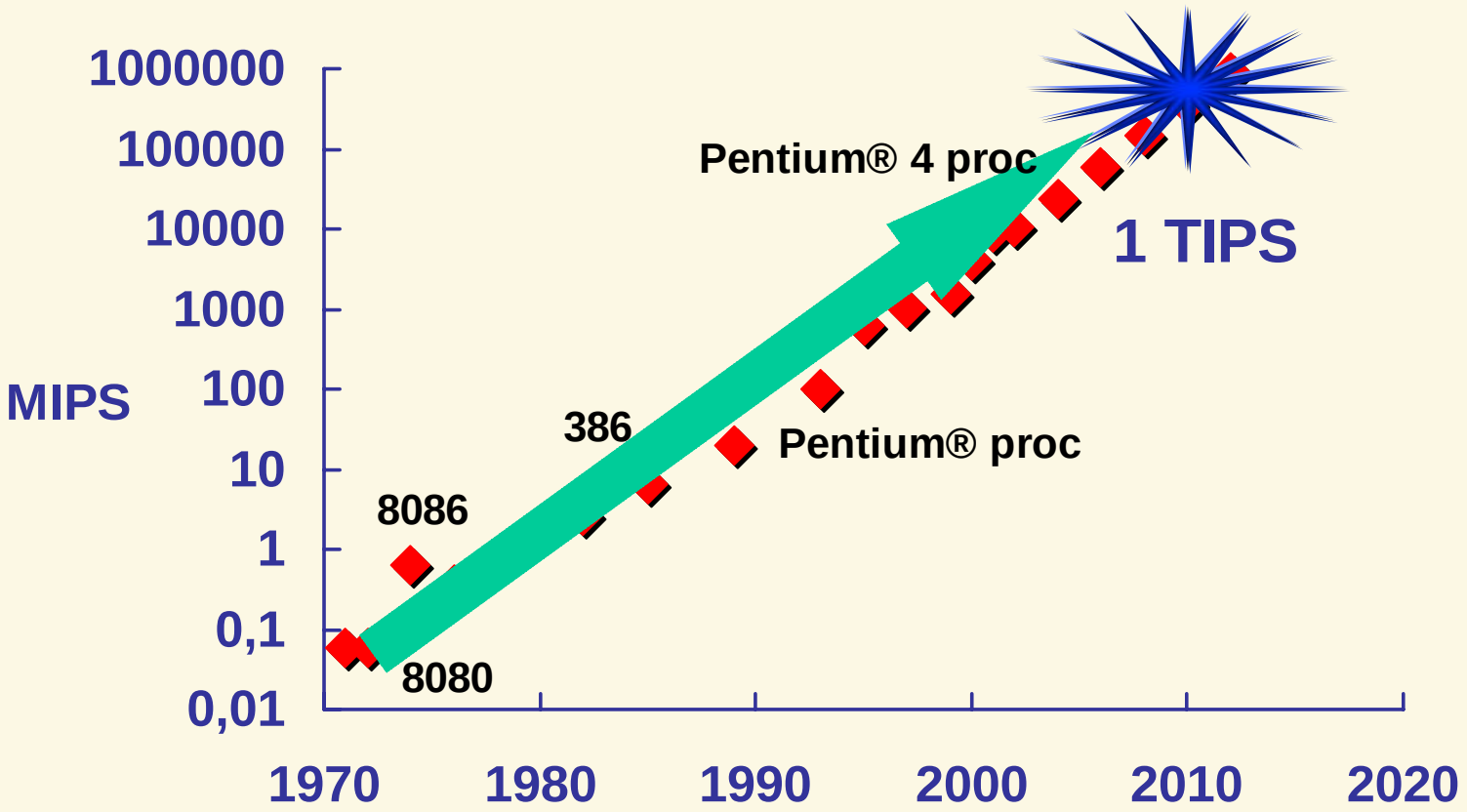
Outline

1) Motivation
2) Basics
3) Different Threshold Voltages
4) Application of Mixed-V_{th}
5) Conclusion

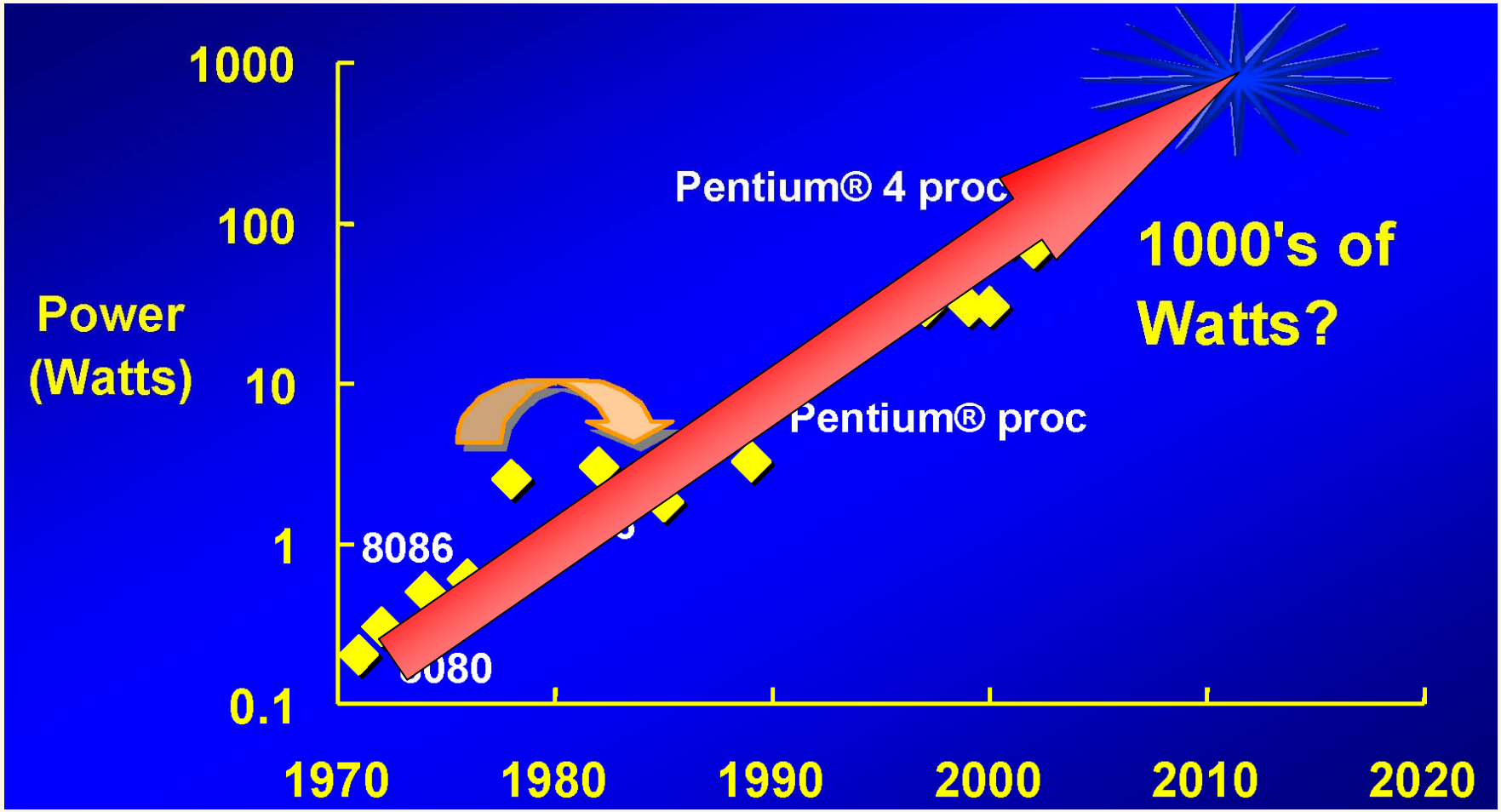
1. Motivation

Trend: Performance



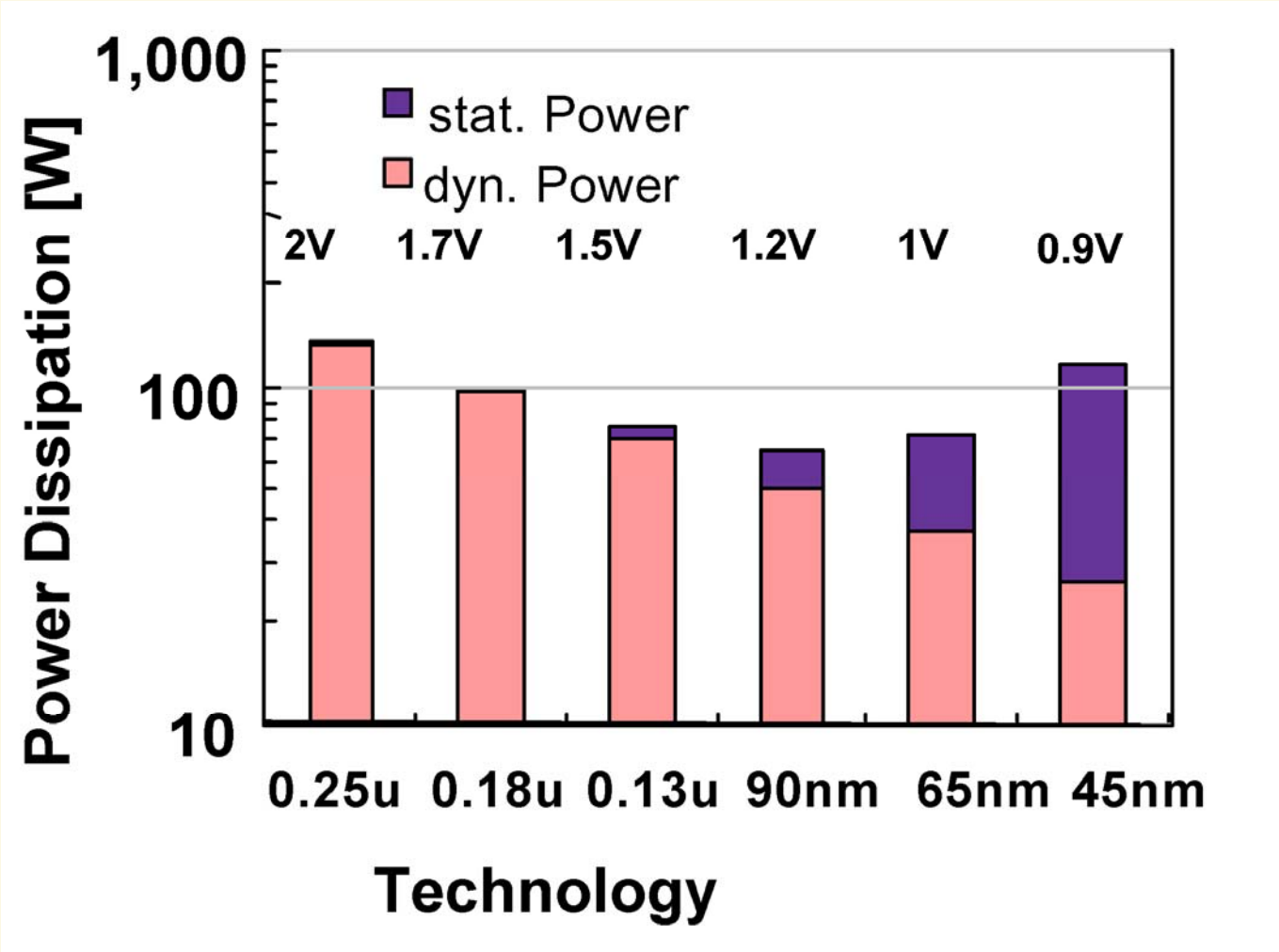
Intel, '03

Trend: Power



Intel, '03

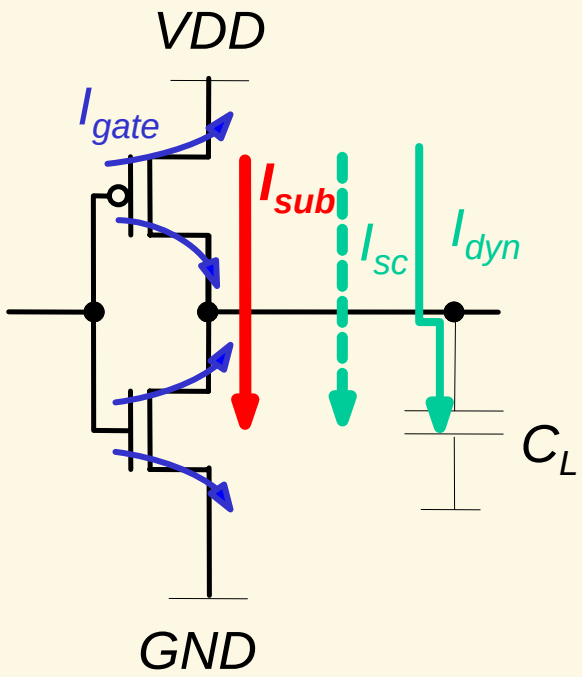
Dynamic Power vs. Leakage

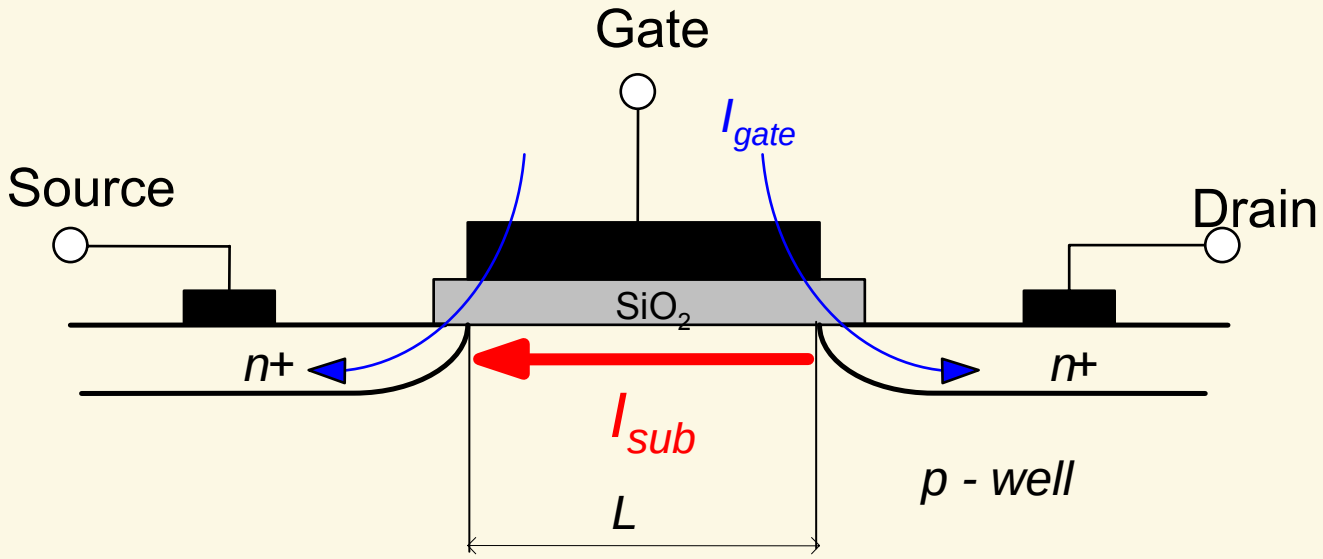


Intel, '02

2. Basics

Power Dissipation in CMOS





- I_{sub} occurs if $V_g < V_{th}$
- carriers move by diffusion along the surface
- ***I_{sub} dominates leakage***

Power & Delay Dependence

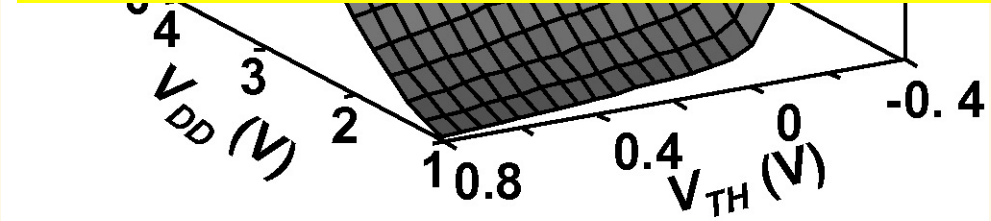
$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^{\,2} + I_0 \frac{W_T}{W} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

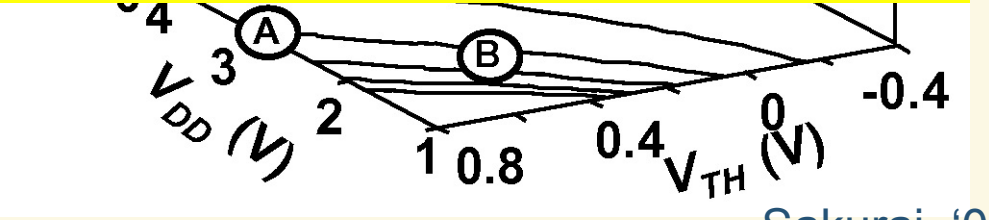
Problem:

fast transistors with high power dissipation (low V_{th})

or

slow transistors with low power dissipation (high V_{th})





Sakurai, '01

3. Different Threshold Voltages

Dual Threshold Voltages (DTCMOS)

- Use different V_{th}'s
  - use lower threshold for devices on the critical paths
  - use higher threshold for devices off the critical paths
- Decrease power without reduce performance
- Approaches at:
  - Gate level (V.Sundararajan, et al., LPED'99)
  - Transistor level (L.Wei, et al., DAC'99)

DTCMOS on Different Levels

Transistor level

+ optimization is accurate
- needs a lot of resources
- not useful for considerably designs

Gate level

+ less time-consuming
- fewer detailed, because only two gate types

New Approach: Mixed-V_{th} (MVT) CMOS

1. Goal: fast gates keep the delay while leakage decreases

- if all transistors in gates are standard dimensioned
  (= PMOS and NMOS have same delay)

→ different output slopes

- up to now: sizing of transistors

⇒ *idea:* use different threshold voltages within a gate to adapt the slopes

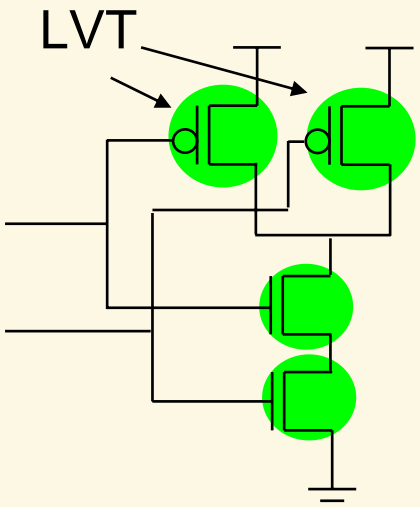
(MVT) CMOS cont'd

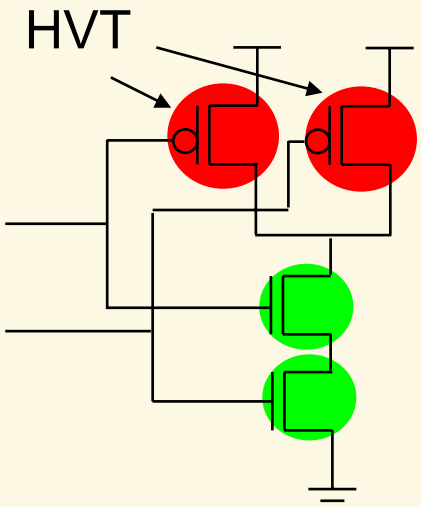
2. Goal: additionally gate types at constant mask count

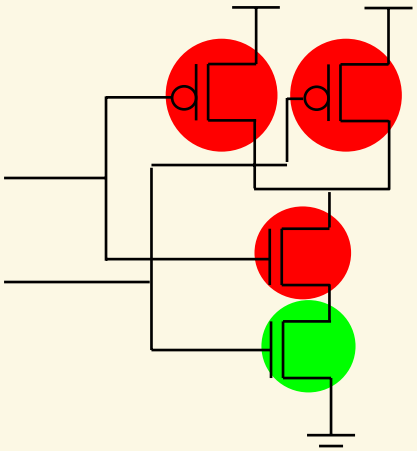
- only two gate types in DTCMOS at gate level (HVT, LVT)
- problem: more LVT gates after optimization as needed to keep the delay

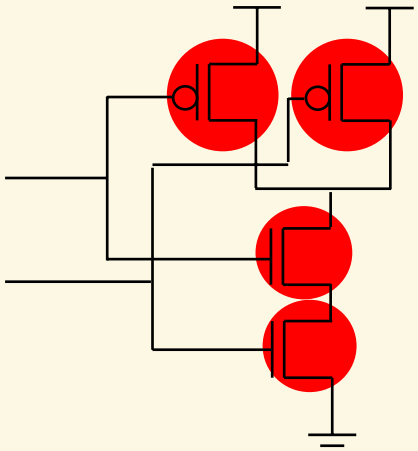
→ *idea:* mixed threshold voltages within a gate

MVT- NAND2









***LVT* gate**	***M-LVT* gate**	***MVT* gate**	***HVT* gate**
- all MOS have low V_{th}	- PMOS have high V_{th}	- PMOS and upper NMOS have high V_{th}	- all MOS have high V_{th}
- rise time is shorter than fall time	- rise and fall time are nearly the same	- ***middle delay cell***	- ***maximum delay cell***
- ***minimum delay cell***	- ***minimum delay cell***		

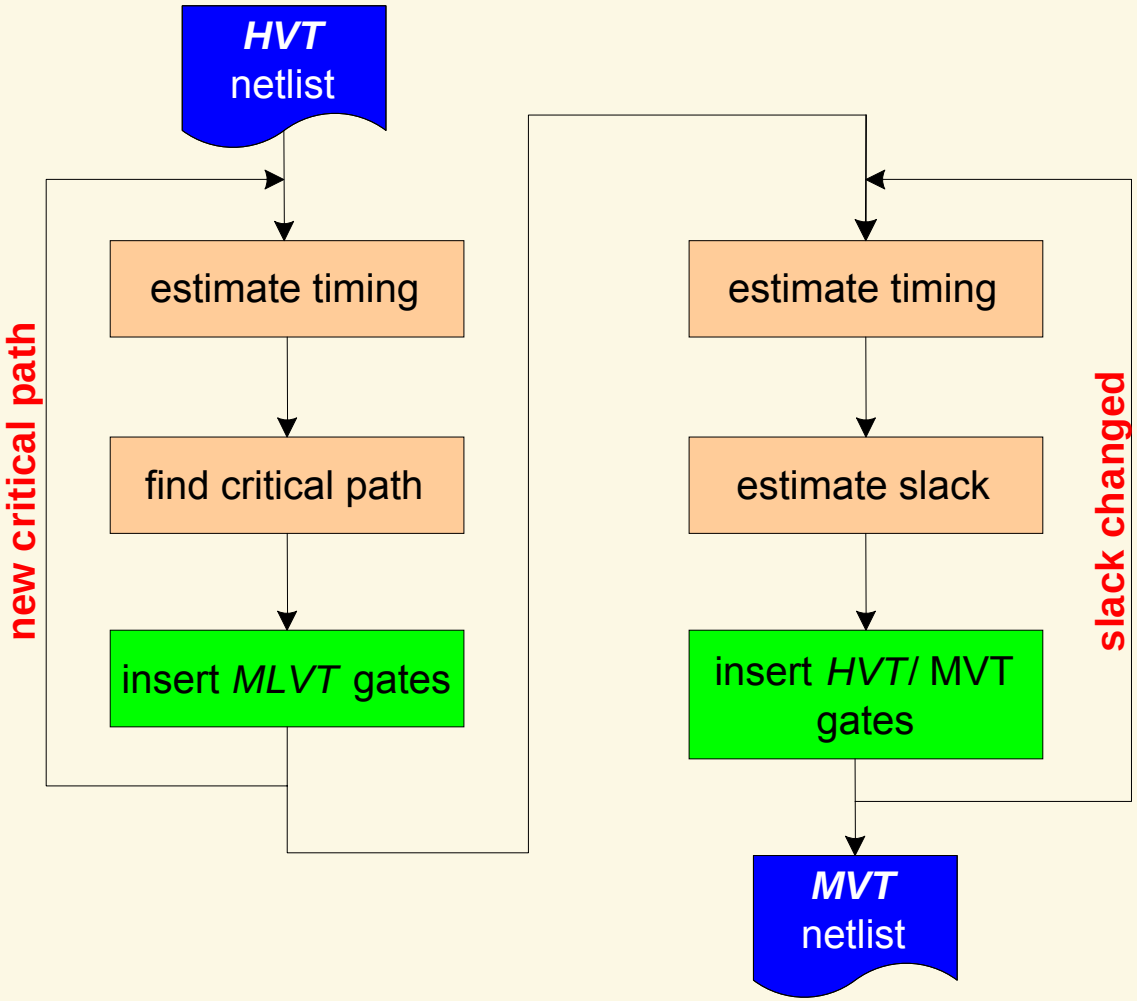
Gate characteristics

		HVT	LVT	M-LVT	MVT
I_{leak} [nA]	E_{in} = 00	**41**	**58**	**58**	**46**
	E_{in} = 01	**43**	**101**	**101**	**46**
	E_{in} = 10	**37**	**89**	**89**	**84**
	E_{in} = 11	**19**	**236**	**19**	**19**
$I_{average}$		**35 nA**	**121 nA**	**67 nA**	**48 nA**
Delay (t_d)		**71 ps**	**53 ps**	**53 ps**	**60 ps**

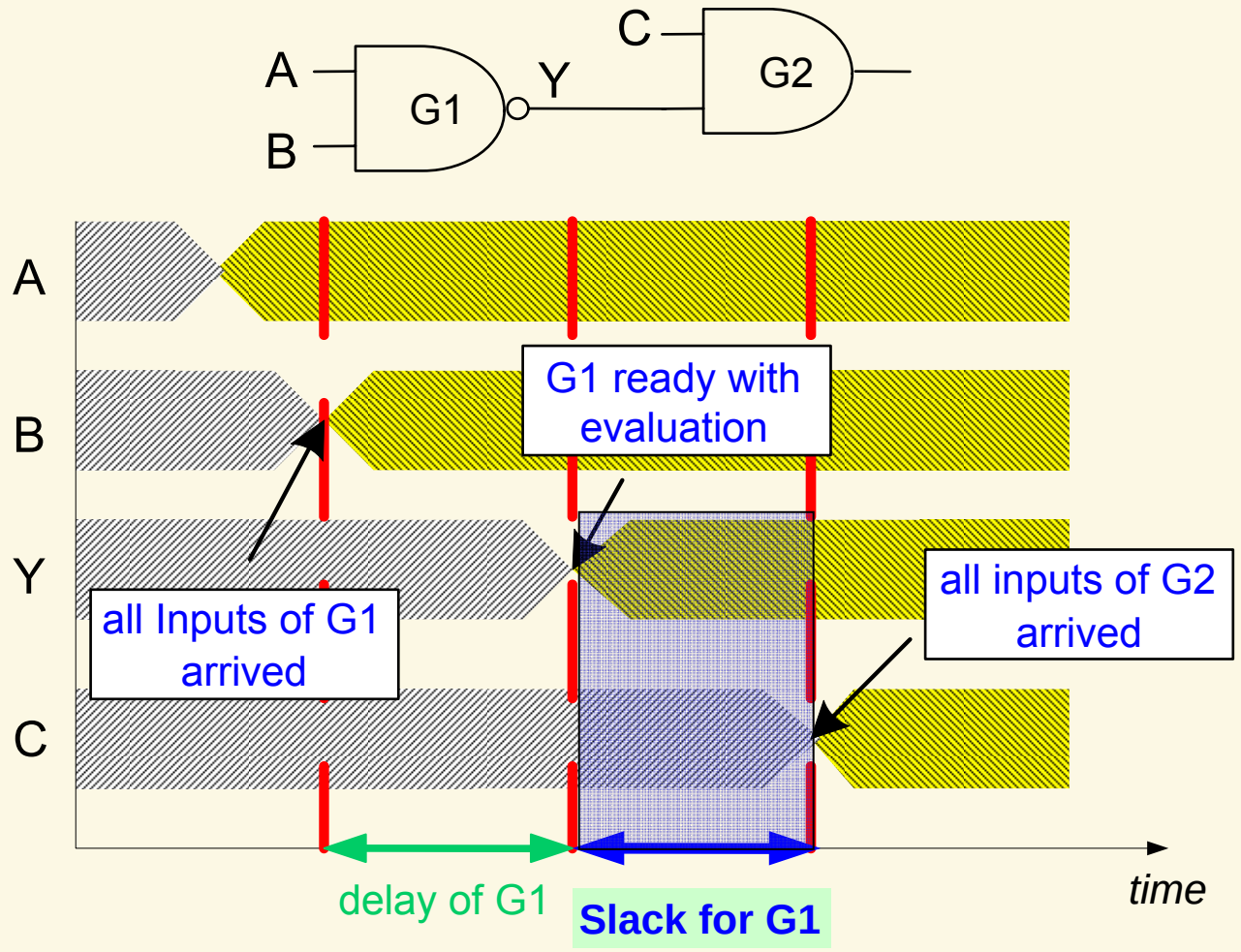
BPTM 65nm technology

4. Application of Mixed-V_{th}

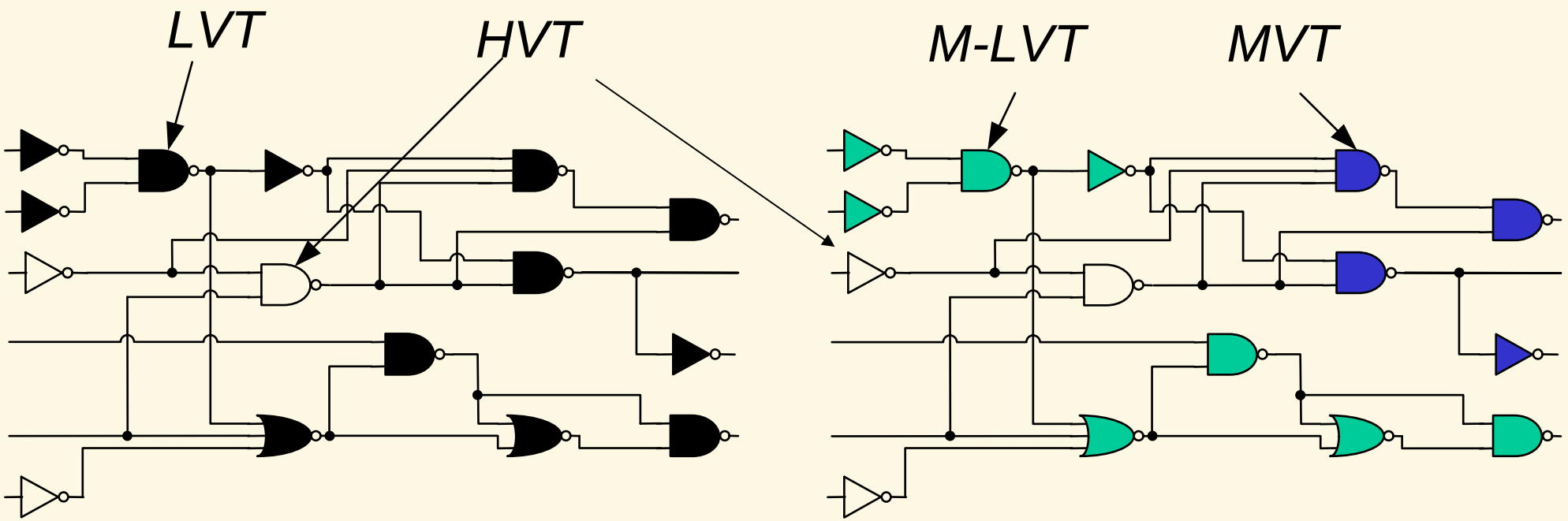
Design flow


HVT
netlist
estimate timing
find critical path
insert MLVT gates
new critical path
estimate timing
estimate slack
insert HVT/ MVT
gates
slack changed
MVT
netlist

Slack


A
B
G1
Y
C
G2
A
B
Y
C
G1 ready with evaluation
all Inputs of G1 arrived
all inputs of G2 arrived
delay of G1
Slack for G1
time

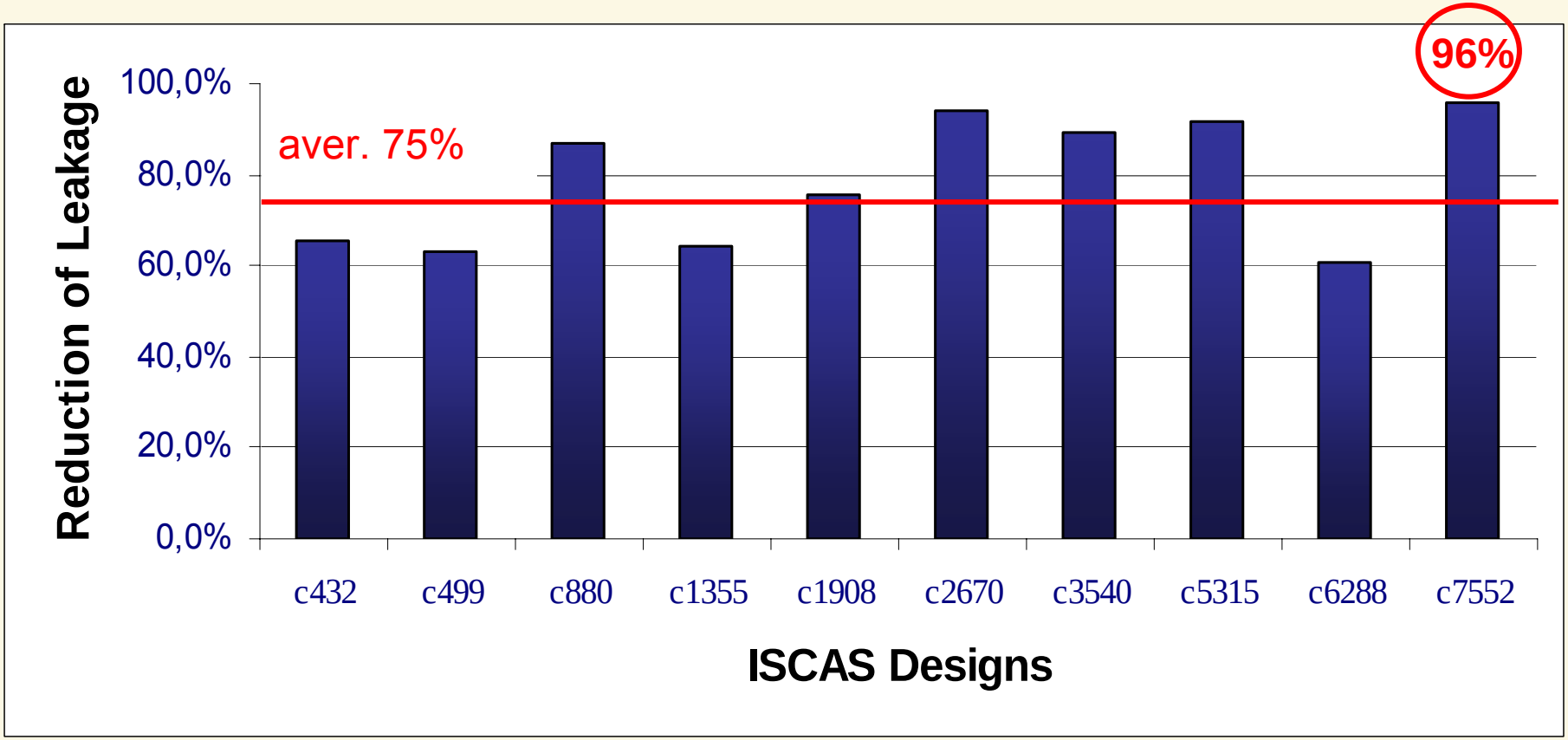
MVT - Paths



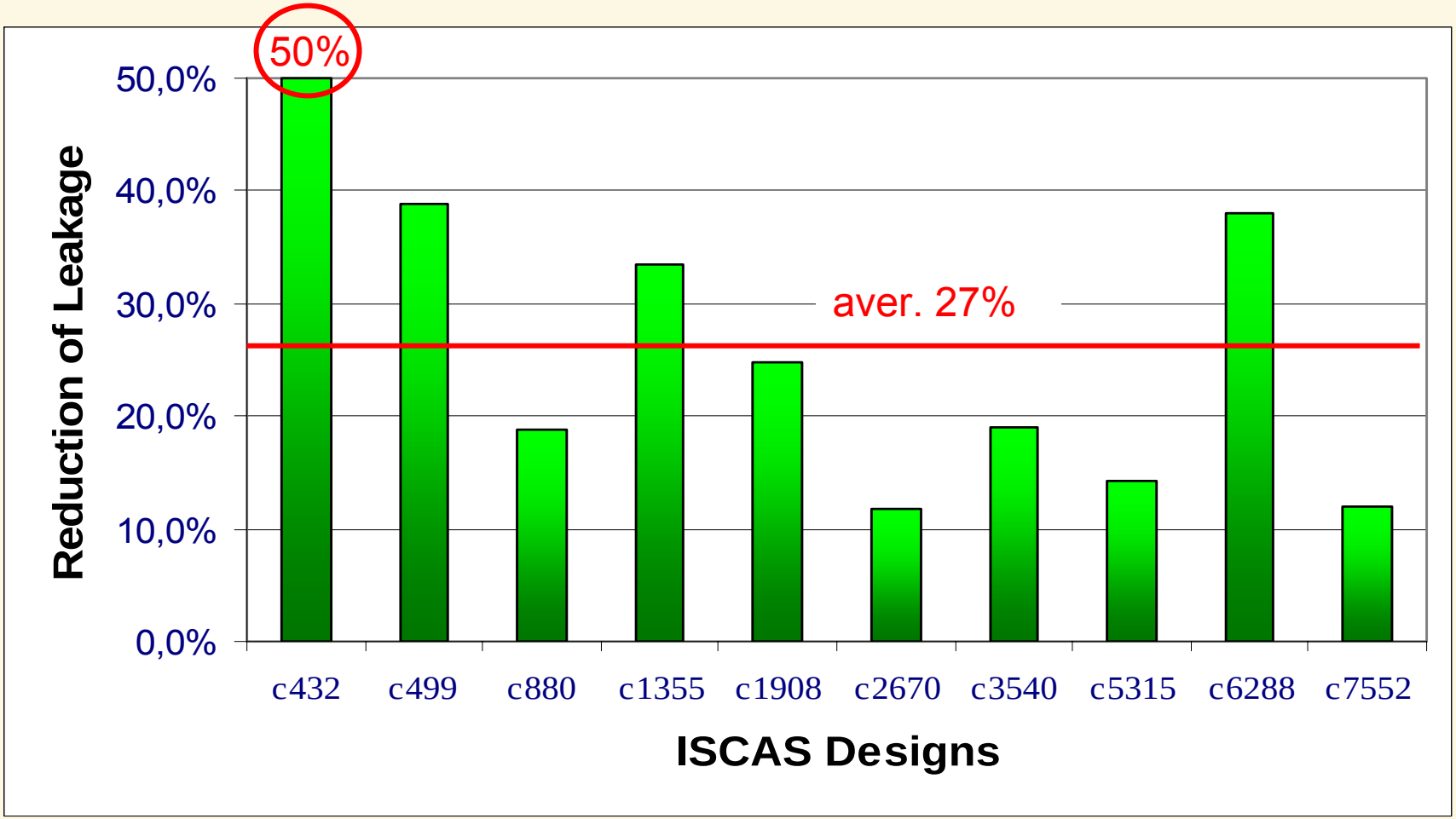
Up to now: *two kinds of cells*
(Dual-Threshold CMOS)

MVT-CMOS

MVT vs. LVT implementation



MVT vs. DVT implementation



5. Conclusion

- Subthreshold current I_{sub} dominates leakage power
- Variation of V_{th} affects I_{sub} and delay
- Mixed-V_{th} (MVT) combines advantages of DTCMOS at gate and at transistor level
- New gate type without additional masks in contrast to DTCMOS
- Average 75% *(vs. LVT)* and 27% *(vs. DTCMOS)* leakage reduction at constant delay

Thank you!

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