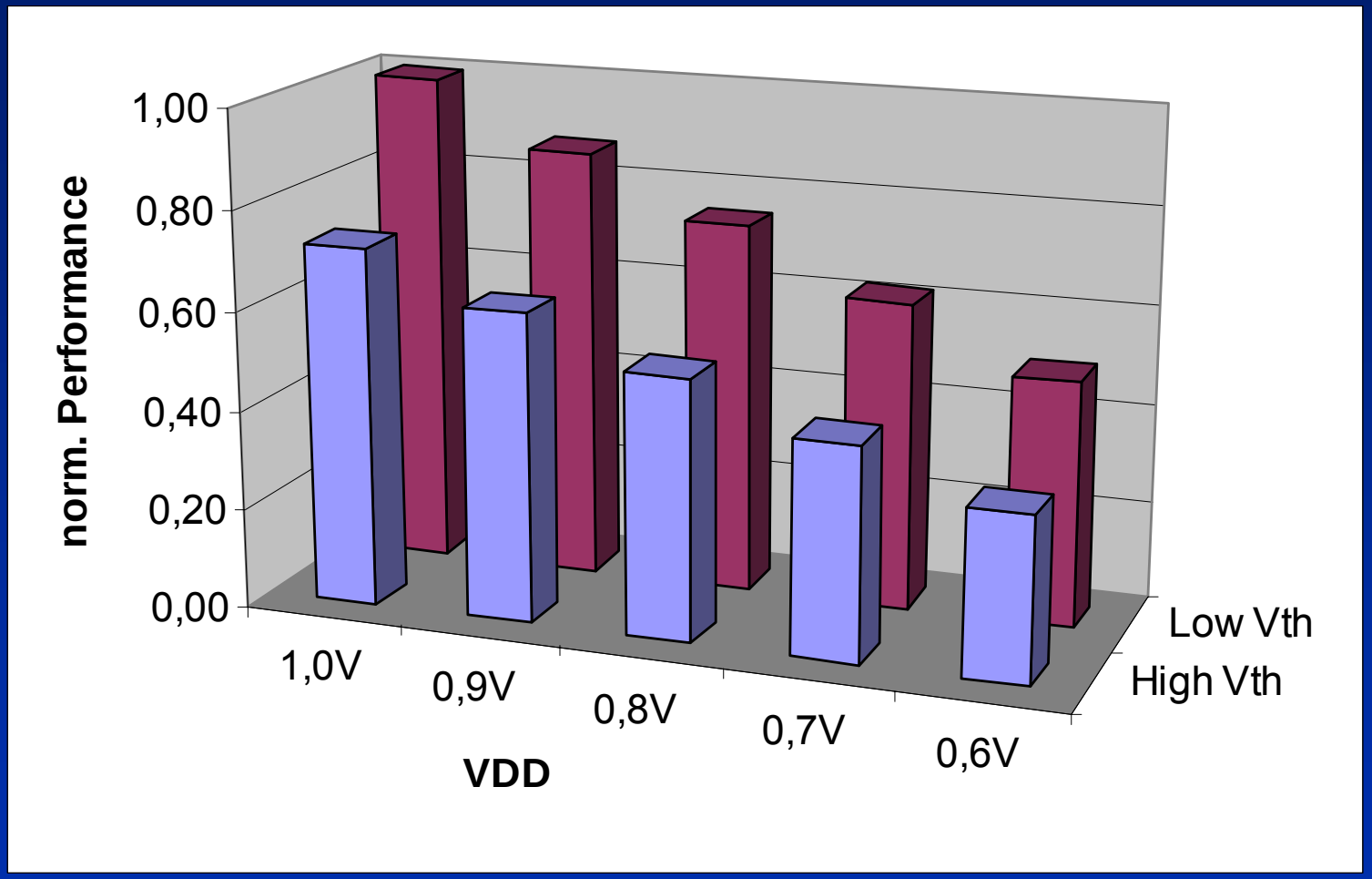
18th International Conference on VLSI Design

Reducing Leakage with Mixed-*Vth* (MVT)

Frank Sill, Frank Grassert, Dirk Timmermann

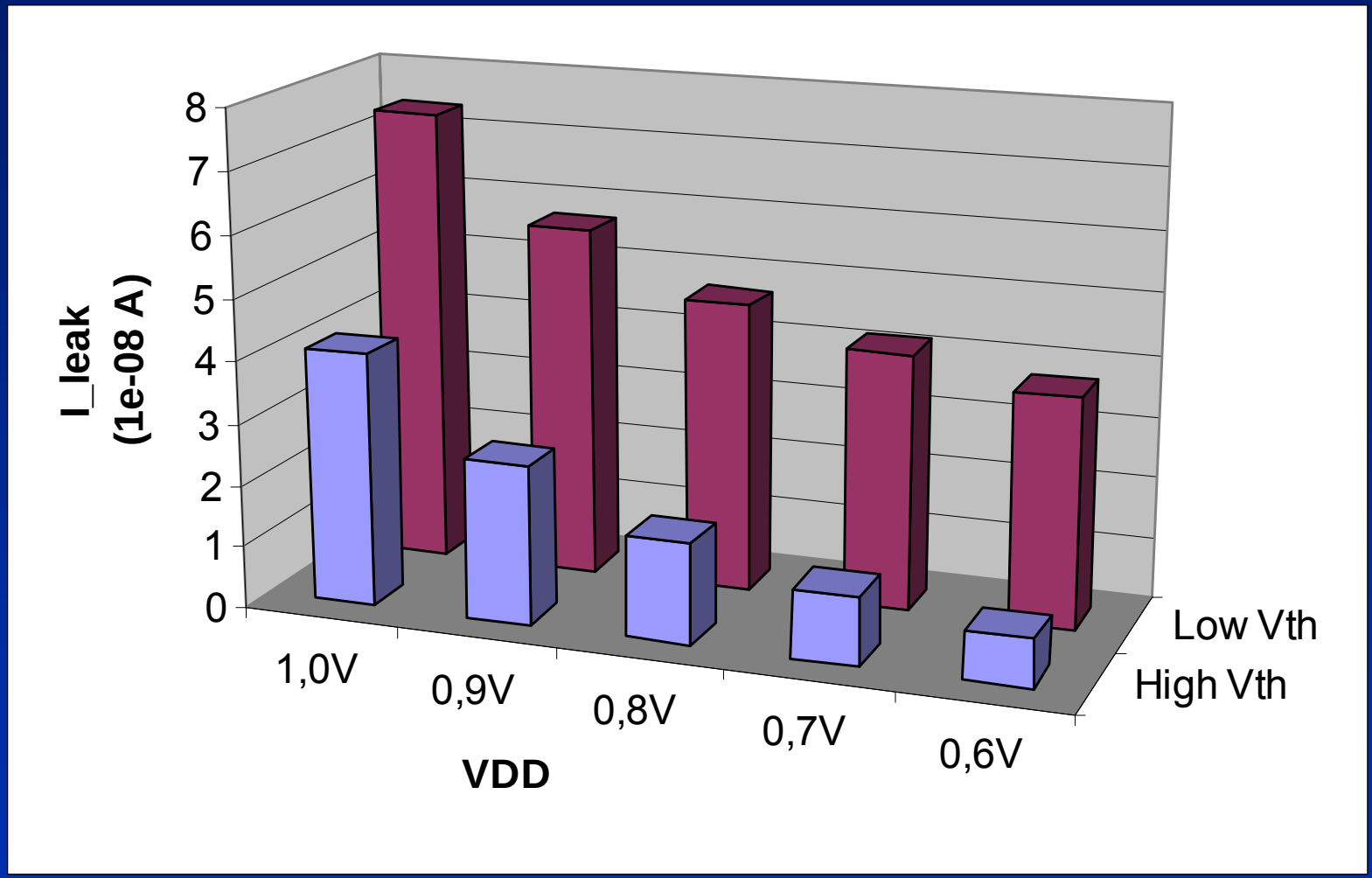
University of Rostock, Germany

Performance at different V_{th}



Measured at NAND2 BPTM 65nm Technology

Leakage at different V_{th}



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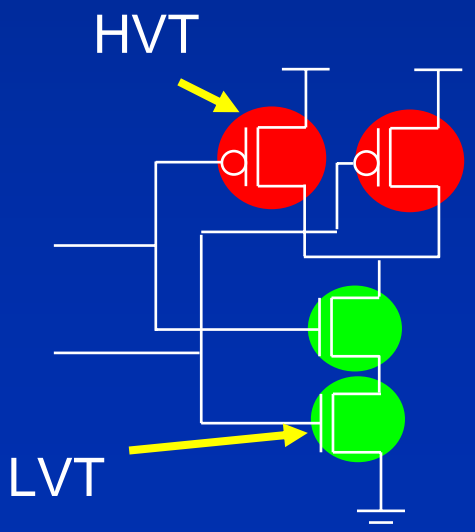
Mixed-V_{th} Pull-*Down/Up*-Paths

Goal: fast gates keep the delay while leakage decreases

- if all transistors in gates are standard dimensioned
  (= PMOS and NMOS have same delay)
- → different output slopes
- up to now: sizing of transistors

→ *idea:* use different threshold voltages within a gate to adapt the slopes



Mixed Stacks

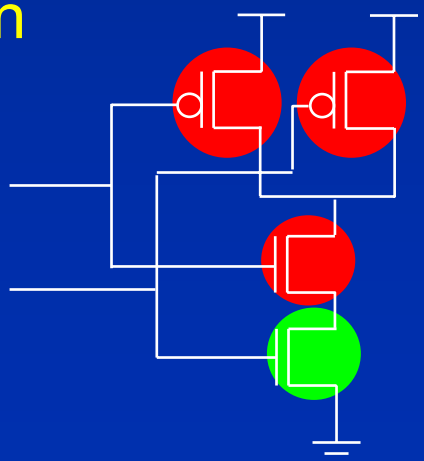
Goal: additionally gate types at constant mask count

- *sub-threshold* leakage of mixed-V_{th} stack → higher than in equal-V_{th} stack at same delay

AND

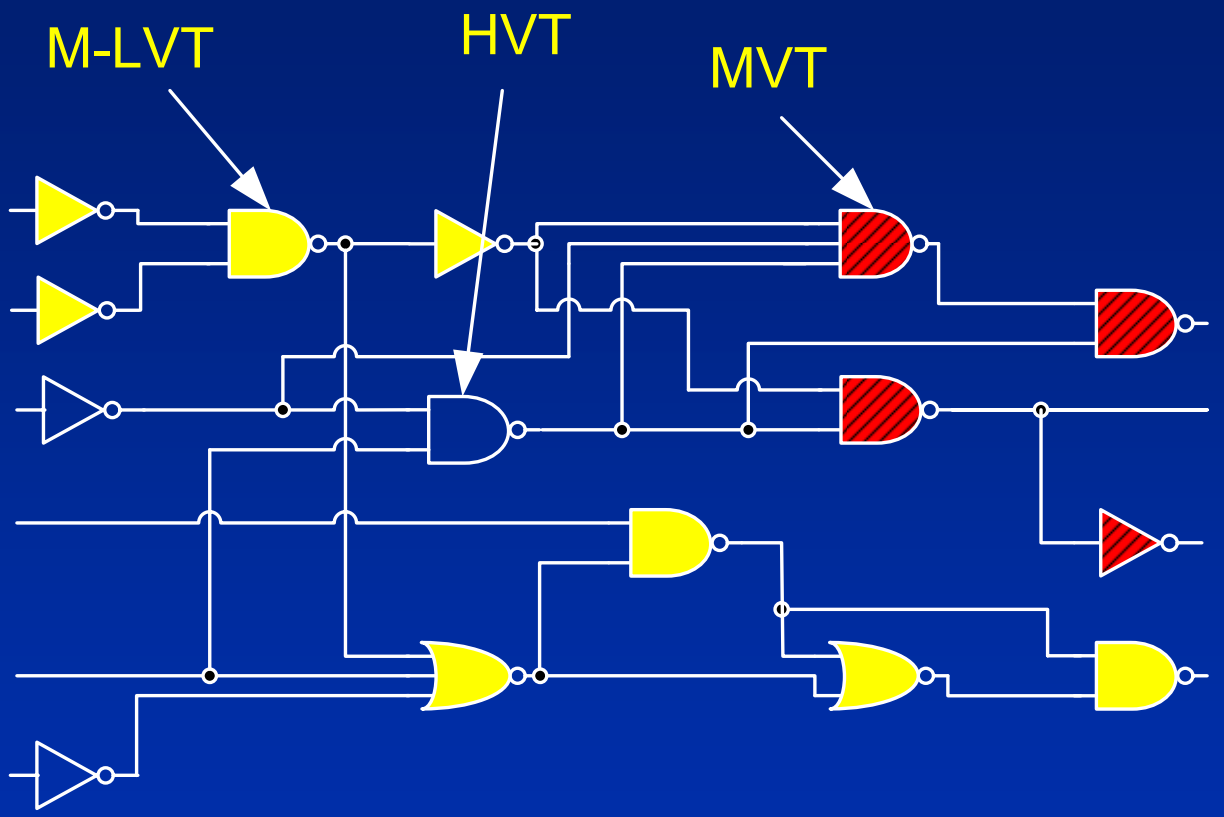
- only two gate types in DTCMOS at gate level (HVT, LVT)

→ problem: more LVT gates after optimization as needed to keep the delay



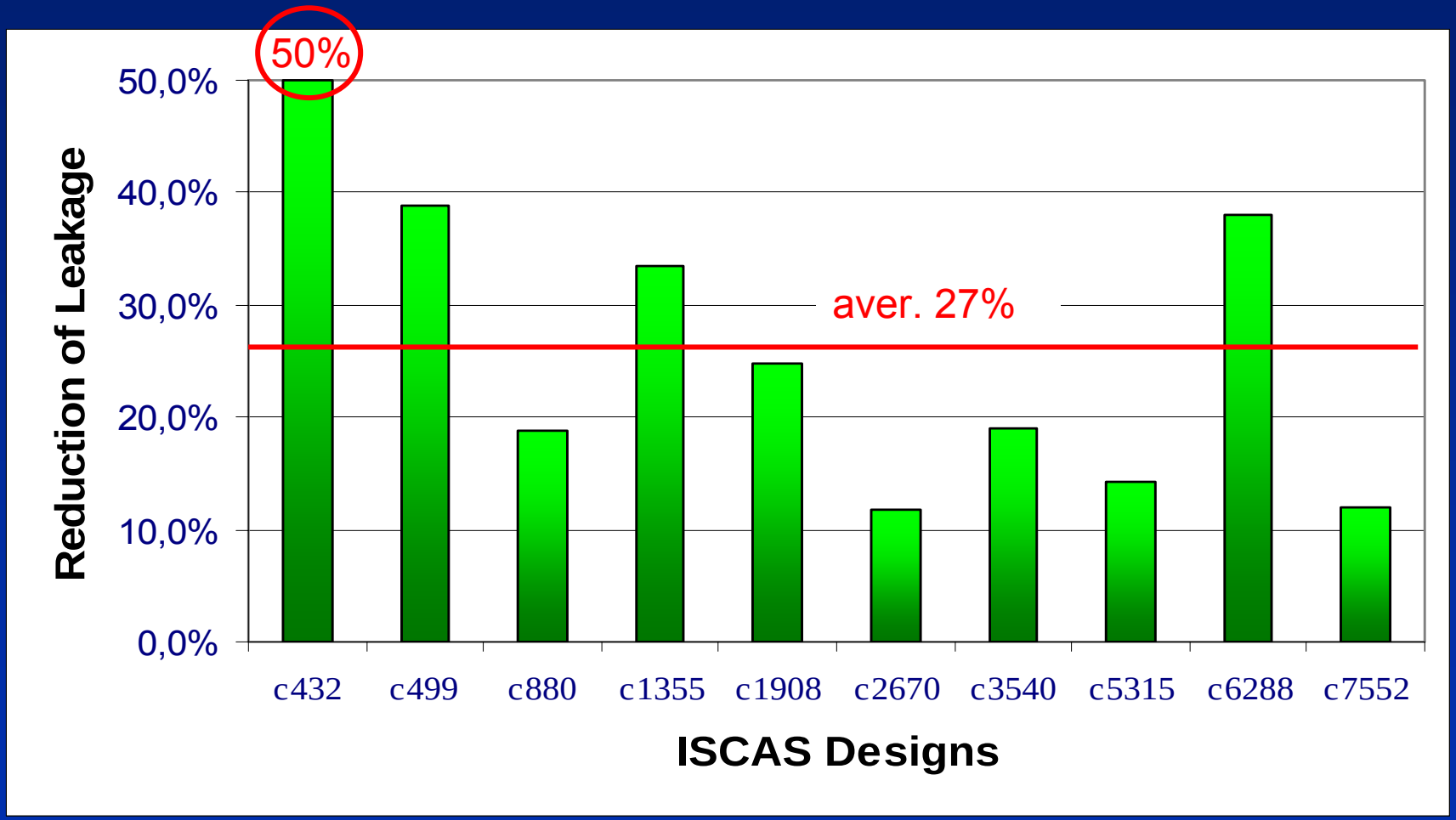
idea: mixed threshold voltages within a gate (stack & PUP/PDP)

MVT paths



path-delay stays constant but leakage goes down

MVT vs. DTCMOS implementation



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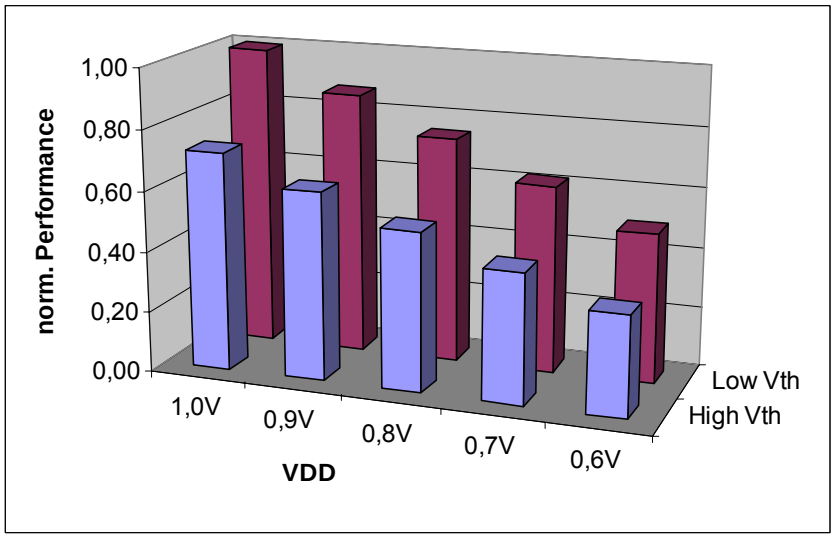
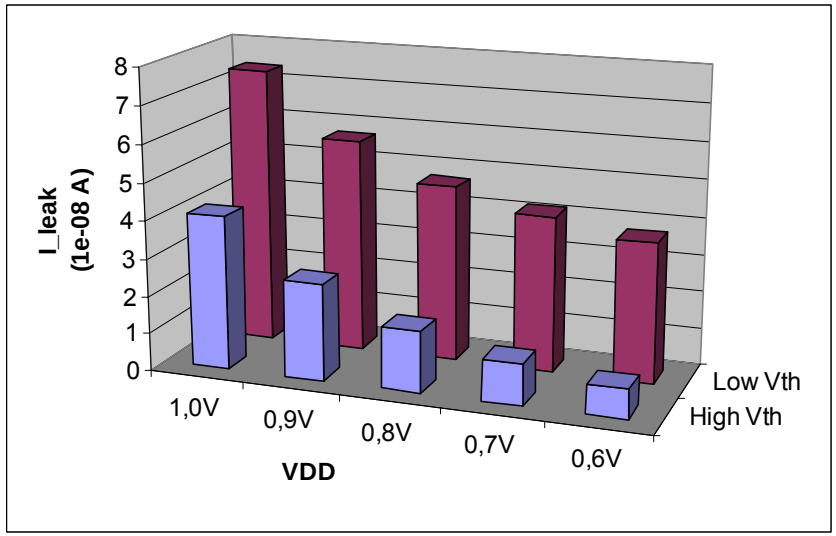
- Leakage of High-Threshold-Voltage (HVT) gates is much lower than leakage of Low-Threshold-Voltage (LVT) gates
- Difference in delay is moderate





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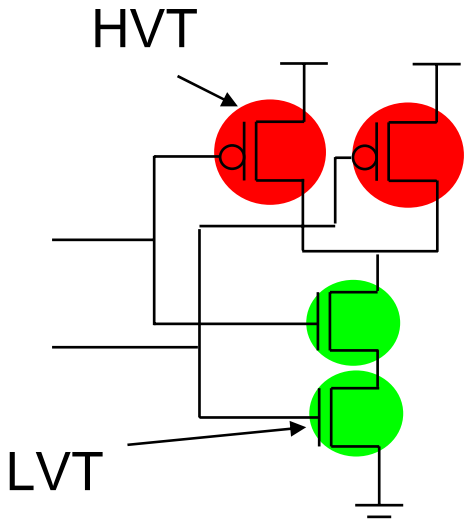

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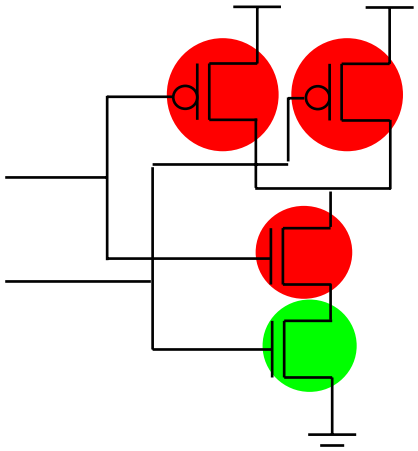

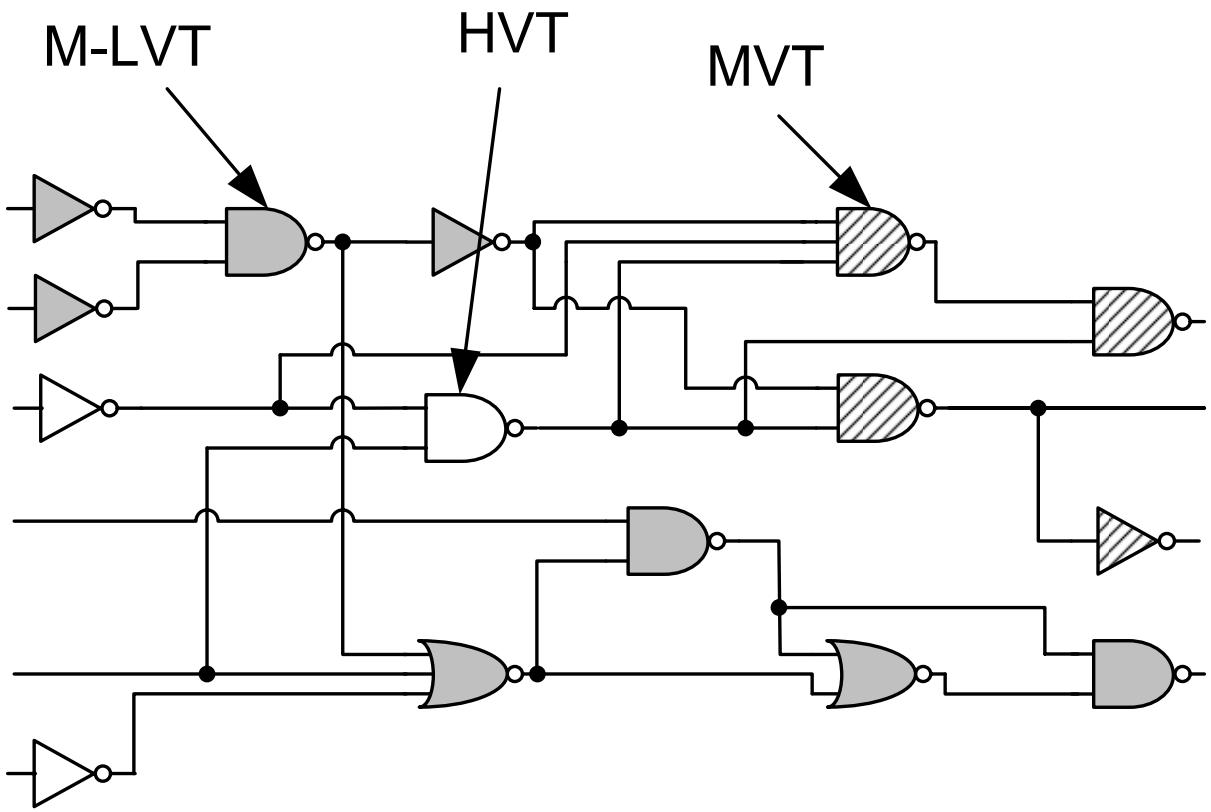

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