Low Power Techniques for Highly Mobile Protection of Media Streams

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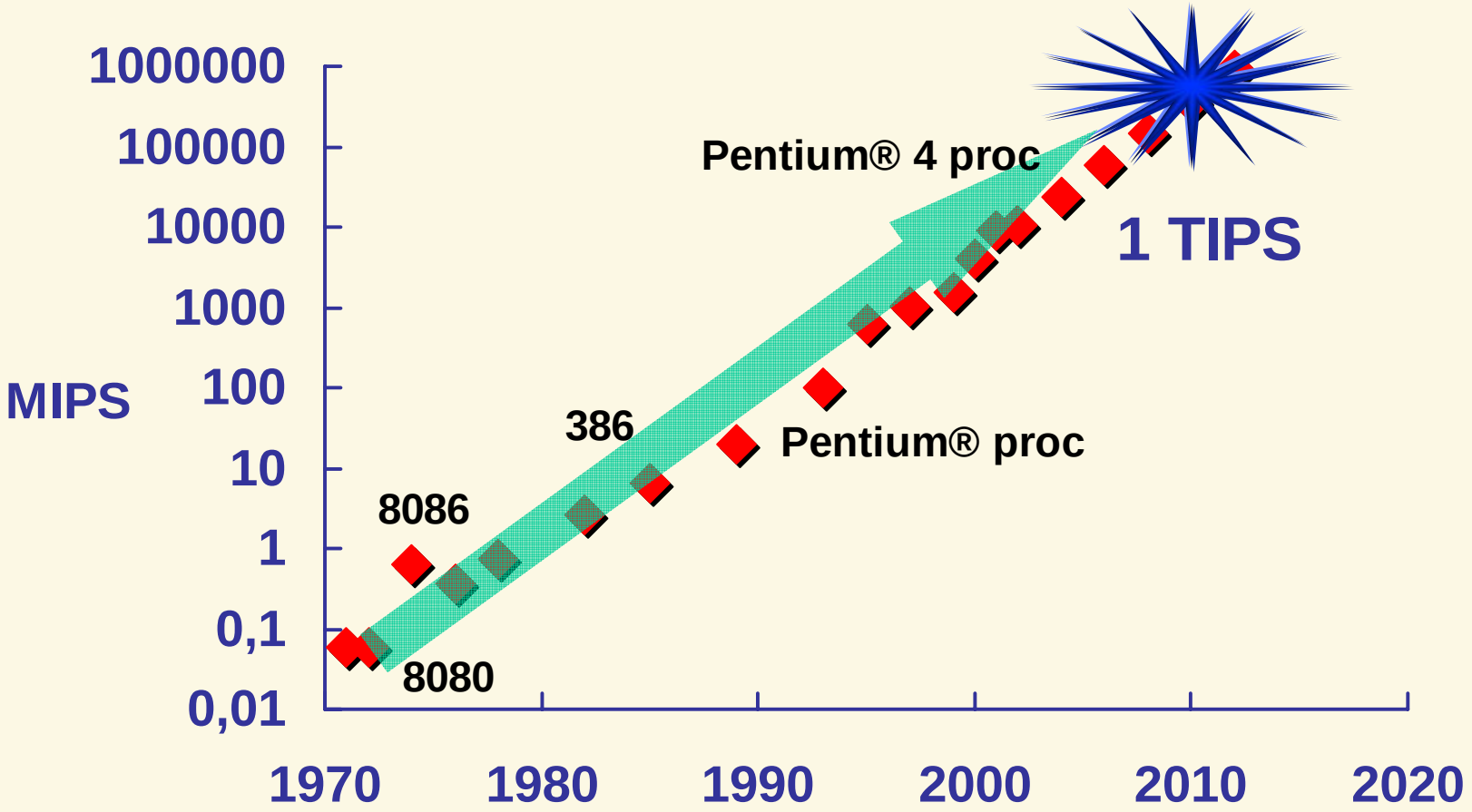
Outline

1. Motivation
2. AC-TSPC
3. Mixed-V_{th}
4. Outlook

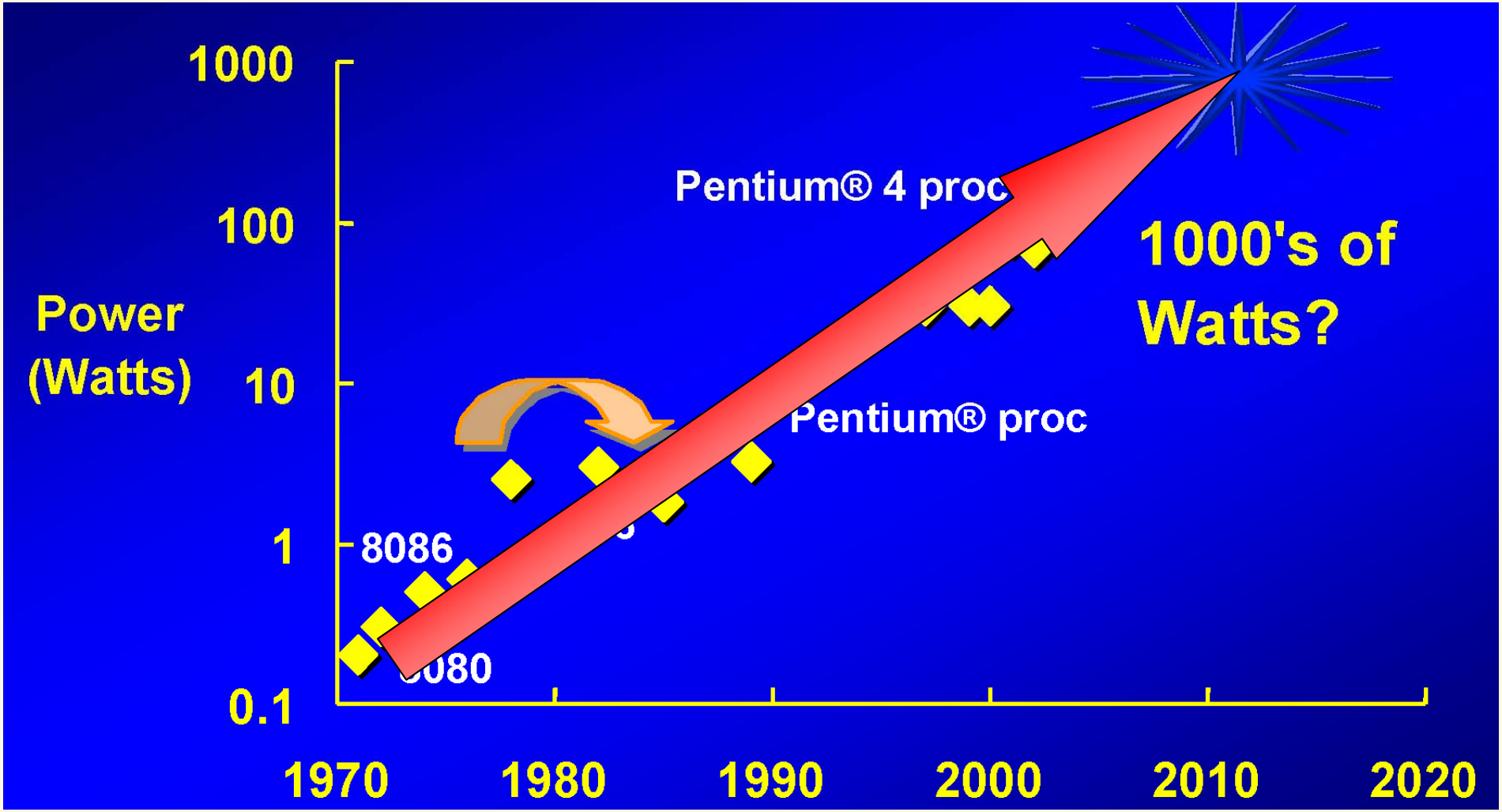
1. Motivation

Trend: Performance



Intel, ‘03

Trend: Power

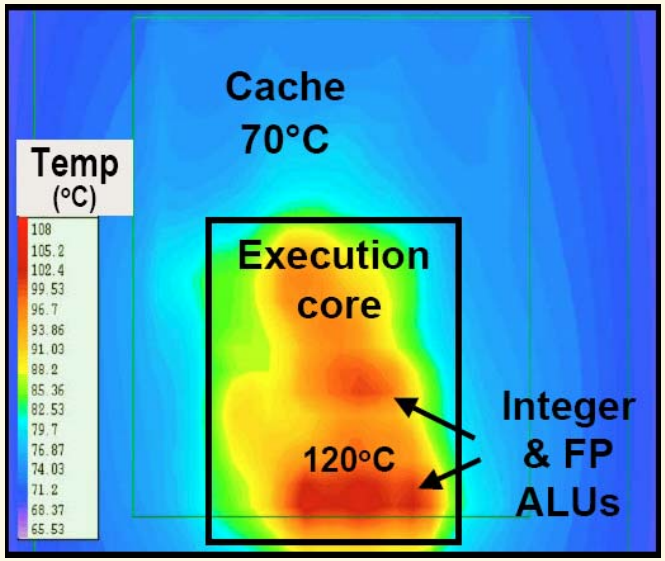


Intel, '03

Why thinking about new ways ?

high power dissipation results in:

- shorter battery life



- expensive cooling
- high energy costs

(>9% of energy costs in USA for internet)

My Work

Goal: Analysis and development of power reduction techniques in multimedia systems

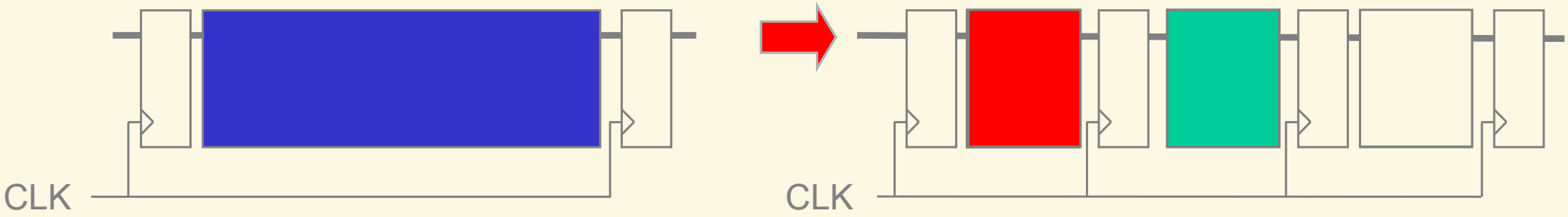
Two Approaches:

1. Reduction of ***dynamic*** power dissipation in high performance systems → AC-TSPC
2. Reduction of ***static*** power dissipation → Mixed-V_{th}

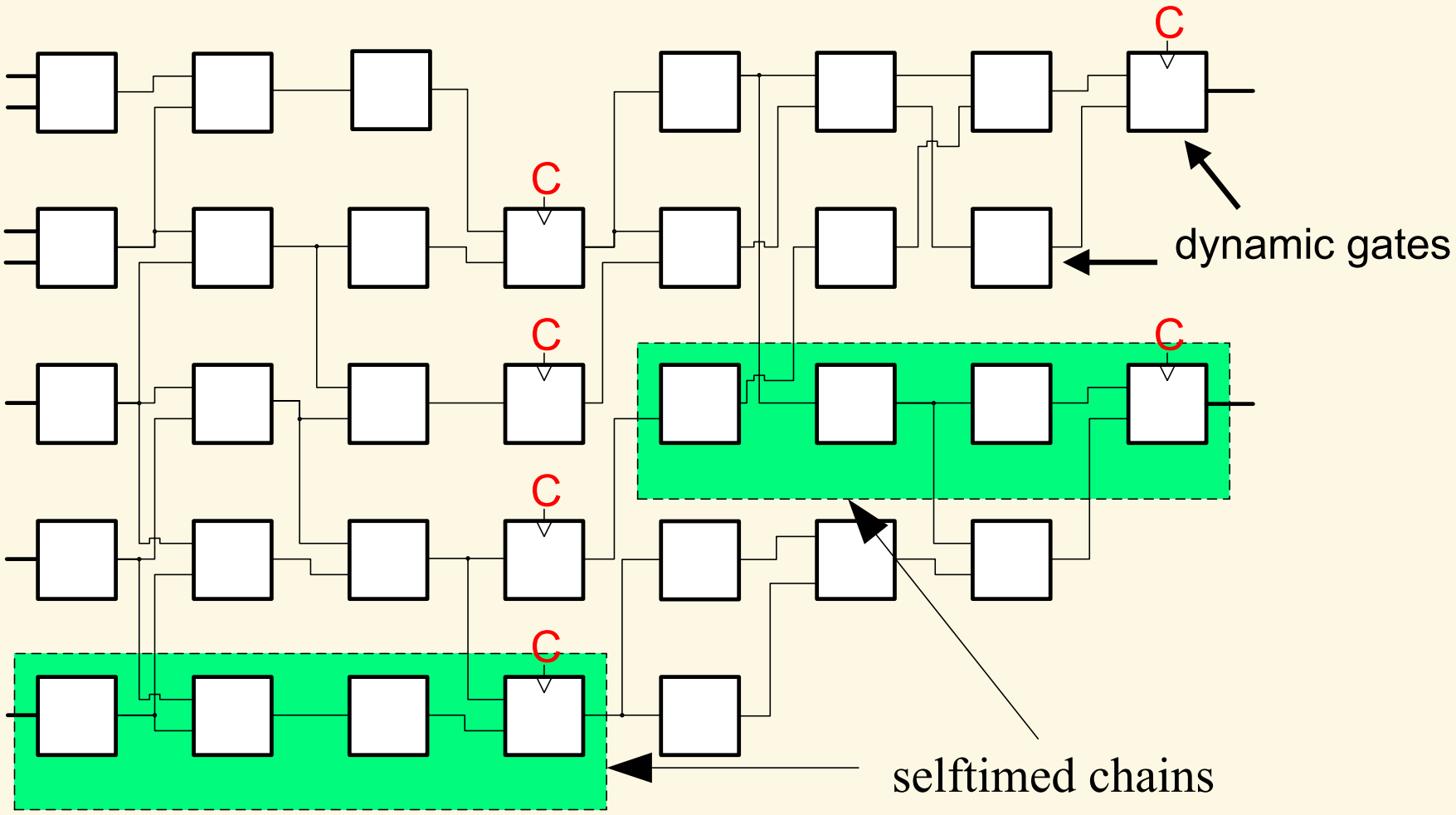
2. AC-TSPC

Pipelines

- Audio, Video or Smartcard applications use data streams
- Pipelines preferred for data stream processing
- High frequencies possible (less logic operations per clock phase)



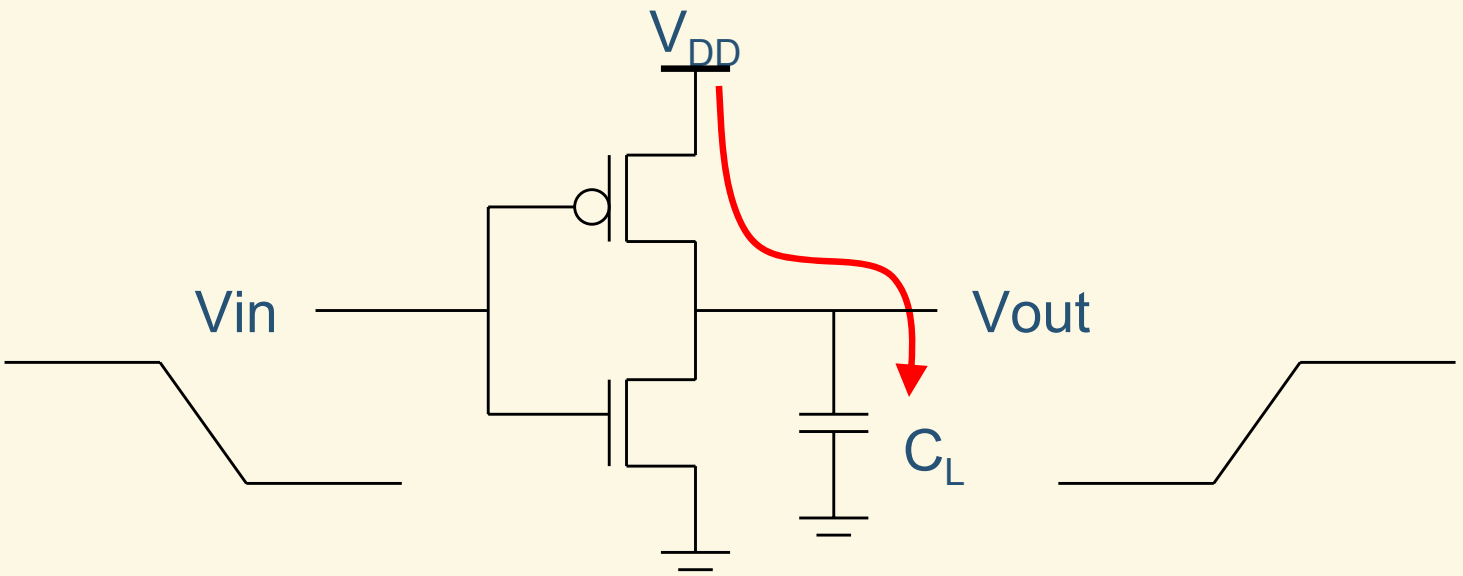
Structure of AC-TSPC



Advantages of AC-TSPC

- use of dynamic gates
  → higher clock frequencies
  → lower input capacity C_L → reduced P_{dyn}
- asynchronous clocked chains
  → reduced latency

Dynamic Power Consumption



load capacitance

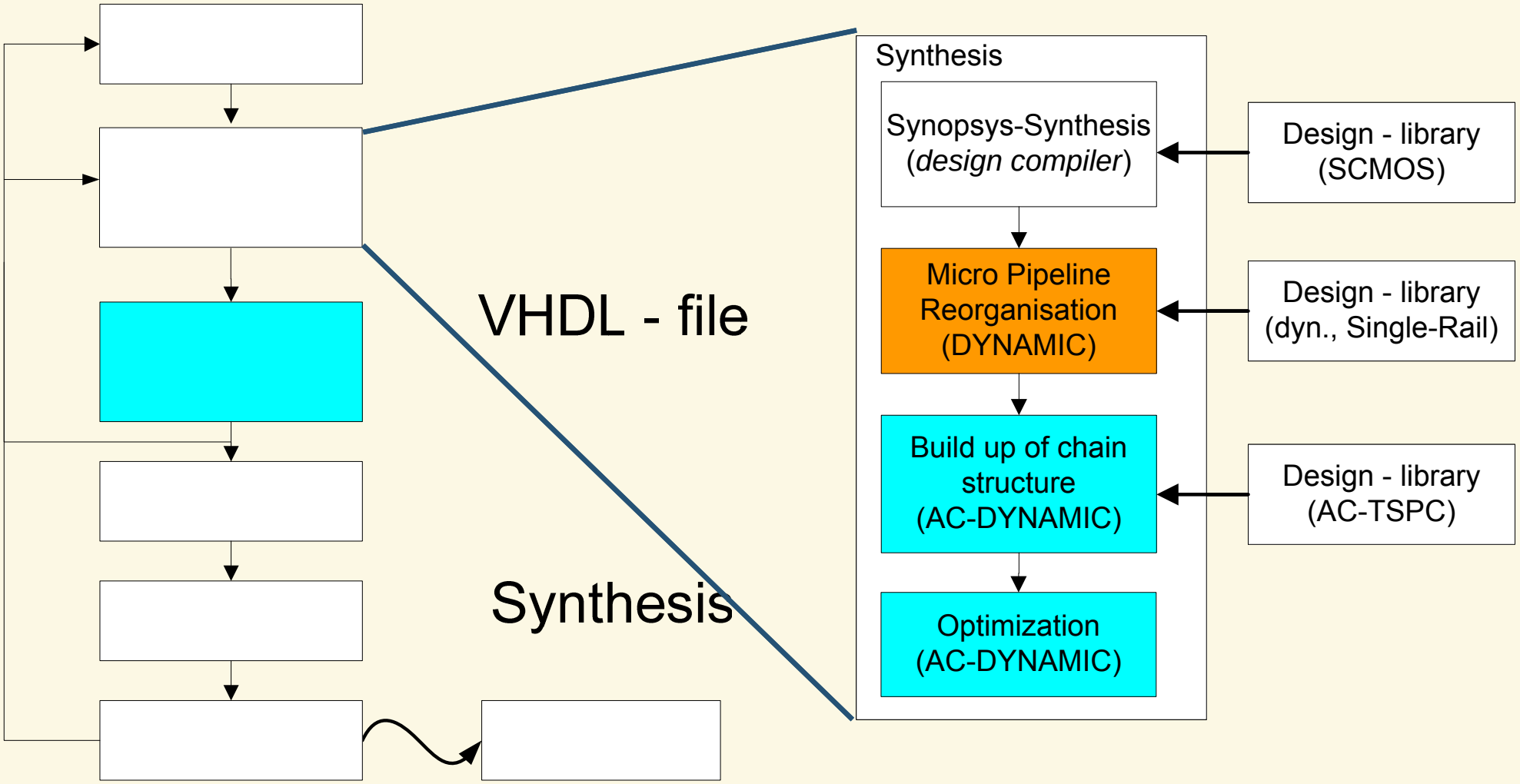
frequency

$$\textit{Dynamic Power} = C_L * V_{DD}^2 * W_{0\rightarrow1} * f$$

supply voltage

probability for 0-to-1 transition on output

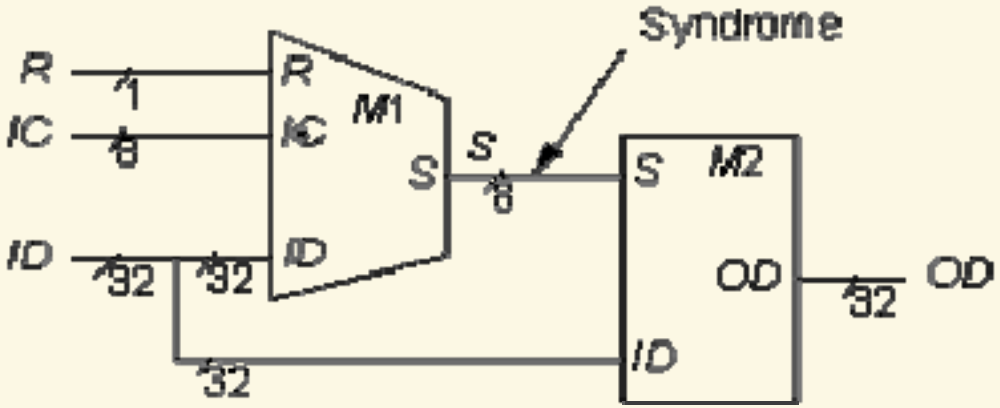
Generic design flow



AC-Dynamic

- Generates chain structure
- Includes additional logic to ensure correct timing
- Optimizations
- Determination of clock signal
- Simulation of the circuit

Example: ISCAS c1355 32-Bit Single-Error-Correction (UMC18)



	Stat. CMOS	AC-TSPC
Latency (ns)	3.8	1.7
Max. frequency (GHz)	0.710	2.1
Power (W/GHz)	28.897	38.070
Power*Delay @2.1GHz (10^{-9}Ws)	**(approx.) 389**	**135**

Publications (AC-TSPC)

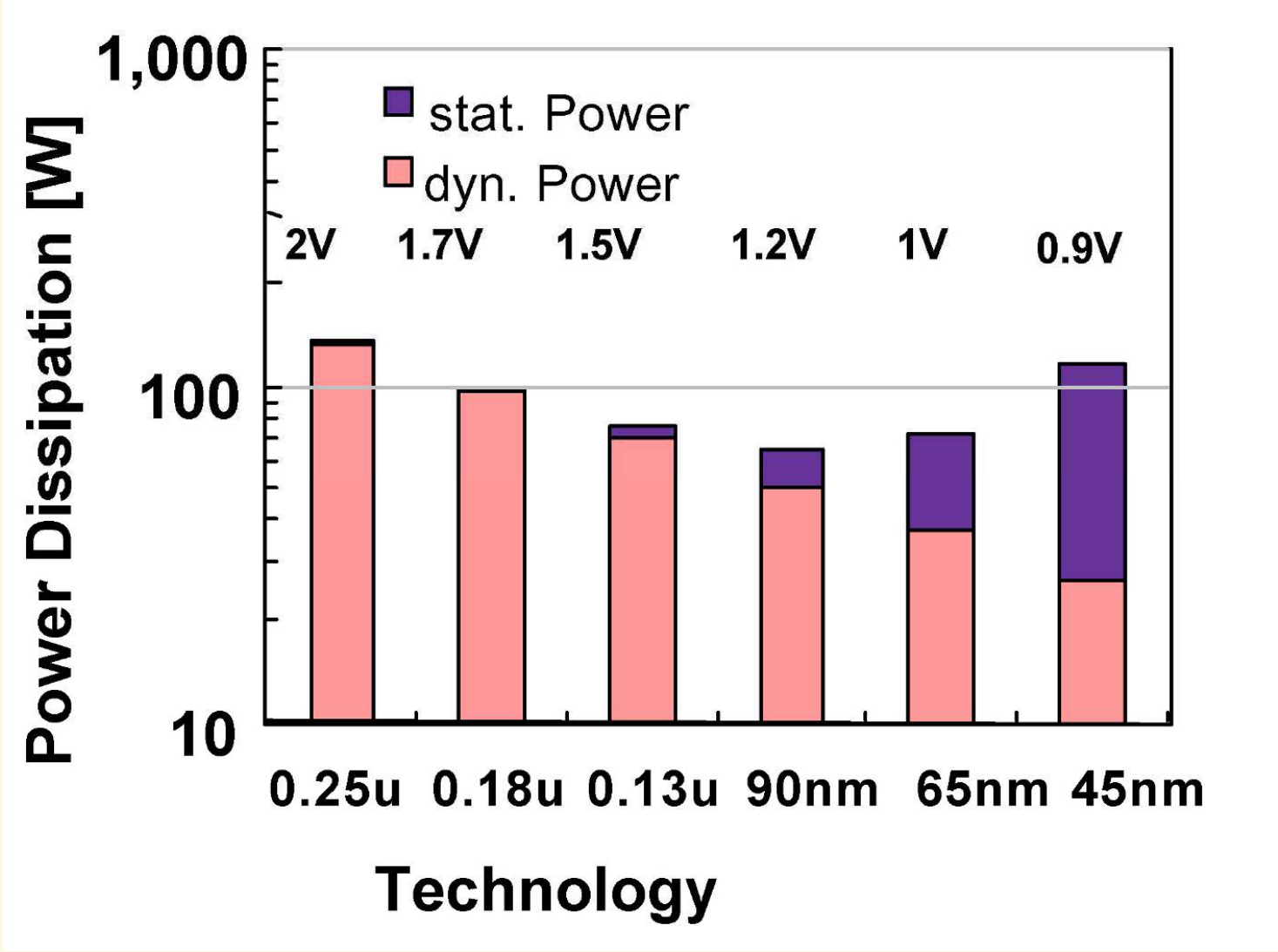
- F. Grassert, F. Sill, D. Timmermann, ***Verlustleistungs-reduzierung in Datenpfaden***, IuK-Tage Mecklenburg-Vorpommern, Rostock, Juni 2003
- F. Sill, F. Grassert, A. Wassatsch, D. Timmermann, ***Designflow zur Entwicklung Geschwindigkeits- und Leistungsoptimierter* Schaltungen**, 4. IuK-Tage Mecklenburg-Vorpommern, Rostock, Juni 2003
- F. Sill, F. Grassert, D. Timmermann, ***A Design Flow for Asynchronous Dynamic Logic and Standard Synthesis Tools***, SNUG 2003, Boston, MA, USA, September 2003, nominated for “Technical Committee Award“

Conclusion

- Highly reduced power dissipation in high performance pipelined designs
- Standard Design flow extended
- Designs can changed into AC-TSPC technology
- 2 national and 1 international publication

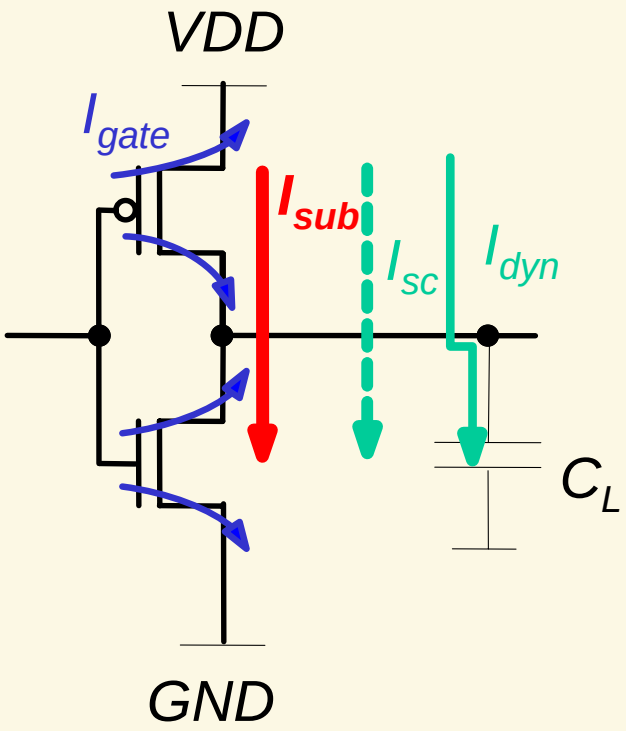
3. Mixed-V_{th}

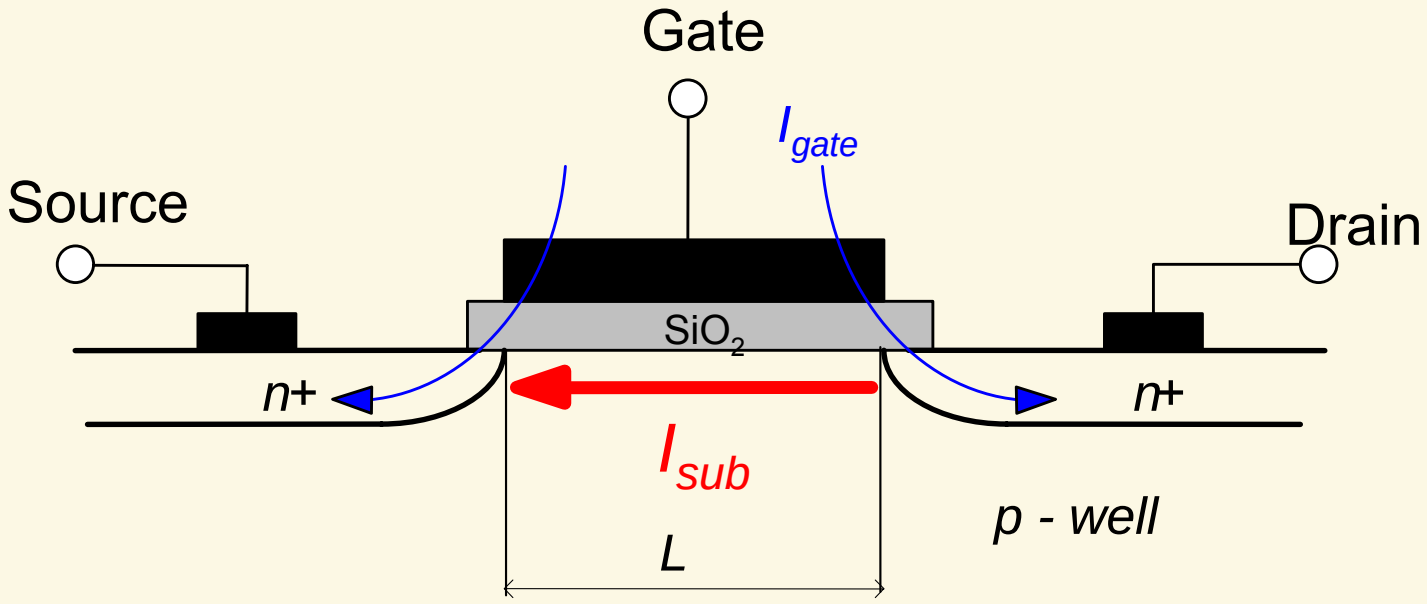
Dynamic Power vs. Leakage



Intel, '02

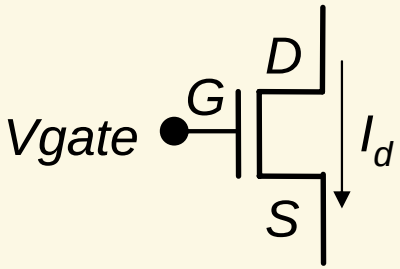
Power Dissipation in CMOS

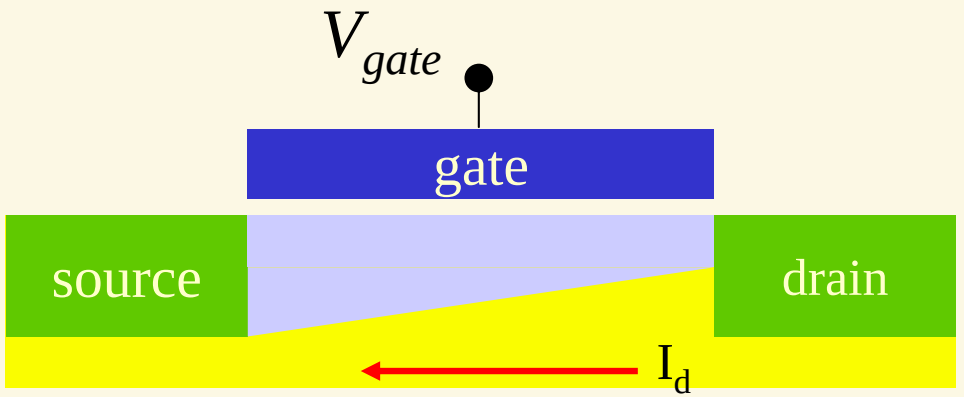




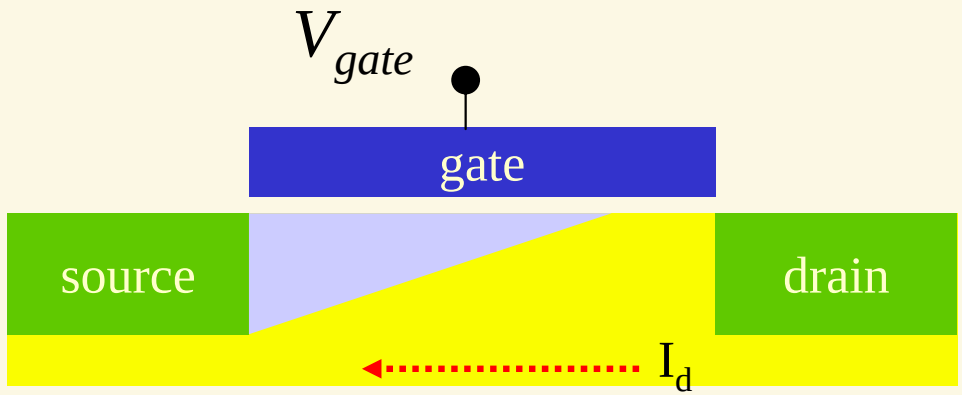
- I_{sub} occurs if $V_{GS} < V_{th}$
- carriers move by diffusion along the surface
- ***I_{sub} dominates leakage***

Threshold Voltage V_{th}





$V_{gate} > V_{th}$



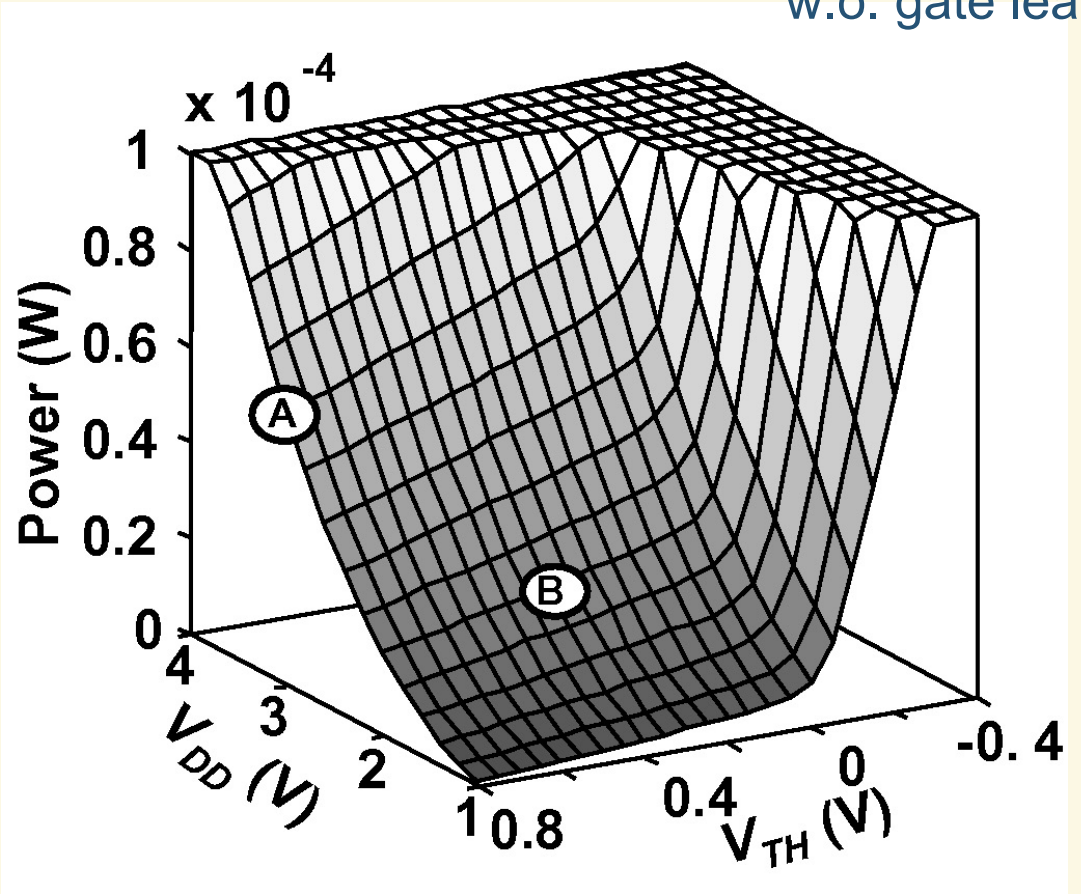
$V_{gate} < V_{th}$

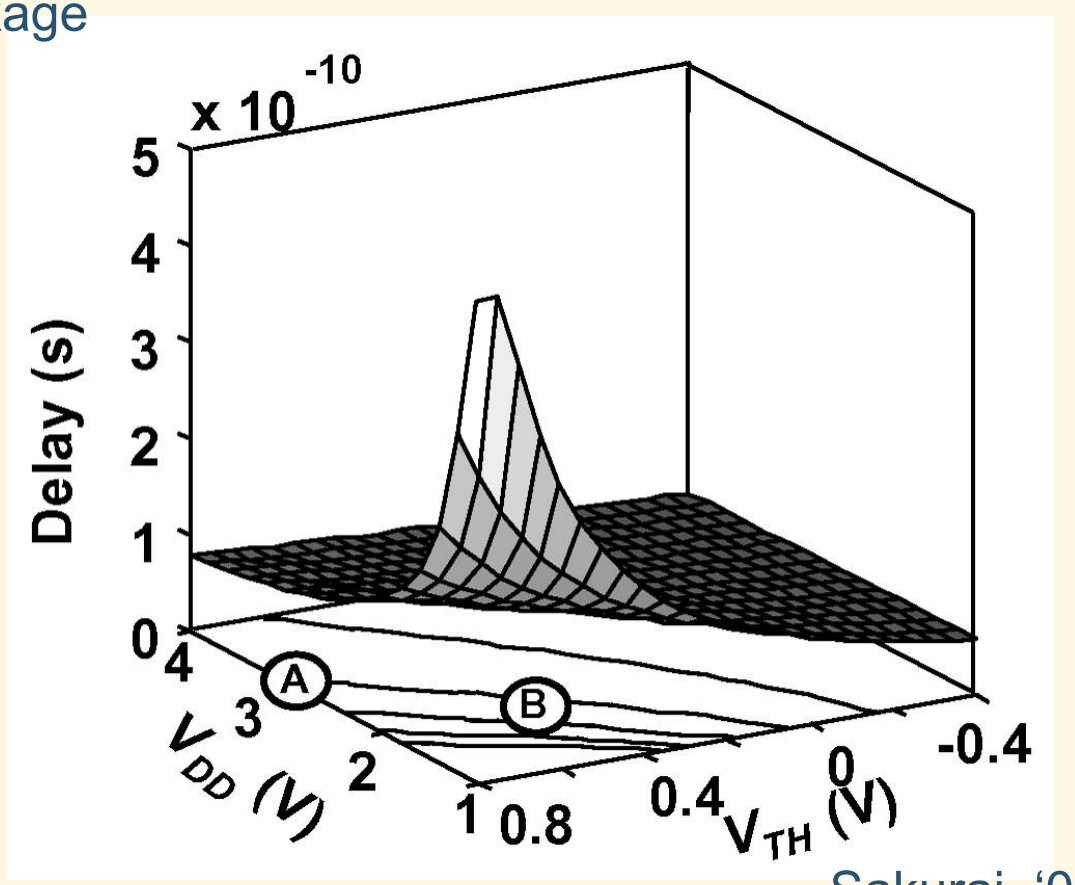
Prof. Wayne Wolf, Princeton University

Power & Delay Dependence

$$P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}{}^2 + I_0 \frac{W_T}{W_0} \cdot 10^{\frac{-V_{TH}}{S}} \cdot V_{DD} \qquad t_d = \frac{k \cdot Q}{I} = \frac{k' \cdot C_L \cdot V_{DD}}{(W/L) \cdot (V_{DD} - V_{TH})^{\alpha_K}}$$

w.o. gate leakage





Sakurai, '01

Power & Delay Dependence

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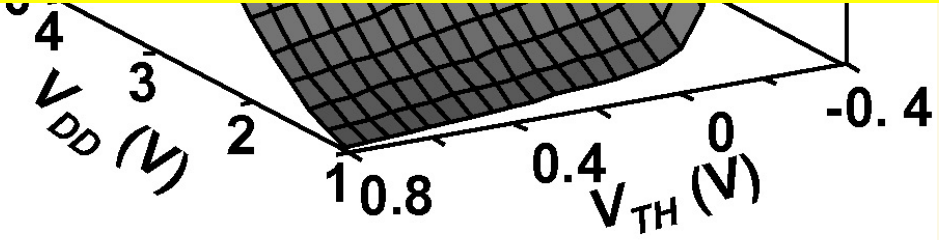
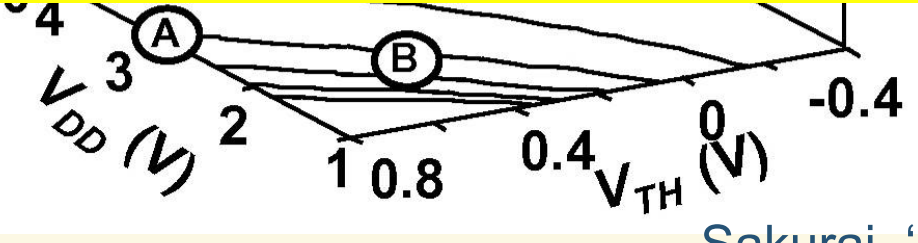
Problem:

fast transistors with high power dissipation (low V_{th})

or

slow transistors with low power dissipation (high V_{th})



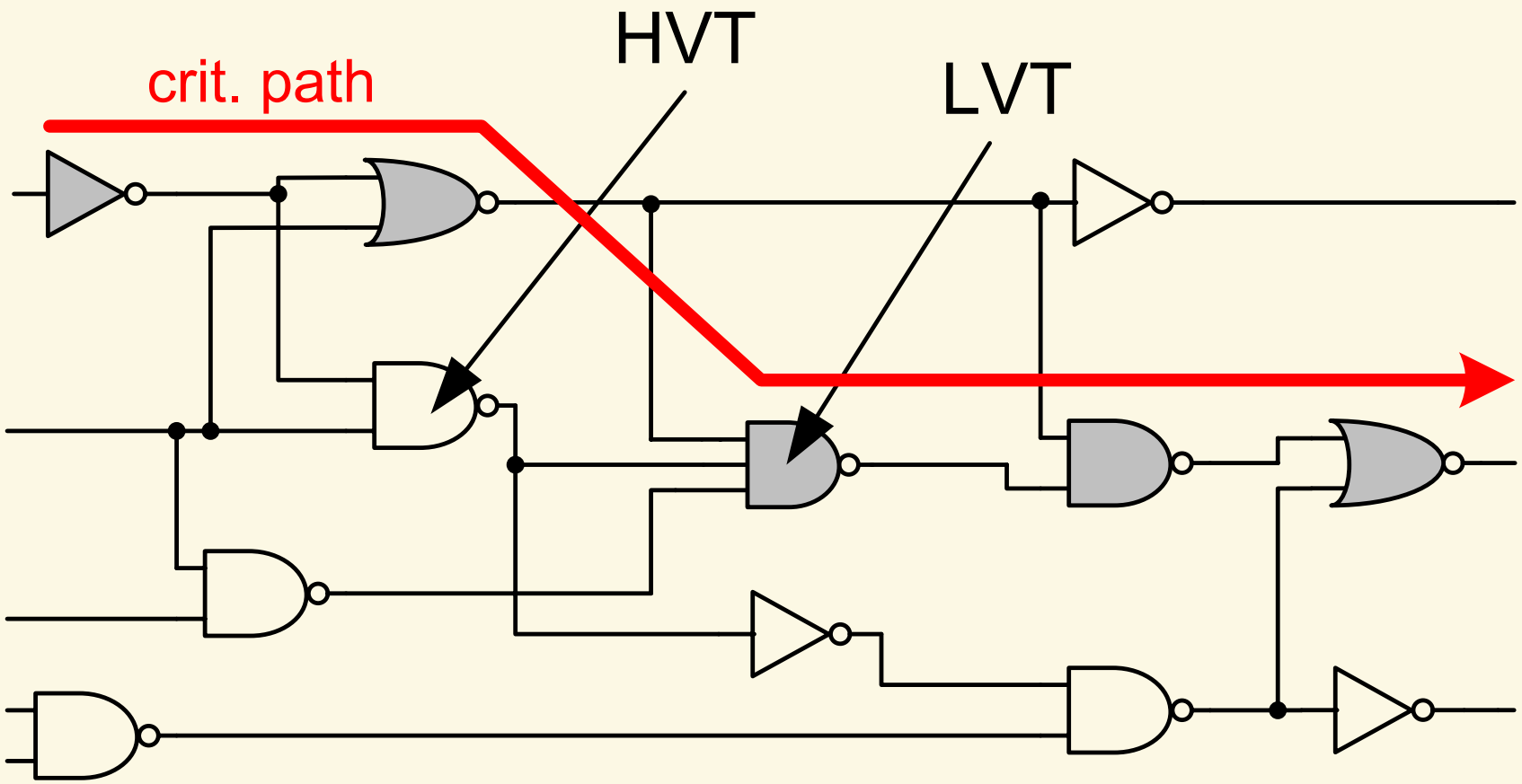


Sakurai, '01

Dual Threshold Voltages (DTCMOS)

- Use different V_{th}'s
  - use lower threshold for devices on the critical paths
  - use higher threshold for devices off the critical paths
- Decrease power without reducing performance
- Approaches at:
  - Gate level (V.Sundararajan, et al., LPED'99)
  - Transistor level (L.Wei, et al., DAC'99)

DTCMOS - Path

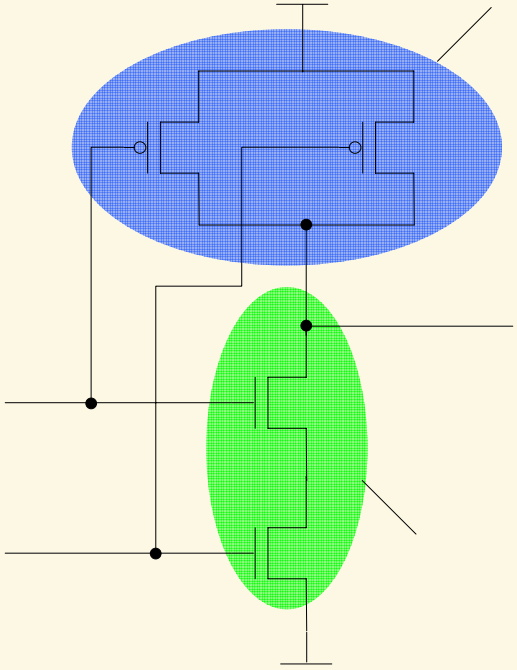


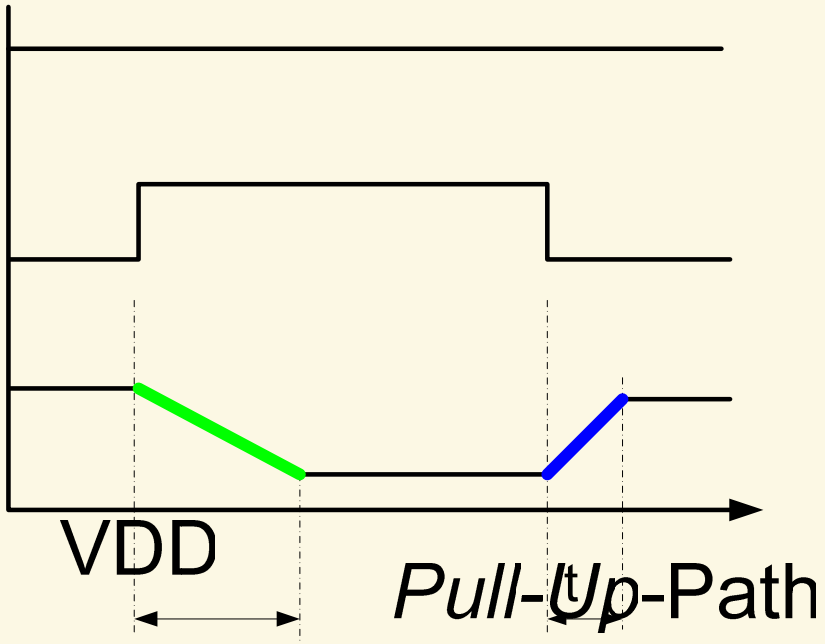
New Approach: Mixed-V_{th} (MVT) CMOS

1. Goal: fast gates keep the delay while leakage decreases

if all transistors in gates arestandard dimensioned (= equal delay)

→ different evaluation times





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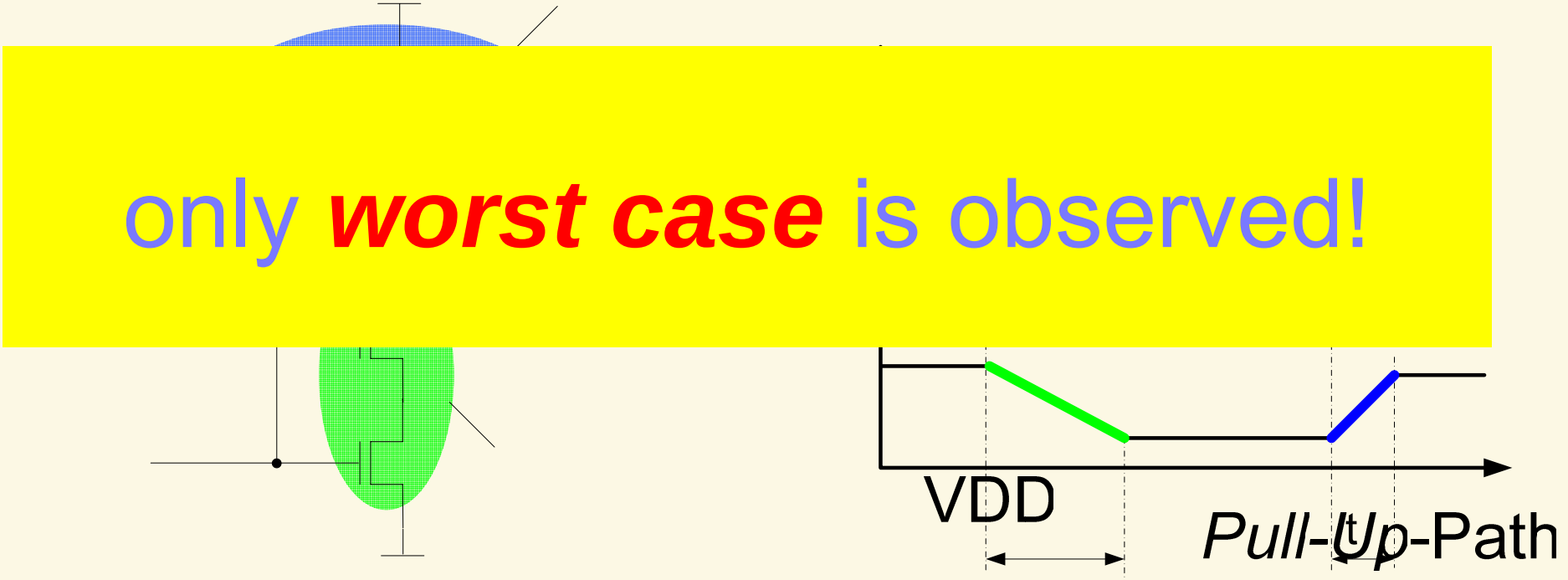


1. Goal (fast low leakage gates)

Up to now: sizing of gates → Reduction of dynamic power dissipation

→ *idea:* use different threshold voltages within a gate to adapt the slopes

↳
- strong reduction of leakage currents
- delay stays constant

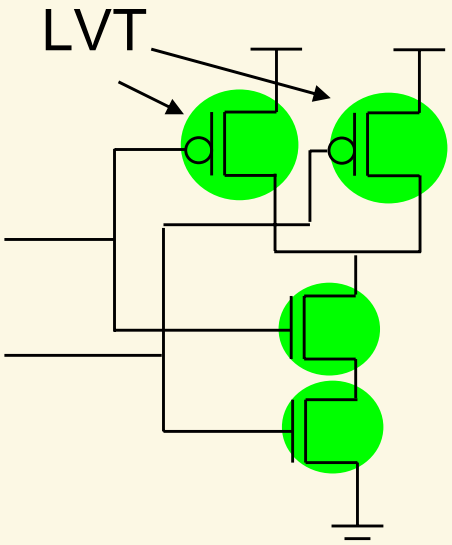
(MVT) CMOS cont'd

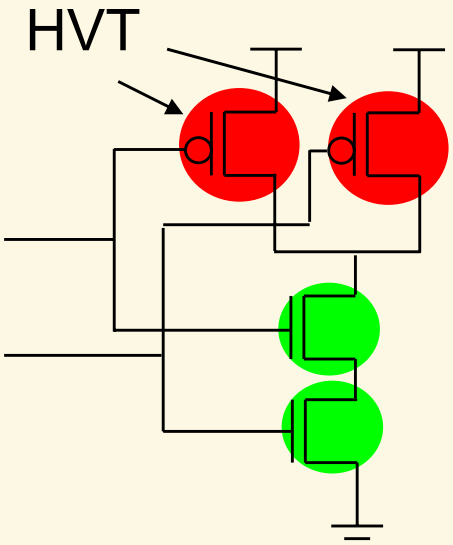
2. Goal: additionally gate types at constant mask count

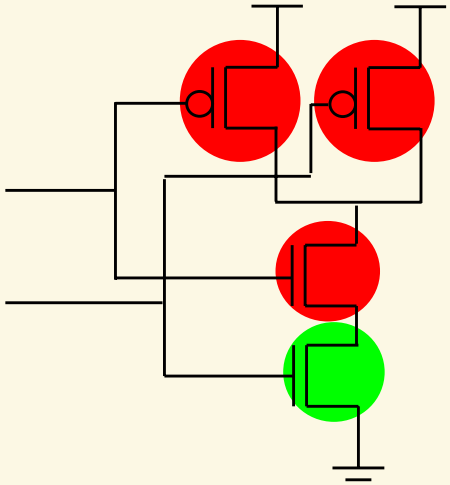
- only two gate types in DTCMOS at gate level (HVT, LVT)
- problem: more LVT gates after optimization as needed to keep the delay

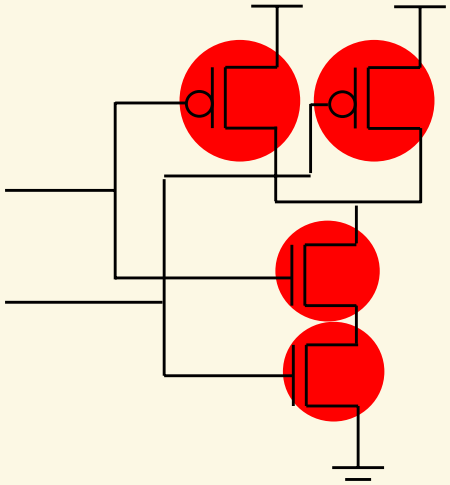
→ *idea:* mixed threshold voltages within a gate

MVT- NAND2









LVT gate

- all MOS have low V_{th}
- rise time is shorter than fall time
- ***minimum delay cell***

M-LVT gate

- PMOS have high V_{th}
- rise and fall time are nearly the same
- ***minimum delay cell***

MVT gate

- PMOS and upper NMOS have high V_{th}
- ***middle delay cell***

HVT gate

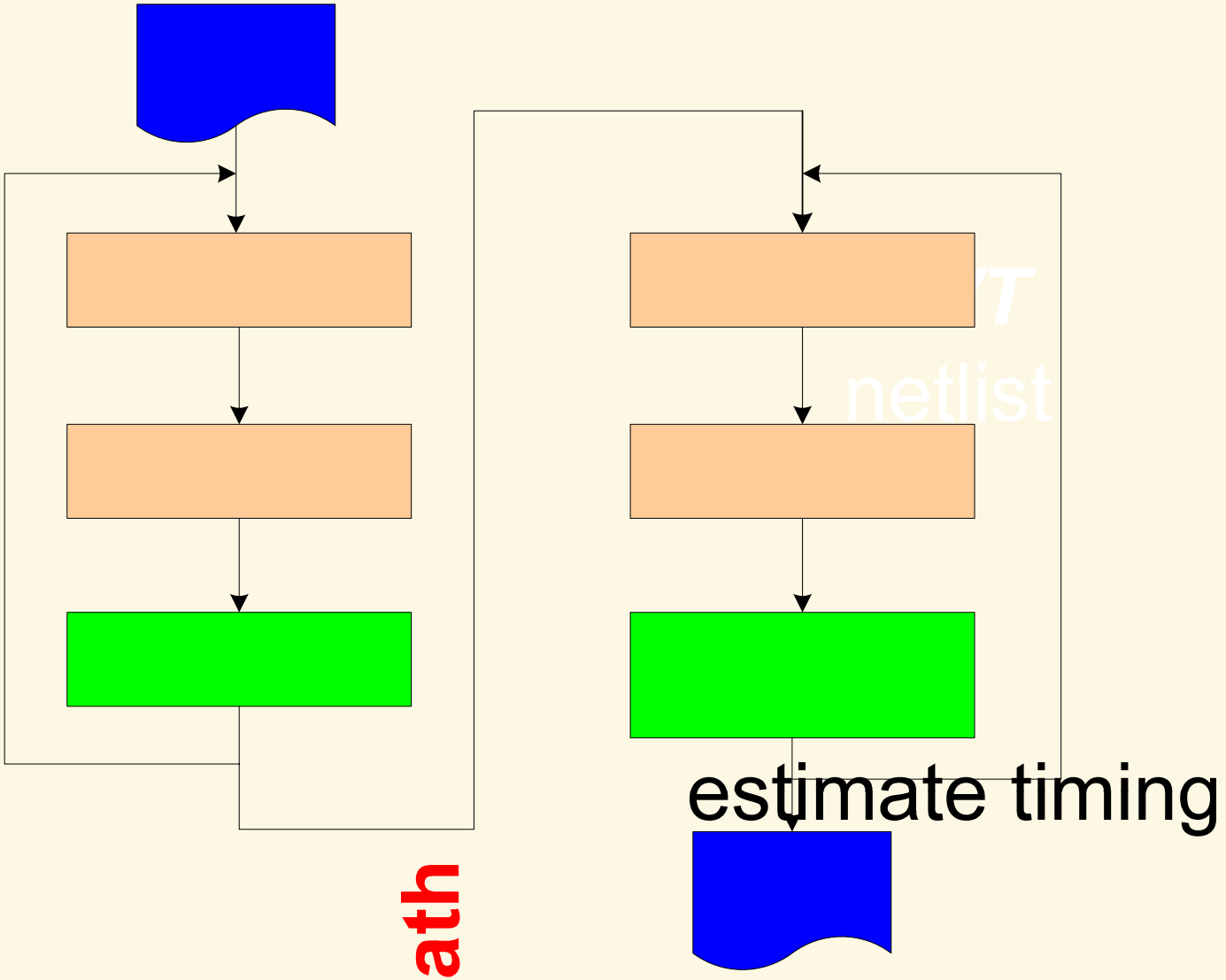
- all MOS have high V_{th}
- ***maximum delay cell***

Gate characteristics

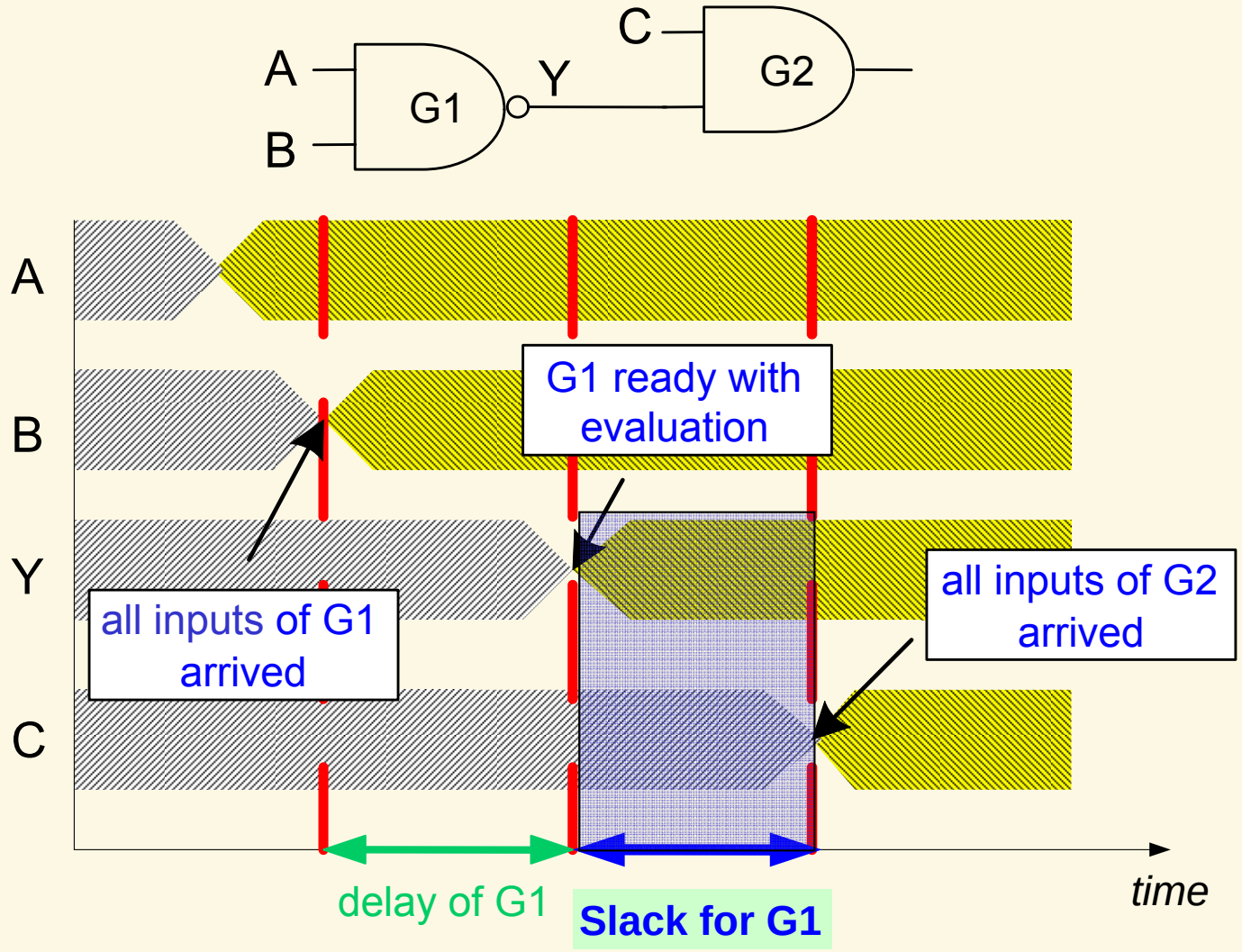
		LVT	M-LVT	MVT	HVT
I_{leak} [nA]	E_{in} = 00	**58**	**58**	**46**	**41**
	E_{in} = 01	**101**	**101**	**46**	**43**
	E_{in} = 10	**89**	**89**	**84**	**37**
	E_{in} = 11	**236**	**19**	**19**	**19**
$I_{average}$		**121 nA**	**67 nA**	**48 nA**	**35 nA**
Delay (t_d)		**53 ps**	**53 ps**	**60 ps**	**71 ps**

BPTM 65nm technology

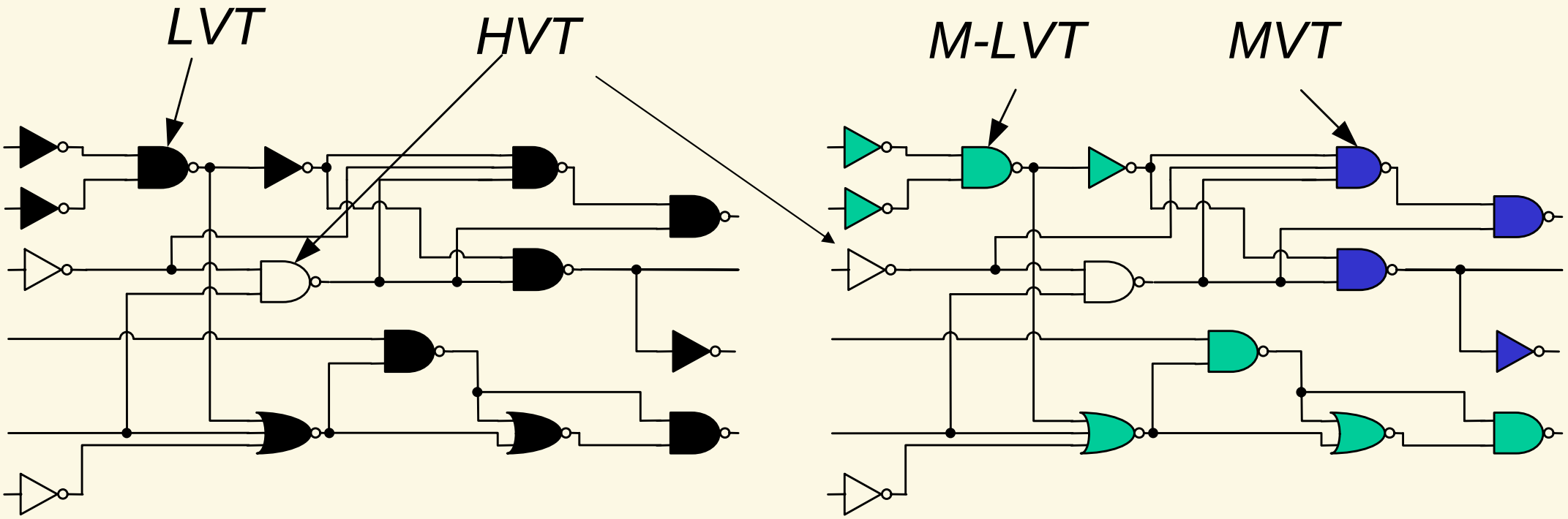
Design flow



Slack


A
B
G1
Y
C
G2
A
B
Y
C
G1 ready with evaluation
all inputs of G1 arrived
all inputs of G2 arrived
delay of G1
Slack for G1
time

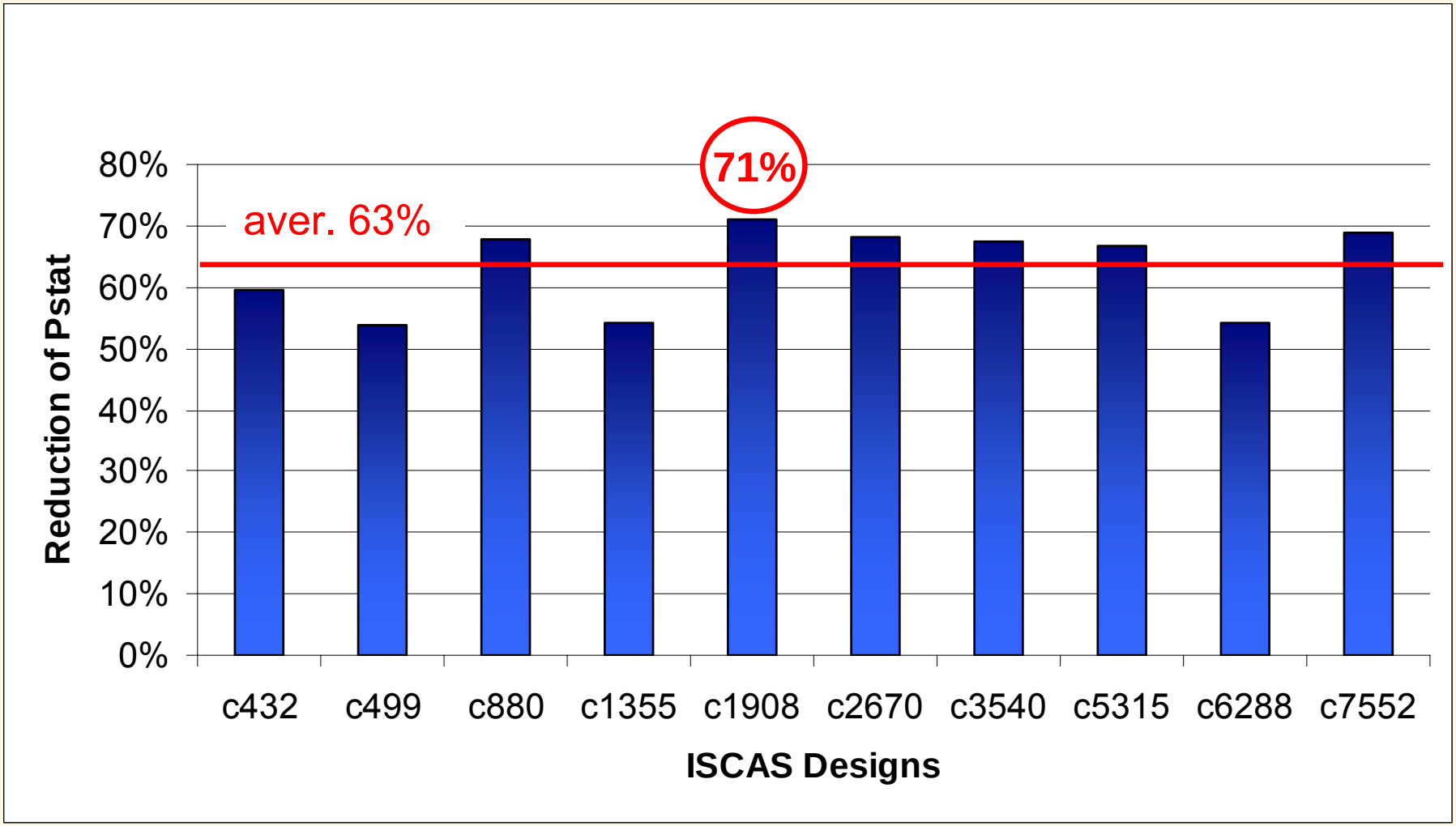
MVT - Paths



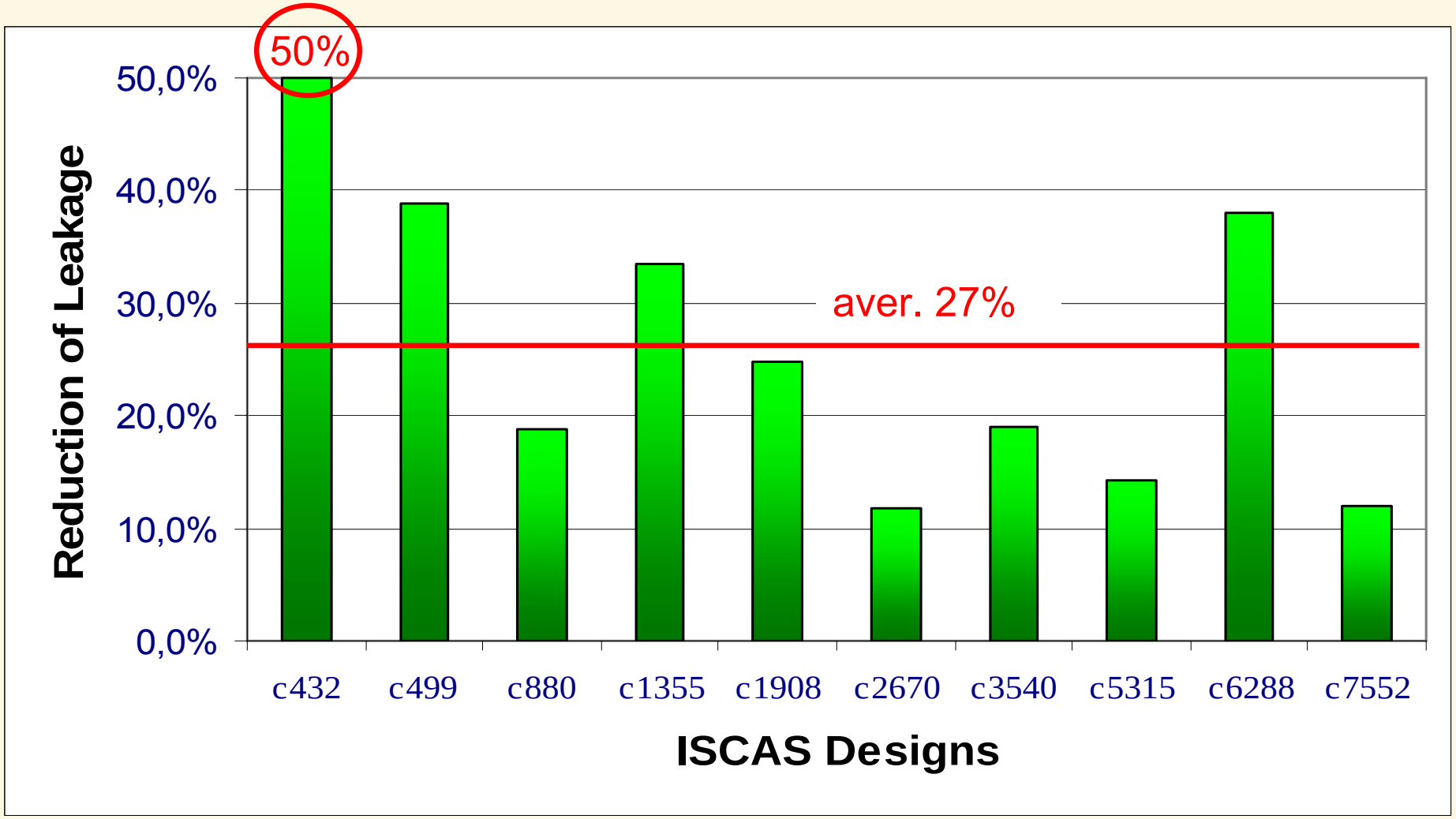
Up to now: *two kinds of cells*
(Dual-Threshold CMOS)

MVT-CMOS

MVT vs. LVT implementation



MVT vs. DTCMOS implementation



Publications (MVT)

- F. Sill, F. Grassert, D. Timmermann, ***Reduzierung des Leistungsverbrauchs in Deep Submicron Designs***, Symposium Maritime Elektrotechnik, Elektronik und Informationstechnik, Rostock, Deutschland, Juni 2004

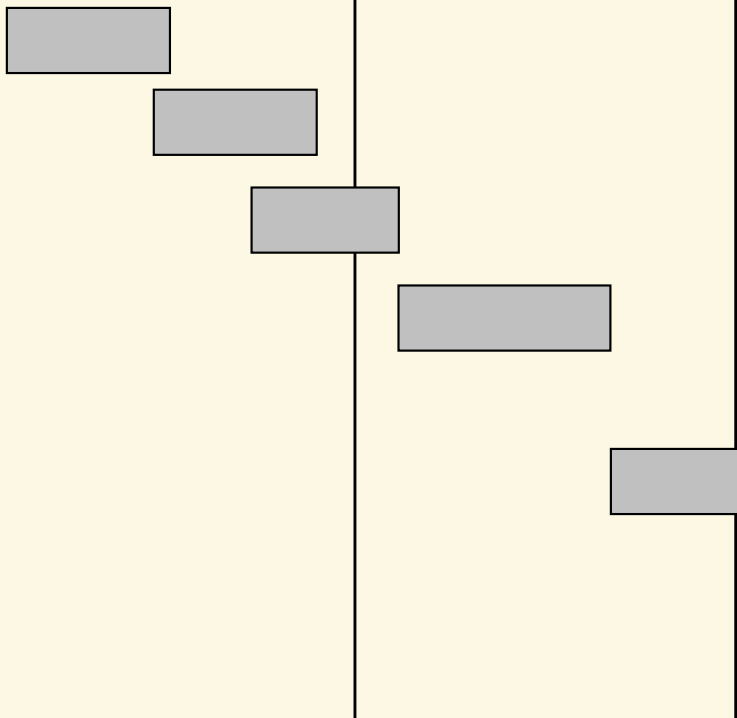
- F. Sill, F. Grassert, D. Timmermann, ***Low Power Gate-level Design with Mixed-Vth (MVT) Techniques***, 17th Symposium on Integrated Circuits and Systems (SBCCI), Porto de Galinhas, Pernambuco, Brasilien, September 2004

- F. Sill, F. Grassert, D. Timmermann, ***Reducing Leakage with Mixed-Vth (MVT)***, 18th Conference on VLSI Design, Kalkutta, Indien, January 2005

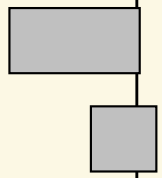
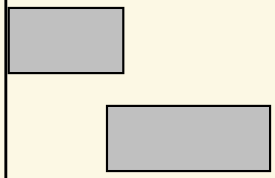
Conclusion

- Subthreshold current I_{sub} dominates leakage power
- Mixed-V_{th} (MVT) reduces I_{sub}
- Design flow developed
- Average 67% *(vs. LVT)* and 27% *(vs. DTCMOS)* leakage reduction at constant delay
- 1 national and 2 international publications

4. Outlook

Tasks	2004	2005	
	4. Quarter	1. Quarter	2. Quarter
MVT • Extension of the library • Development of algorithms for *Sizing* • Analyzation of dynamic power • Additional approaches for reduction of *gate-leakage* • Comparison of realization of different V_{th} (modif. of T_{ox}, NDEP) • Optimization of algorithms (e.g. valuation of gates)			

Outlook cont‘d

Tasks	2005		
	2. Quarter	3. Quarter	4. Quarter
AC-TSPC • Analysis of leakage effects • Combination with MVT			
Multimedia circuit • Implementation with AC-TSPC • Implementation with MVT			
Writing			

Thank you!

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