Reliability and Energy Dissipation in Ultra Deep Submicron Designs

Institute of Applied Microelectronics and Computer Science

Reliability and Energy Dissipation in Ultra Deep Submicron Designs

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Outline

1) Introduction
2) Trends
3) Reasons for Energy Dissipation and Variability
4) Solutions
5) Summary

Why thinking about Energy and Reliability?

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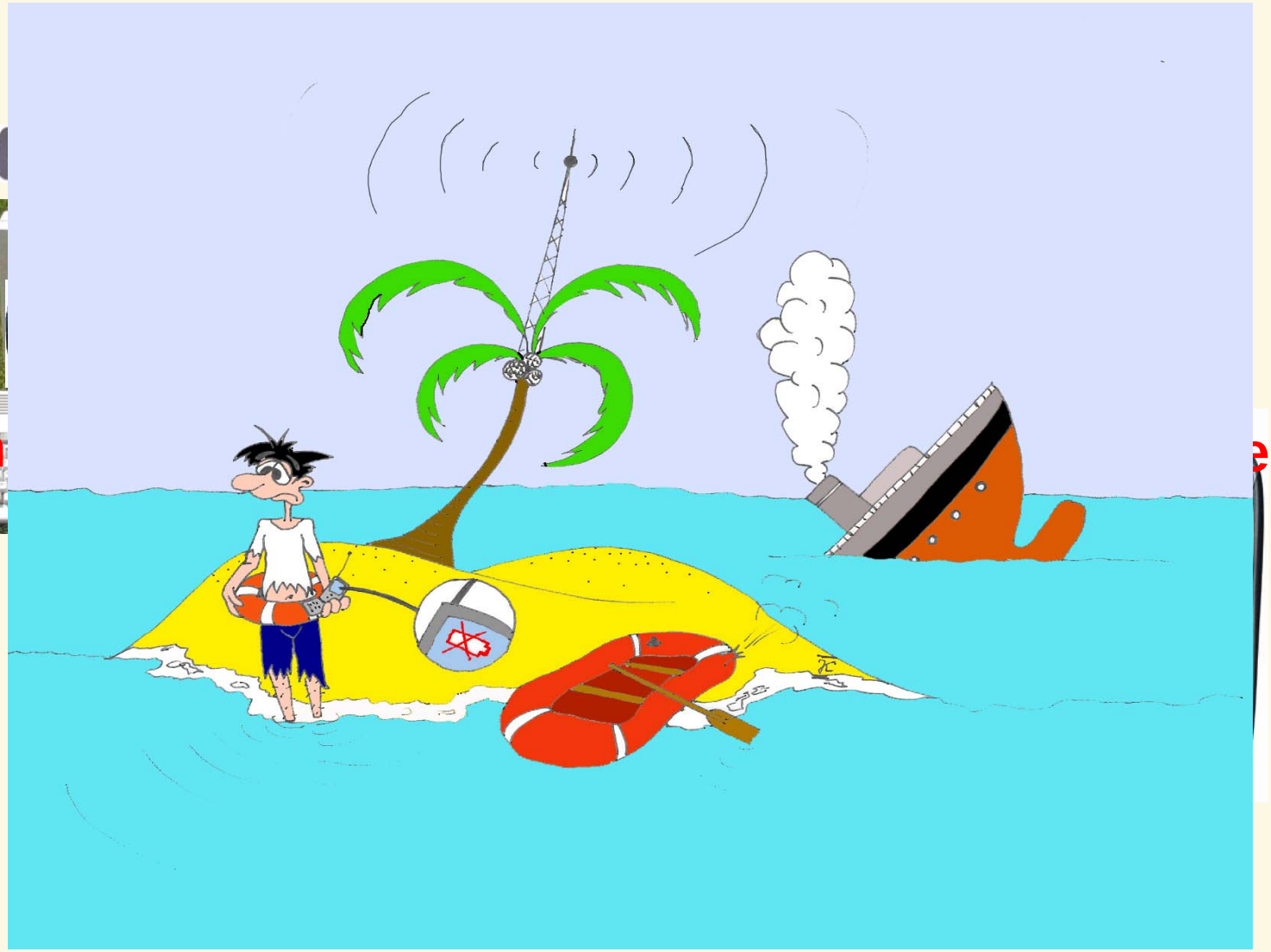


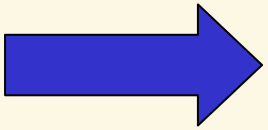
ect rate

Why is Variability critical?

Variability = *variation of process / technology parameters*

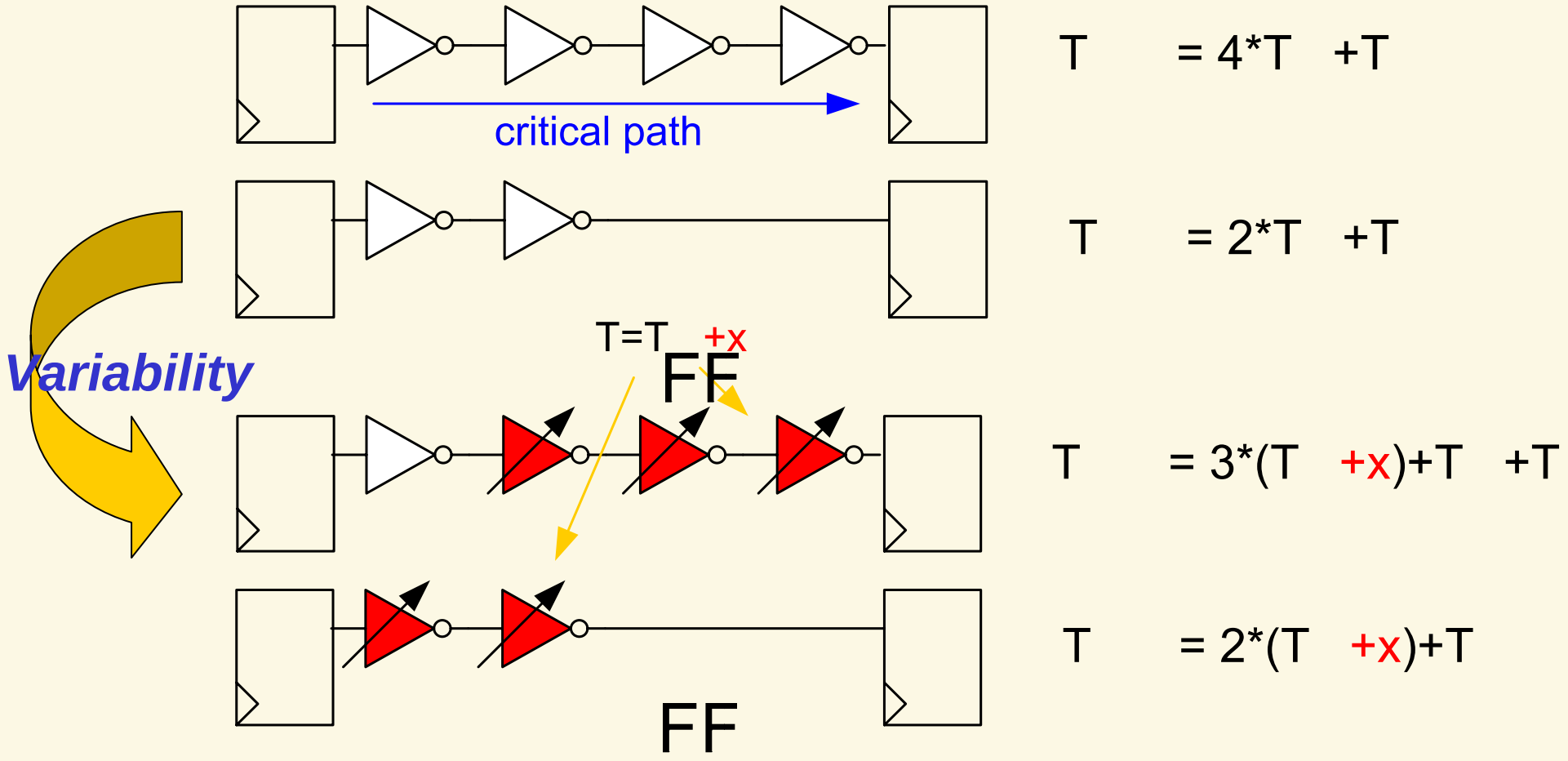
Variability result in:

- Increasing delay of logic elements / wires
- Defect logic elements / wires



- Failed chips (defect Yield)
- Failed chips while run time (Reliability)
- Chips failed desired performance (= *delay*) (parametric Yield)

Variability in critical paths



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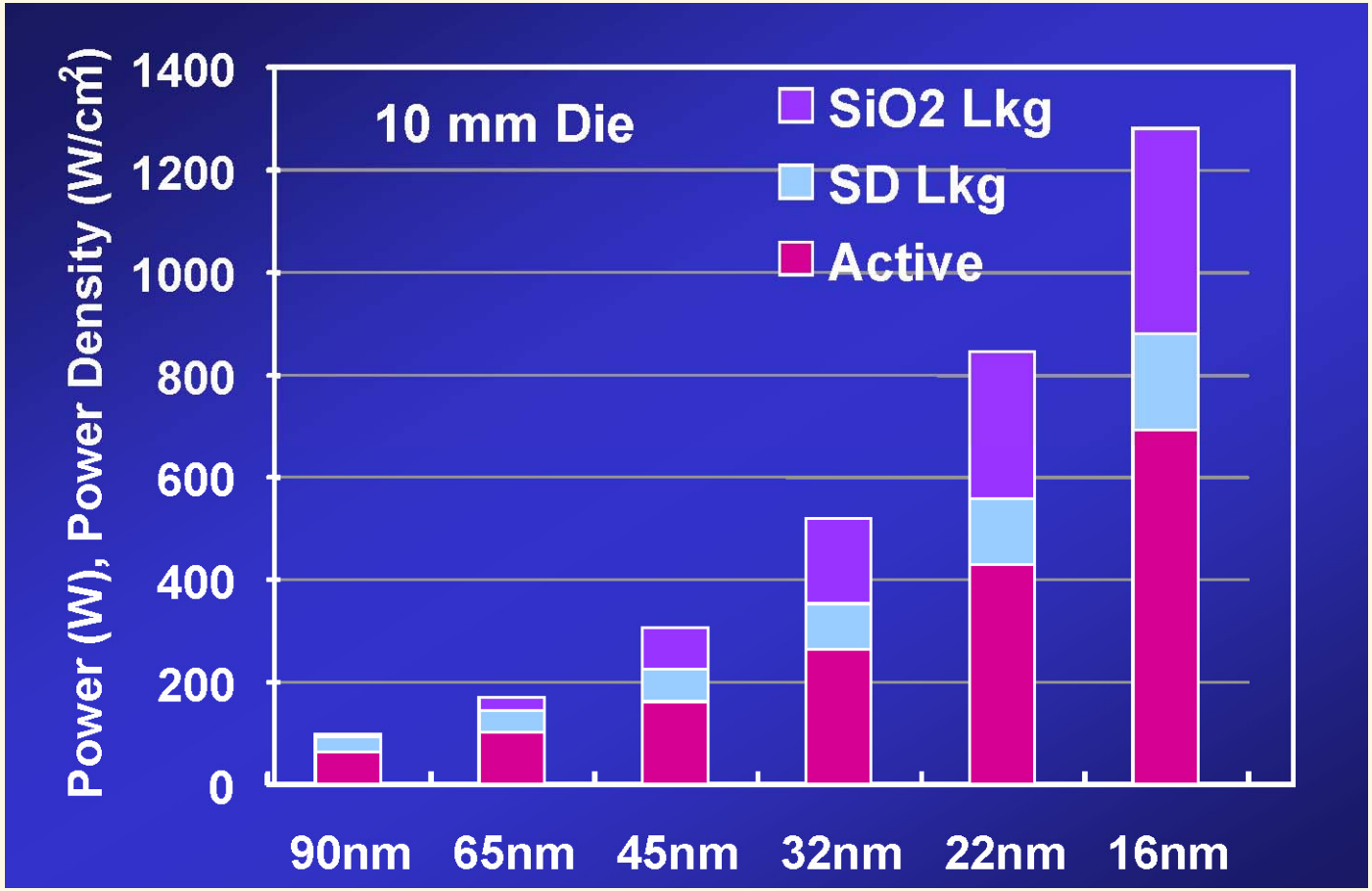
Trends: ITRS Roadmap

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Technology Node (nm)	90	65	45	32	22	16	11	8
Integration Capacity (BT)	2	4	8	16	32	64	128	256
Delay = CV/I scaling	0.7	~0.7	>0.7	Delay scaling will slow down				
Energy/Logic Op scaling	>0.35	>0.5	>0.5	Energy scaling will slow down				
Bulk Planar CMOS	High Probability						Low Probability	
Alternate, 3G etc	Low Probability						High Probability	
Variability	Medium			High			Very High	
ILD (K)	~3	<3	Reduce slowly towards 2-2.5					
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	6-7	7-8	8-9	0.5 to 1 layer per generation				

from: S. Brokar, VLSI'05

Power Trends



from: S. Brokar, VLSI'05

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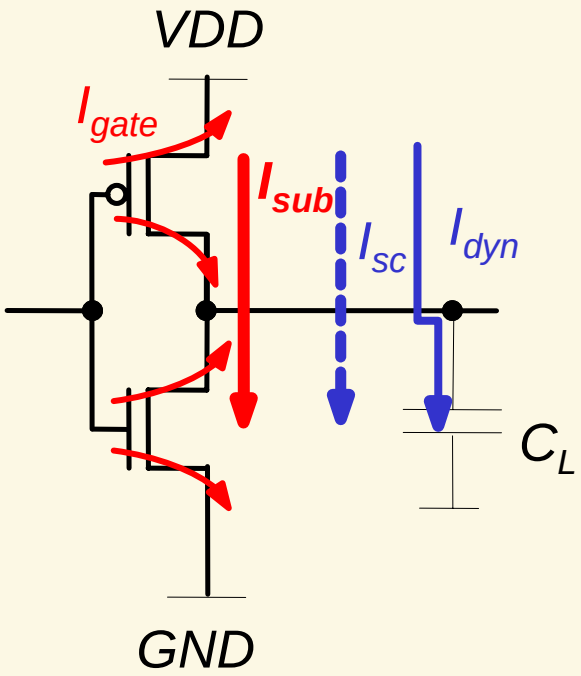
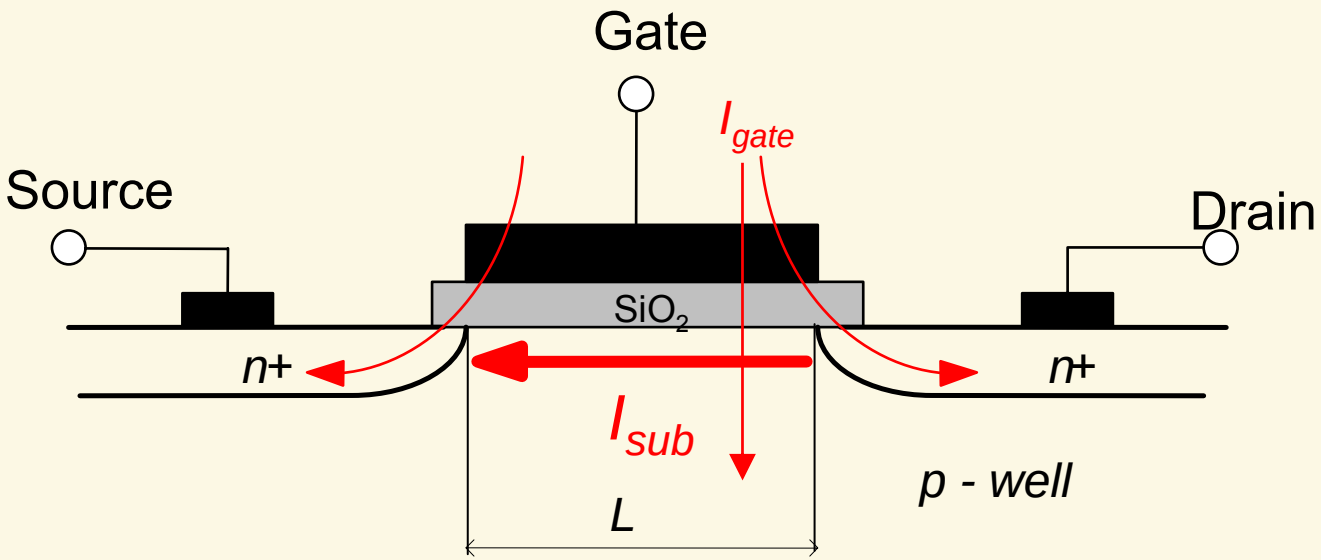
3) Reasons
   - Sources of Energy Dissipation
   - Sources of Variability
4) Solutions
5) Summary

Sources of Energy Dissipation

$$\text{Energy} = E_{switching} + E_{leakage}$$

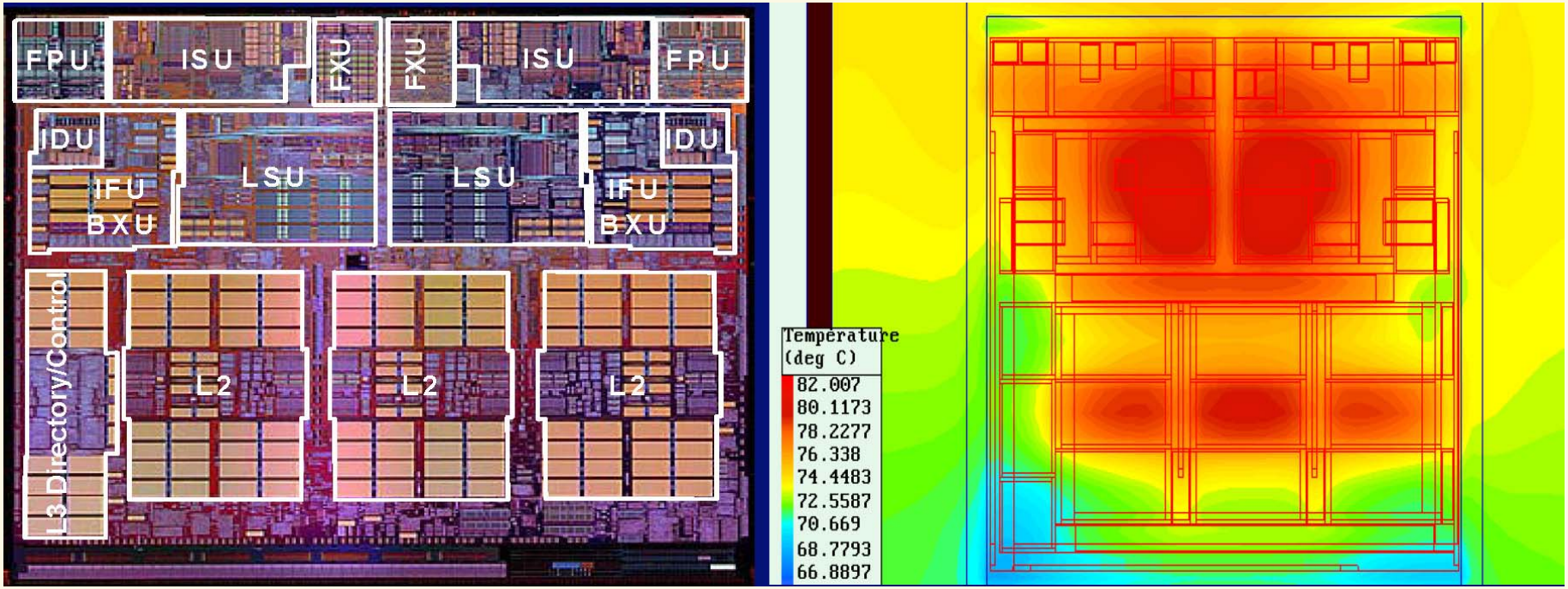
$$\text{Energy} = (C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f_{0\rightarrow1} + V_{DD} I_{leakage})*t$$





Sources of Variability (1)

Temperature Variations + Hot spots

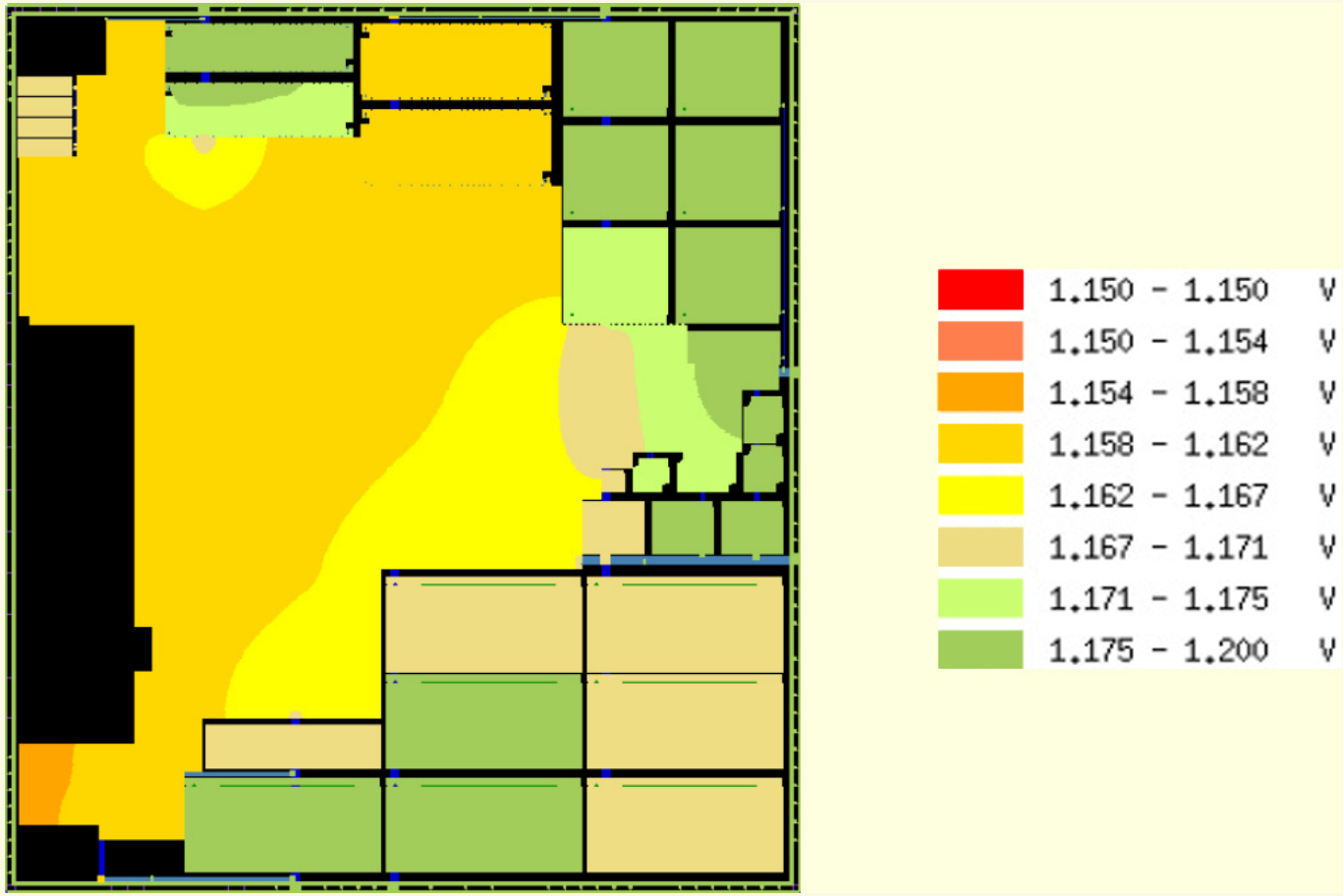


Power4 Server Chip

from: Devgan, ICCAD'03

Sources of Variability (2)

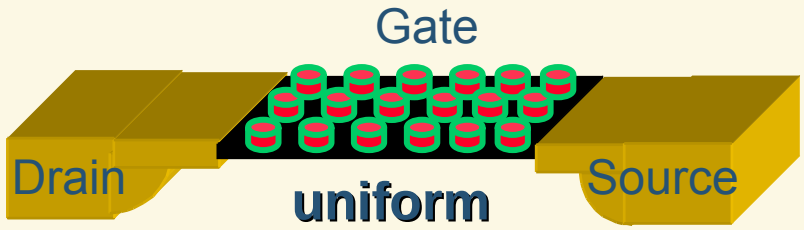
Supply Voltage Drop

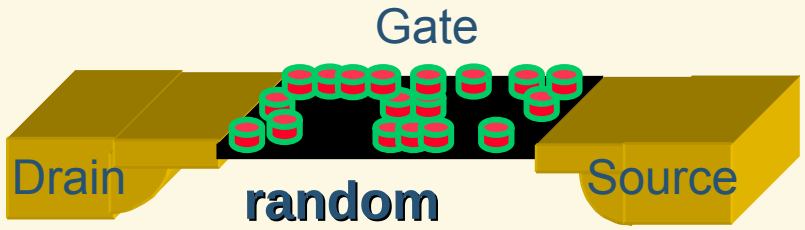


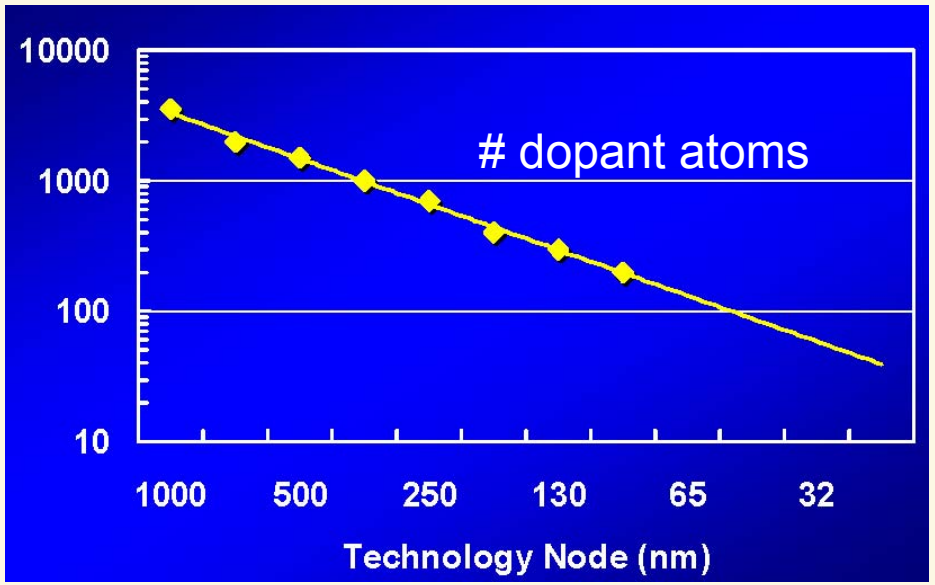
from: S.Trester,2005

Sources of Variability (3)

Random dopant fluctuations







from: S. Brokar, VLSI'05

More sources

- Electromigration
- Varying line width
- Soft errors (alpha particles, cosmic rays)
- …

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   - Goals
   - Triple Module Redundancy
   - Self adaptive design
   - Critical paths
   - Redundant Transistor Insertion
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Solutions: Goals

1) Increase defect and parametric Yield

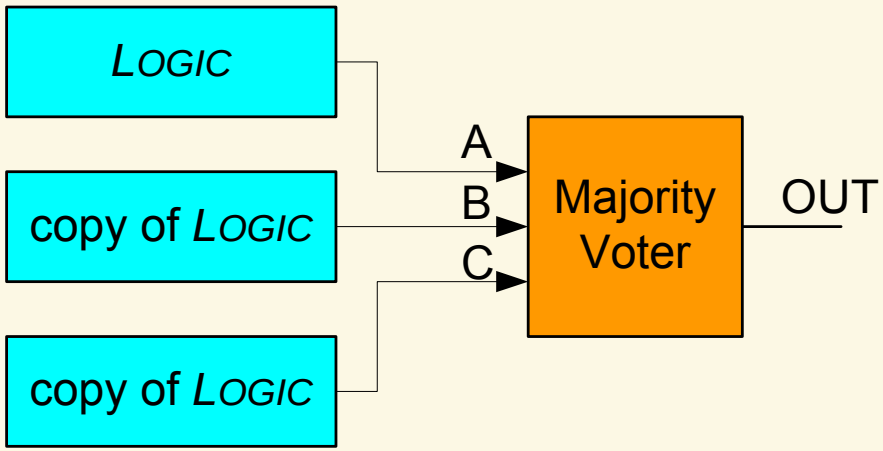
$$Y = \frac{\#\ Good\ Chips\ on\ Wafer}{Total\ \#\ Chips} 100\%$$

2) Increase Reliability

3) Decrease Energy dissipation @ nearly constant Reliability and Yield

Triple Module Redundancy (TMR)

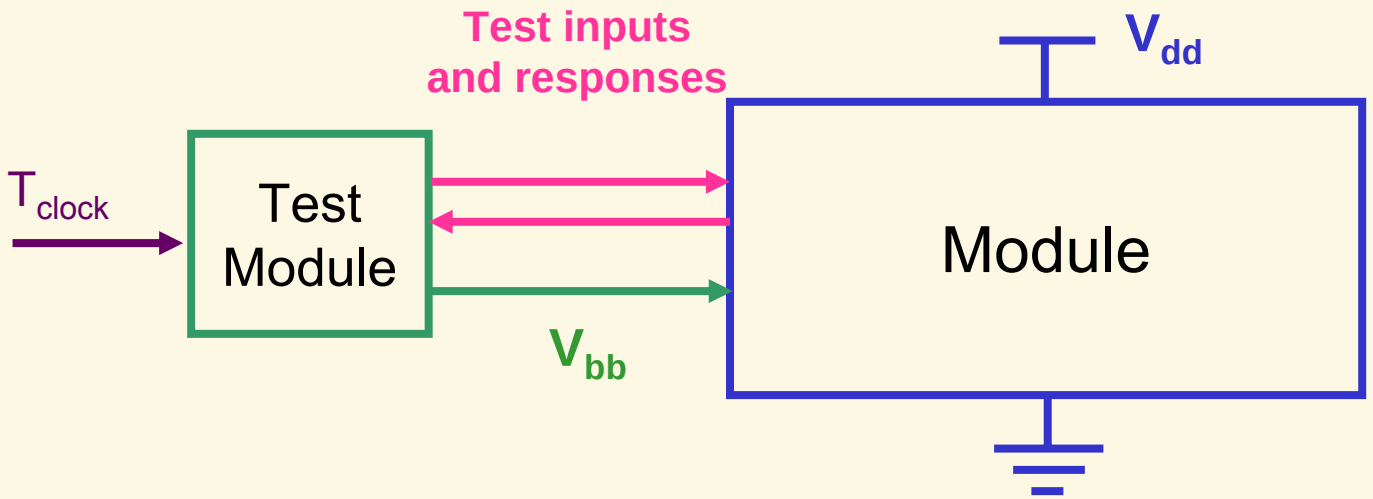
- Implementation of three copies of the same circuit
- *Majority Voter* decides (bit-wise)
- Reliability $R_{TMR} \rightarrow \boldsymbol{R^3+3R^2(1-R)}$, Energy $\rightarrow$ ***x3***



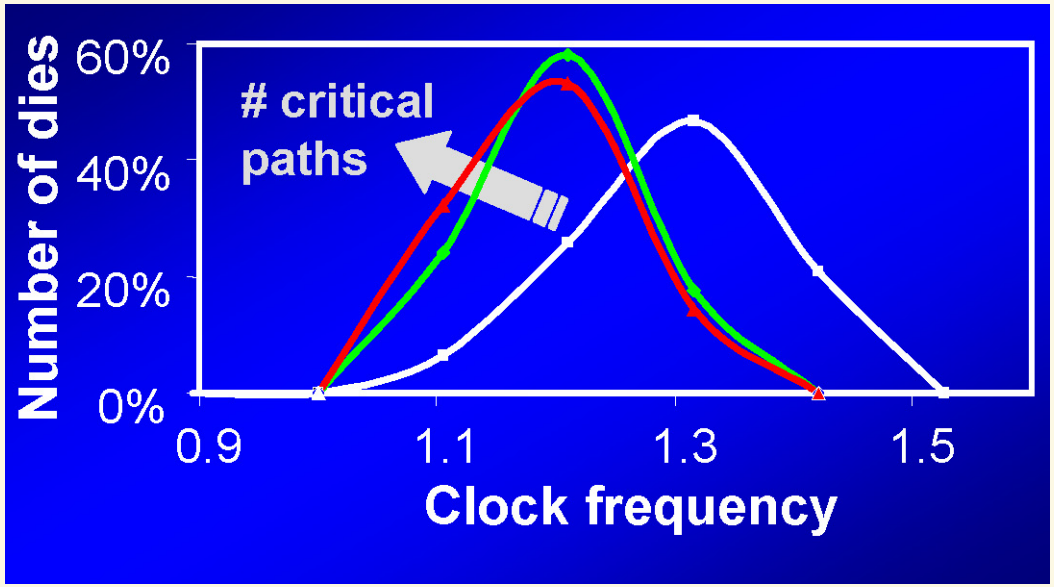
A	B	C	OUT
1	1	0	1
0	0	1	0
0	1	0	0
0	1	1	1

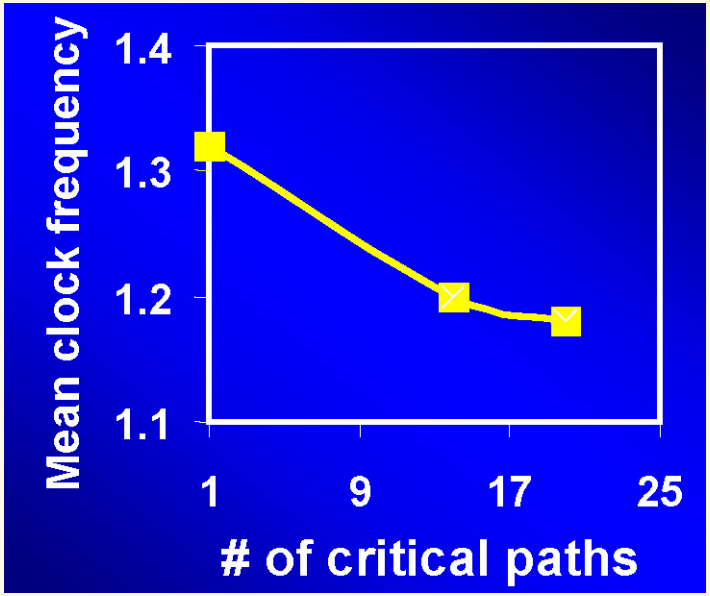
Self adaptive design

- Extend idea of clock domains to Adaptive Power Domains
- Tackle static process and slowly varying timing variations
- Control VDD, V_{th} *(indirectly by body bias)*, T_{clock} by calibration @ Power On



Critical Paths



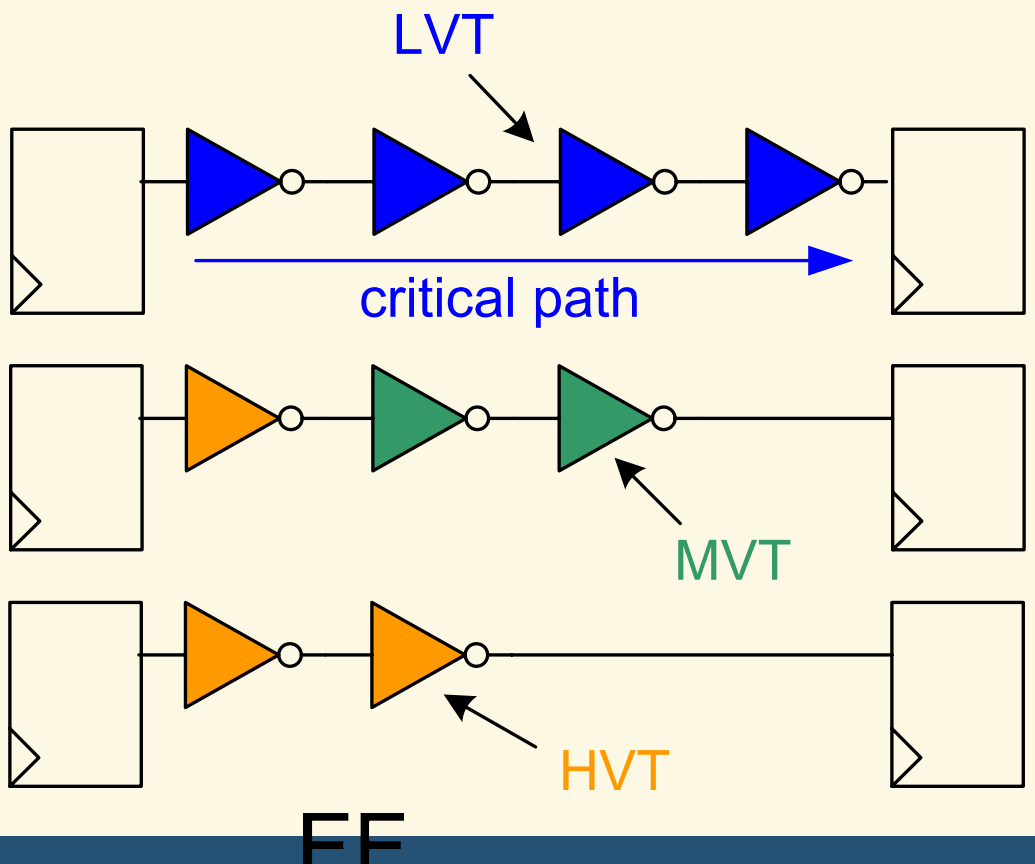


from: S. Brokar, VLSI'05

- **Problem**: variations of gate properties in critical paths directly determine variation of clock frequency
- **Solution**: Reduce count of critical paths

Critical Paths and MVT

Idea of MVT approach:



use different types of Gates:

LVT: fast, high leakage

MVT: medium speed,
medium leakage

HVT: slow, low leakage

Leakage reduced but count of critical paths increased!

Critical Paths and MVT cont'd

Problem: Leakage reduced but count of critical paths increased!

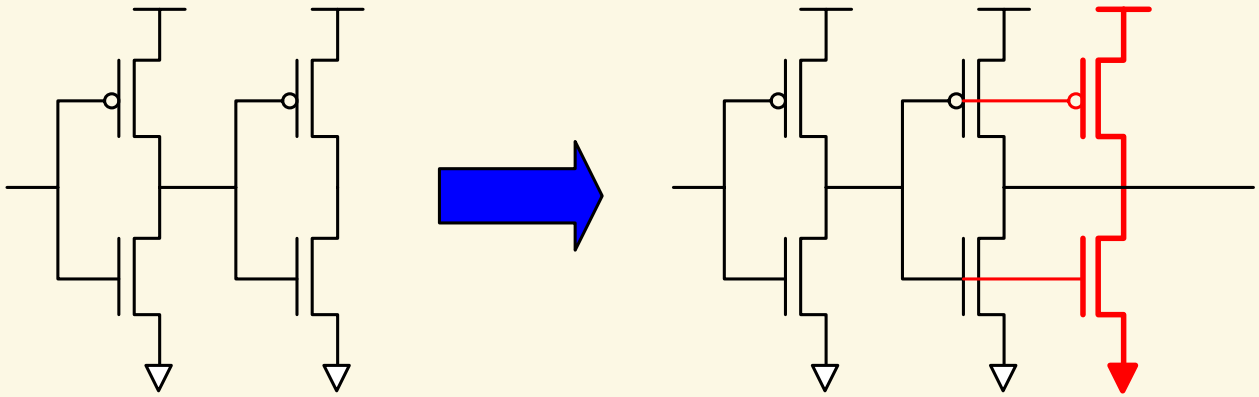
Solution: Use of HVT or MVT gates only if *reliability does not fall below desired value*

Result: MVT allows adapted reliability

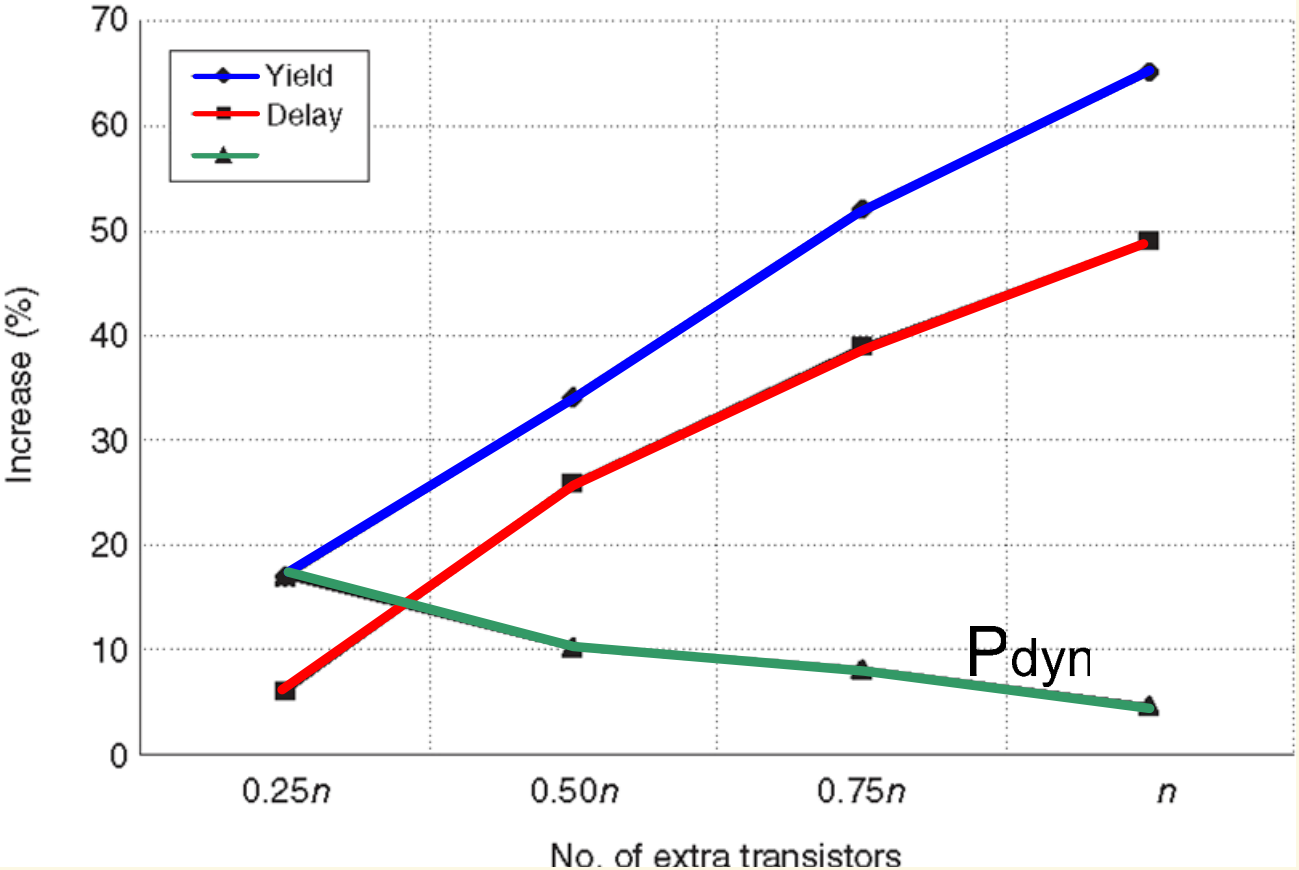
User can decide between weighting of reducing leaking or increasing reliability

Redundant Transistor Insertion

- Random insertion of redundant transistors
- Trade-off between *Yield* and *Power Dissipation*, *Area*, and *Delay*
- For constant delay: redundant transistors only in non-critical paths



Redundant Transistor Insertion cont'd



Siristana, IEEE D&T,2004

Summary

- Energy dissipation and variations top issues in deep submicron designs
- Improvement of yield and reliability only as trade-off with energy dissipation and delay
- Redundant design and reduction of critical path count increases reliability

Thank you!